



LC35256FM, FT-55U/70U

256K (32768 words × 8 bits) SRAM
Control Pins: \overline{OE} and \overline{CE}

Preliminary

Overview

The LC35256FM and LC35256FT are asynchronous silicon-gate CMOS SRAMs with a 32K-word by 8-bit structure. These are full-CMOS devices with 6 transistors per memory cell, and feature low-voltage operation, a low operating current drain, and an ultralow standby current. Control inputs include \overline{OE} for fast memory access and \overline{CE} (chip enable) for power saving and device selection. This makes these devices optimal for systems that require low power or battery backup, and makes memory expansion easy. The ultralow standby current allows these devices to be used with capacitor backup as well.

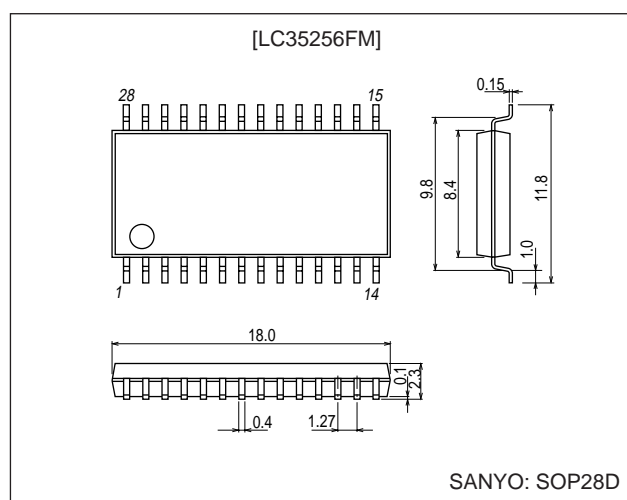
Features

- Supply voltage range: 4.5 to 5.5 V
- Access time at 5 V operation:
LC35256FM, FT-55U: 55 ns (maximum)
LC35256FM, FT-70U: 70 ns (maximum)
- Standby current: 3.0 μ A ($T_a \leq 70^\circ\text{C}$)
5.0 μ A ($T_a \leq 85^\circ\text{C}$)
- Operating temperature: -40 to $+85^\circ\text{C}$
- Data retention voltage: 2.0 to 5.5 V
- All I/O levels: TTL compatible
- Input/output shared function pins, 3-state output pins
- No clock required
- Package
28-pin SOP (450 mil) plastic package: LC35256FM
28-pin TSOP (8 × 13.4 mm) plastic package: LC35256FT

Package Dimensions

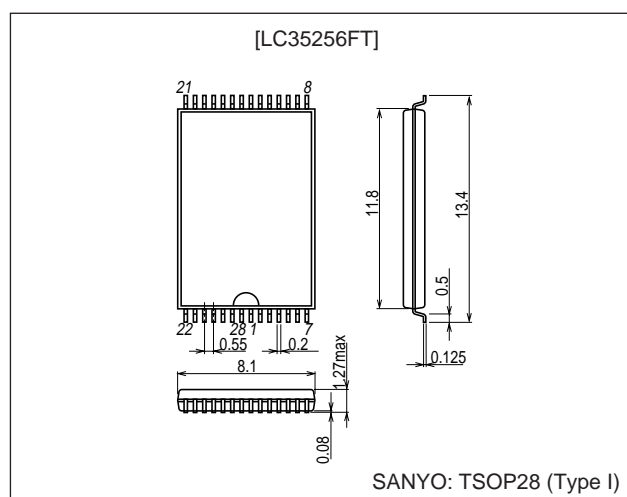
unit: mm

3187A-SOP28D



unit: mm

3221-TSOP28 (Type I)

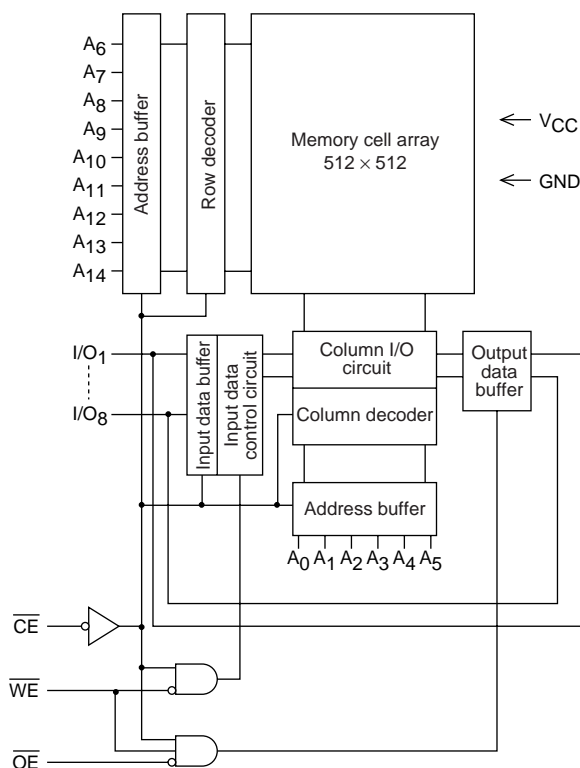
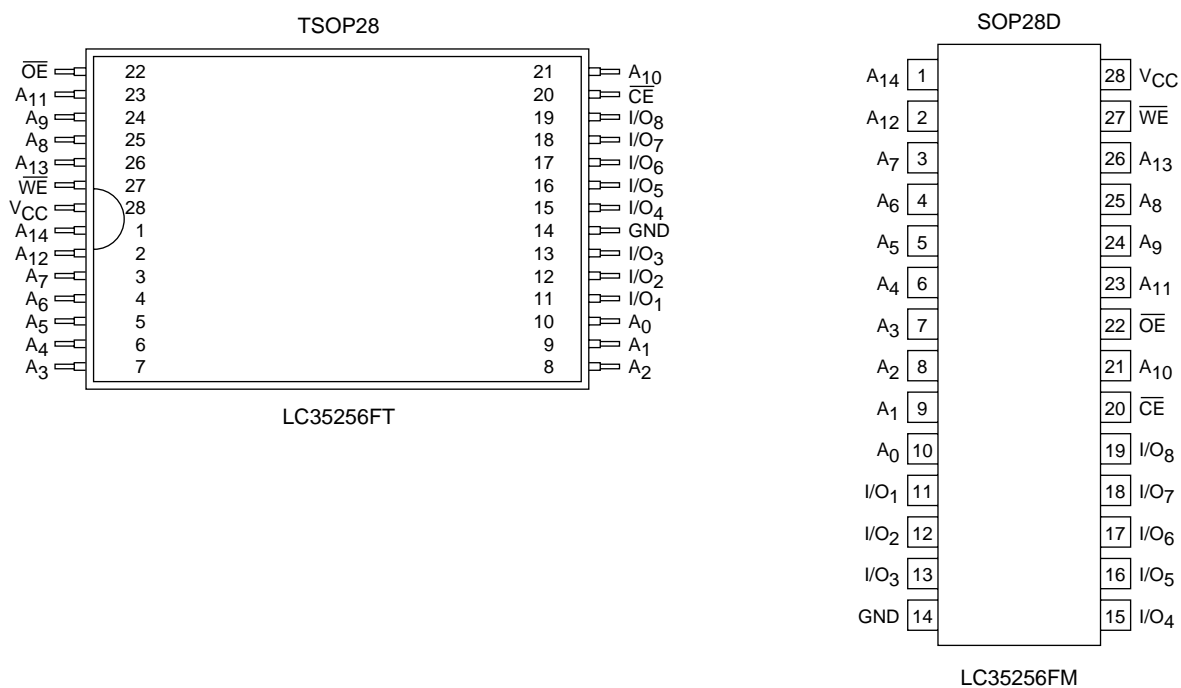


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Pin Functions

| | |
|-----------------|--------------------------|
| A0 to A14 | Address input |
| \overline{WE} | Read/write control input |
| \overline{OE} | Output enable input |
| \overline{CE} | Chip enable input |
| I/O1 to I/O8 | Data I/O |
| V_{CC} , GND | Power supply, ground |

Function Table

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O | Supply current |
|----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Read cycle | L | L | H | Data output | I_{CCA} |
| Write cycle | L | X | L | Data input | I_{CCA} |
| Output disable | L | H | H | High impedance | I_{CCA} |
| Unselected | H | X | X | High impedance | I_{CCS} |

Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------|--------------|------------|-------------------------|------|
| Maximum supply voltage | V_{CC} max | | 7.0 | V |
| Input pin voltage | V_{IN} | | -0.3* to $V_{CC} + 0.3$ | V |
| I/O pin voltage | $V_{I/O}$ | | -0.3 to $V_{CC} + 0.3$ | V |
| Operating temperature | T_{opr} | | -40 to +85 | °C |
| Storage temperature | T_{stg} | | -55 to +125 | °C |

Note: * The minimum value is -3.0 V for pulse widths under 30 ns.

I/O Capacitances at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------|-----------|------------------------|---------|-----|-----|------|
| | | | min | typ | max | |
| I/O pin capacitance | $C_{I/O}$ | $V_{I/O} = 0\text{ V}$ | | 6 | 10 | pF |
| Input pin capacitance | C_I | $V_{IN} = 0\text{ V}$ | | 6 | 10 | pF |

Note: All units are not tested; only samples are tested.

DC Allowable Operating Ranges at $T_a = -40\text{ to }+85^\circ\text{C}$, $V_{CC} = 4.5\text{ to }5.5\text{ V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------|----------|------------|---------|-----|----------------|------|
| | | | min | typ | max | |
| Supply voltage | V_{CC} | | 4.5 | 5.0 | 5.5 | V |
| Input voltage | V_{IH} | | 2.2 | | $V_{CC} + 0.3$ | V |
| | V_{IL} | | -0.3* | | +0.8 | V |

Note: * The minimum value is -3.0 V for pulse widths under 30 ns.

LC35256FM, FT-55U/70U

DC Electrical Characteristics at Ta = -40 to +85°C, VCC = 4.5 to 5.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------------|--|---|---|------------|-------------------|------|
| | | | min | typ* | max | |
| Input leakage current | I _{LI} | V _{IN} = 0 to V _{CC} | -1.0 | | +1.0 | μA |
| Output leakage current | I _{LO} | V _{CE} = V _{IH} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , V _{IO} = 0 to V _{CC} | -1.0 | | +1.0 | μA |
| Output high-level voltage | V _{OH} | I _{OH} = -1.0 mA | 2.4 | | | V |
| Output low-level voltage | V _{OL} | I _{OL} = 2.0 mA | | | 0.4 | V |
| Operating current drain | TTL inputs | I _{CCA2} | V _{CE} = V _{IL} , I _{IO} = 0 mA, V _{IN} = V _{IH} or V _{IL} | | 5.0 | mA |
| | | I _{CCA3} | V _{CE} = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{IO} = 0 mA, Duty 100 % | Min. cycle | LC35256FM, FT-55U | |
| | | | | | LC35256FM, FT-70U | |
| | | | | 1 μs cycle | | |
| Standby mode current drain | V _{CC} - 0.2 V/ 0.2 V inputs | I _{CCS1} | V _{CE} ≥ V _{CC} - 0.2 V, V _{IN} = 0 to V _{CC} | Ta ≤ 25°C | 0.05 | μA |
| | | | | Ta ≤ 60°C | | |
| | | | | Ta ≤ 70°C | | |
| | | | | Ta ≤ 85°C | | |
| | TTL inputs | I _{CCS2} | V _{CE} = V _{IH} , V _{IN} = 0 to V _{CC} | | | 1.0 |

Note: * Reference values when V_{CC} = 5 V and Ta = 25°C.

AC Electrical Characteristics at Ta = -40 to +85°C, VCC = 4.5 to 5.5 V

AC test conditions

Input pulse voltage levels: V_{IH} = 2.4 V, V_{IL} = 0.6 V

Input rise and fall times: 5 ns

Input and output timing levels: 1.5 V

Output load: 30 pF + 1 TTL gate (including the jig capacitance)

Read Cycle

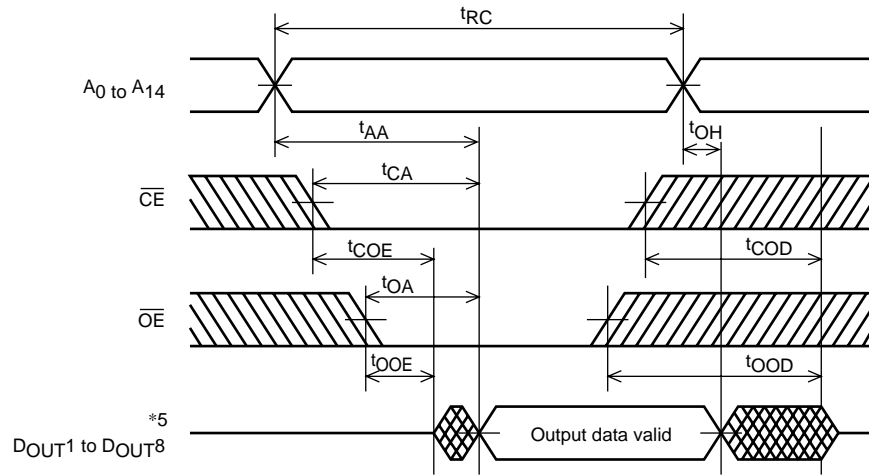
| Parameter | Symbol | LC35256FM, FT | | | | Unit |
|--|------------------|---------------|-----|------|-----|------|
| | | -55U | | -70U | | |
| | | min | max | min | max | |
| Read cycle time | t _{RC} | 55 | | 70 | | ns |
| Address access time | t _{AA} | | 55 | | 70 | ns |
| $\overline{\text{CE}}$ access time | t _{CA} | | 55 | | 70 | ns |
| $\overline{\text{OE}}$ access time | t _{OA} | | 30 | | 35 | ns |
| Output hold time | t _{OH} | 10 | | 10 | | ns |
| $\overline{\text{CE}}$ output enable time | t _{COE} | 5 | | 10 | | ns |
| $\overline{\text{OE}}$ output enable time | t _{OOE} | 5 | | 5 | | ns |
| $\overline{\text{CE}}$ output disable time | t _{COD} | | 20 | | 30 | ns |
| $\overline{\text{OE}}$ output disable time | t _{OOD} | | 20 | | 25 | ns |

Write Cycle

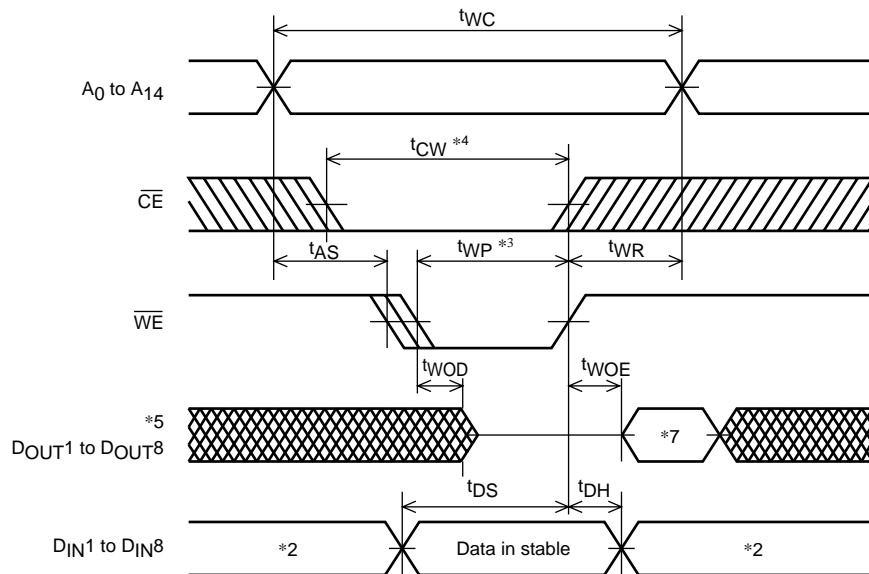
| Parameter | Symbol | LC35256FM, FT | | | | Unit |
|--|------------------|---------------|-----|------|-----|------|
| | | -55U | | -70U | | |
| | | min | max | min | max | |
| Write cycle time | t _{WC} | 55 | | 70 | | ns |
| Address setup time | t _{AS} | 0 | | 0 | | ns |
| Write pulse width | t _{WP} | 40 | | 50 | | ns |
| $\overline{\text{CE}}$ setup time | t _{CW} | 50 | | 60 | | ns |
| Write recovery time | t _{WR} | 0 | | 0 | | ns |
| $\overline{\text{CE}}$ write recovery time | t _{WR1} | 0 | | 0 | | ns |
| Data setup time | t _{DS} | 25 | | 30 | | ns |
| Data hold time | t _{DH} | 0 | | 0 | | ns |
| $\overline{\text{CE}}$ data hold time | t _{DH1} | 0 | | 0 | | ns |
| $\overline{\text{WE}}$ output enable time | t _{WOE} | 5 | | 5 | | ns |
| $\overline{\text{WE}}$ output disable time | t _{WOD} | | 20 | | 30 | ns |

Timing Charts

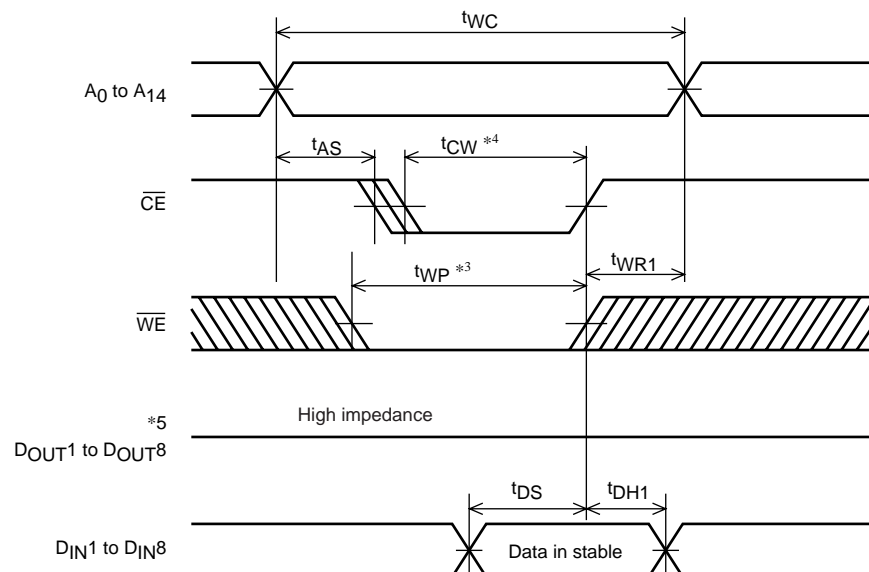
[Read cycle] *1



[Write cycle 1] (\overline{WE} write) *6



[Write cycle 2] (\overline{CE} write) *6



Notes: 1. \overline{WE} must be held at the high level during the read cycle.

2. Do not apply reverse phase signals to the D_{OUT} pins when those pins are in the output state.

3. The time t_{WP} is the period when both \overline{CE} and \overline{WE} are low. It is defined as the time from the fall of \overline{WE} to the rise of \overline{CE} or \overline{WE} , whichever occurs first.

4. The time t_{CW} is the period when both \overline{CE} and \overline{WE} are low. It is defined as the time from the fall of \overline{CE} to the rise of \overline{CE} or \overline{WE} , whichever occurs first.

5. The D_{OUT} pins will be in the high-impedance state if any one of the following hold: \overline{OE} is at the high level, \overline{CE} is at the high level, or \overline{WE} is at the low level.

6. The \overline{OE} pin must be either held high or held low during the write cycle.

7. D_{OUT} has the same phase as the write data during this write cycle.

Circuit Design Notes

When designing application circuits, always take the following into consideration and design the circuits so that the absolute maximum ratings are never exceeded.

- Supply voltage fluctuations
- Sample-to-sample variations in the electrical characteristics of the electronic components used, including semiconductor devices, resistors, and capacitors.
- Ambient temperature
- Variations in the input and clock signals
- The application of abnormal pulses

Furthermore, be sure to operate this device within the stipulated ranges of all parameters for which an allowable operating range is specified.

When CMOS IC input pins are left in the open state, through currents may occur in internal circuits to which intermediate voltage levels are applied, and this can result in incorrect circuit operation. Be sure to handle all unused input pins as specified in the device documentation.

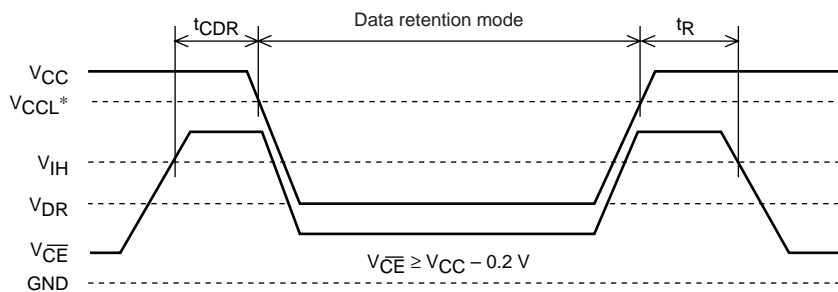
Data Retention Conditions at $T_a = -40$ to $+85^\circ\text{C}$

| Parameter | Symbol | Conditions | min | typ* | max | Unit |
|-------------------------------|------------|--|-----------------------------|------|-----|---------------|
| Data retention supply voltage | V_{DR} | $V_{CE} \geq V_{CC} - 0.2\text{ V}$ | 2.0 | | 5.5 | V |
| Data retention supply current | I_{CCDR} | $V_{CC} = 3.0\text{ V}$ $V_{CE} \geq V_{CC} - 0.2\text{ V}$ | $T_a \leq 25^\circ\text{C}$ | 0.02 | | μA |
| | | | $T_a \leq 60^\circ\text{C}$ | | 1.0 | |
| | | | $T_a \leq 70^\circ\text{C}$ | | 2.0 | |
| | | | $T_a \leq 85^\circ\text{C}$ | | 3.5 | |
| Chip enable setup time | t_{CDR} | | 0 | | | ns |
| Chip enable hold time | t_R | | t_{RC}^{**} | | | ns |

Note: * Reference values for $V_{CC} = 3\text{ V}$, $T_a = 25^\circ\text{C}$.

** t_{RC} : Read cycle time

Data Retention Waveforms



Note: * V_{CCL} 5 V operation: 4.5 V

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