



LC3564RM,RT-10LV/12LV/15LV

64K (8192 words × 8 bits) SRAM

Overview

The LC3564RM,RT are 8192-word × 8bit, asynchronous, silicon gate, low-voltage CMOS SRAM LSIs. They operate from a 2.0 to 3.6V supply, making them ideal for hand-held, battery-operated equipment.

They are fully CMOS devices employing 2-layer A1 wiring to realize high-speed access, low operating current consumption and very low standby current. They incorporate control signal inputs; \overline{OE} for high-speed memory access, and 2 chip enables $\overline{CE1}$ and $CE2$ for power-down and device selection.

They are ideal for systems requiring high speed, low power and battery backup or for easy memory expansion. The very low standby current means that backup can also be achieved using a capacitor.

Features

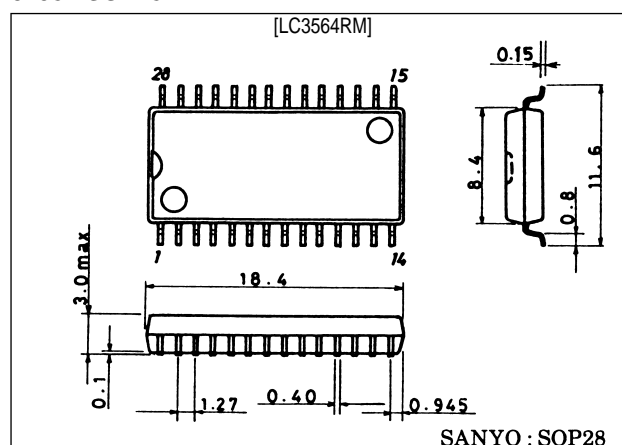
- Supply voltage range: 2.0 to 3.6V
 - 3V operation: 2.7 to 3.6V
 - Battery operation: 2.0 to 2.4V
- High-speed access time
 - 3V operation
 - LC3564RM,RT-10LV: 100ns (max)
 - LC3564RM,RT-12LV: 120ns (max)
 - LC3564RM,RT-15LV: 150ns (max)
 - Battery operation
 - LC3564RM,RT-10LV: 200ns (max)
 - LC3564RM,RT-12LV: 250ns (max)
 - LC3564RM,RT-15LV: 300ns (max)
- Very-low standby current
 - 3V operation
 - $T_a \leq 70^\circ\text{C}$: 1.0 μA
 - $T_a \leq 85^\circ\text{C}$: 3.0 μA
 - Battery operation
 - $T_a \leq 70^\circ\text{C}$: 0.85 μA
 - $T_a \leq 85^\circ\text{C}$: 2.5 μA
- Operating temperature range: -40 to $+85^\circ\text{C}$
- Data retention supply voltage: 2.0 to 3.6V
- Input/output levels: CMOS Compatible (0.8V_{cc}/0.2V_{cc})
- 3 control inputs (\overline{OE} , $\overline{CE1}$, $CE2$)

- Common-pin input/outputs, 3-state output
- Clock not needed (fully-static RAM)
- Package
 - SOP 28-pin (450mil) plastic package: LC3564RM series
 - TSOP 28-pin (8 × 13.4mm) plastic package: LC3564RT series

Package Dimensions

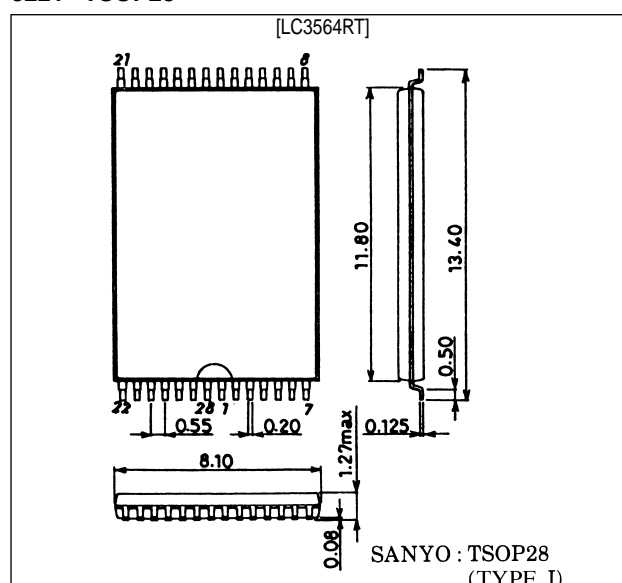
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3158 - SOP28



unit: mm

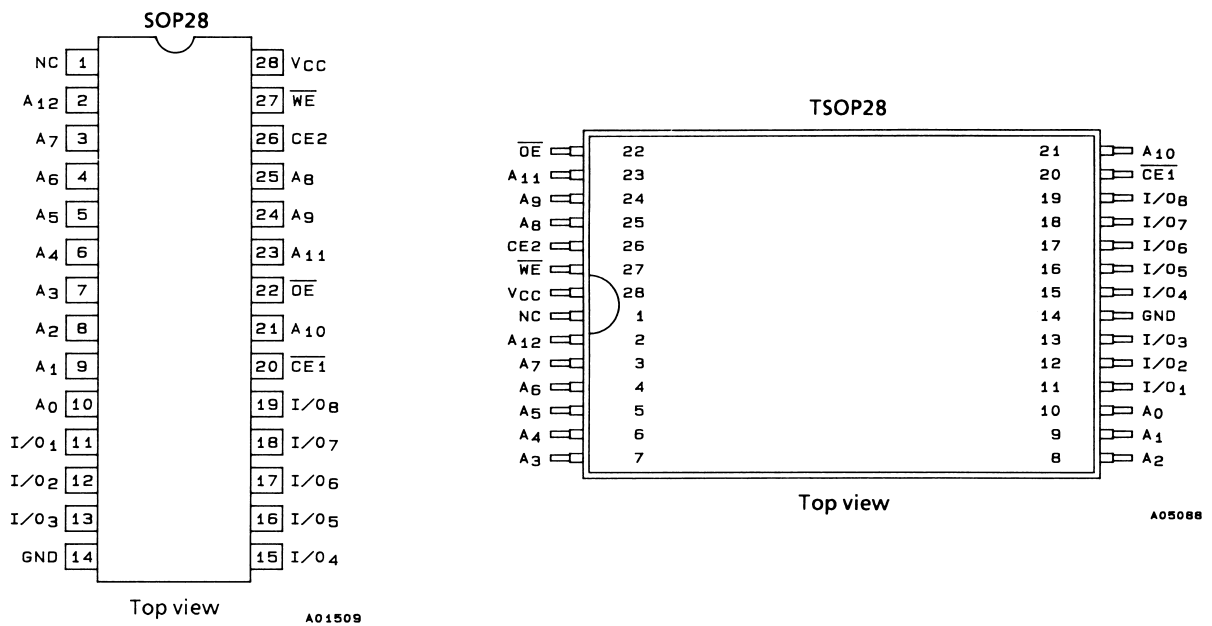
3221 - TSOP28



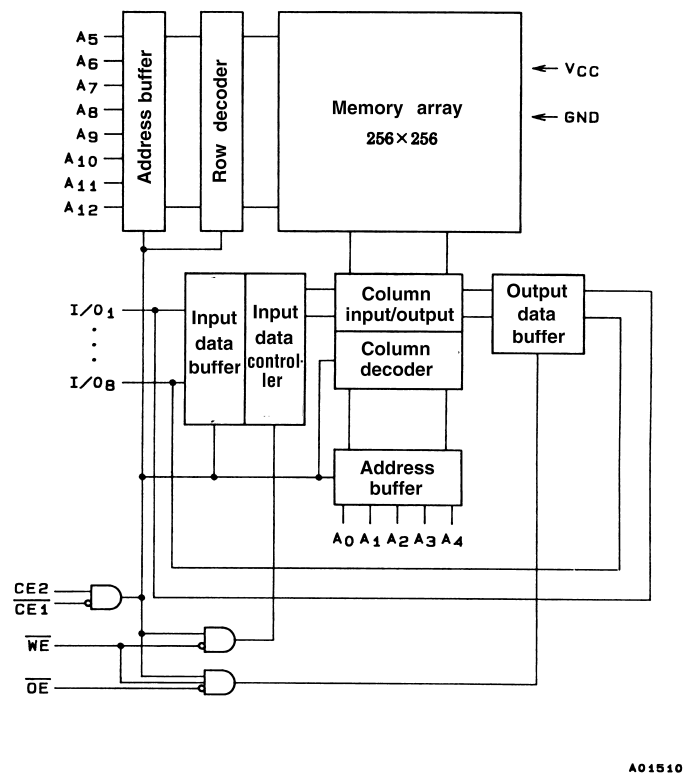
SANYO Electric Co., Ltd. Semiconductor Business Headquarters

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Pin Assignment



Block Diagram



Pin Functions

| Number | Name | Function |
|-----------------------|------------------------|--------------------------|
| 1 | NC | No connection |
| 2 to 10, 21, 23 to 25 | A0 to A12 | Address inputs |
| 27 | \overline{WE} | Read/write control input |
| 22 | \overline{OE} | Output enable input |
| 20, 26 | $\overline{CE1}$, CE2 | Chip enable inputs |
| 11 to 13, 15 to 19 | I/O1 to I/O8 | Data input/outputs |
| 28, 14 | V _{CC} , GND | Supply and ground pins |

Truth Table

| Mode | $\overline{CE1}$ | CE2 | \overline{OE} | $\overline{WE1}$ | I/O | Supply current |
|----------------|------------------|-----|-----------------|------------------|----------------|------------------|
| Read cycle | L | H | L | H | Data output | I _{CCA} |
| Write cycle | L | H | X | L | Data input | I _{CCA} |
| Output disable | L | H | H | H | High impedance | I _{CCA} |
| No selection | H | X | X | X | High impedance | I _{CCS} |
| | X | L | X | X | High impedance | I _{CCS} |

Note: X = H or L

Specifications

Absolute Maximum Ratings at T_a = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|------------|-------------------------------|------|
| Maximum supply voltage | V _{CC max} | | 4.6 | V |
| Input voltage range | V _{IN} | | −0.3 to V _{CC} + 0.3 | V |
| Input/output voltage range | V _{I/O} | | −0.3 to V _{CC} + 0.3 | V |
| Operating temperature range | T _{opr} | | −40 to +85 | °C |
| Storage temperature range | T _{stg} | | −55 to +125 | °C |

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended operating conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Inout/Output Capacitance at T_a = 25°C, f = 1 MHz

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|------------------------------|------------------|-----------------------|---------|------|------|------|
| | | | min. | typ. | max. | |
| Input/output pin capacitance | C _{I/O} | V _{I/O} = 0V | - | 6 | 10 | pF |
| Input pin capacitance | C _I | V _I = 0V | - | 6 | 10 | pF |

Note: Measured samples only.

3V Operation

DC Recommended Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6V

| Parameter | Symbol | Ratings | | | Unit |
|----------------|----------|-------------|------|----------------|------|
| | | min. | typ. | max. | |
| Supply voltage | V_{CC} | 2.7 | 3.0 | 3.6 | V |
| Input voltage | V_{IH} | $0.8V_{CC}$ | - | $V_{CC} + 0.3$ | V |
| | V_{IL} | -0.3^* | - | $0.2V_{CC}$ | V |

* When pulsewidth is less than 30 ns, the minimum value is -2.0V .

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6V

| Parameter | | Symbol | Conditions | | Ratings | | | Unit |
|---------------------------|-----------------------------------|-------------------|---|--|-----------------------|-------|------|------|
| | | | | | min. | typ.* | max. | |
| Input leakage current | | I _{LI} | V _{IN} = 0V to V _{CC} | | −1.0 | - | +1.0 | μA |
| I/O leakage current | | I _{LO} | V _{CE1} = V _{IH} or V _{CE2} = V _{IL} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , V _{I/O} = 0V to V _{CC} | | −1.0 | - | +1.0 | μA |
| Output high level voltage | | V _{OH} | I _{OH} = −2.0mA | | V _{CC} − 0.4 | - | - | V |
| Output low level voltage | | V _{OL} | I _{OL} = 2.0mA | | - | - | 0.4 | V |
| Operating supply current | V _{CC} − 0.2V/0.2V input | I _{CCA1} | V _{CE1} ≤ 0.2V, V _{CE2} ≥ V _{CC} − 0.2V, I _{I/O} = 0mA, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} − 0.2V | Ta ≤ 70°C | - | 0.01 | 1.0 | μA |
| | | | | Ta ≤ 85°C | - | - | 3.0 | μA |
| | CMOS input | I _{CCA2} | V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0mA, V _{IN} = V _{IH} or V _{IL} | | - | - | 4 | mA |
| | | | I _{CCA3} | V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0mA, duty = 100% | min. cycle | - | - | 25 |
| | | 200 ns cycle | | | - | - | 15 | mA |
| | | 1 μs cycle | | | - | - | 10 | mA |
| Standby supply current | V _{CC} − 0.2V/0.2V input | I _{CCS1} | V _{CE2} ≤ 0.2V or {V _{CE1} ≥ V _{CC} − 0.2V, V _{CE2} ≥ V _{CC} − 0.2V} | Ta ≤ 70°C | - | 0.01 | 1.0 | μA |
| | | | | Ta ≤ 85°C | - | - | 3.0 | μA |
| | CMOS input | I _{CCS2} | V _{CE2} = V _{IL} or V _{CE1} = V _{IH} , V _{IN} = 0V to V _{CC} | | - | - | 1 | mA |

* $V_{CC} = 3.0\text{V}$, $T_a = 25^\circ\text{C}$

AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6V

AC test conditions

Input pulse voltage level: $0.2V_{CC}$ to $0.8V_{CC}$

Input rise and fall times: 5 ns

Input/output timing level: $V_{CC}/2$

Output load: 30 pF (including jig capacitance)

Read Cycle

| Parameter | Symbol | LC3564RM,RT | | | | | | Unit |
|-------------------------|-------------------|-------------|------|-------|------|-------|------|------|
| | | -10LV | | -12LV | | -15LV | | |
| | | min. | max. | min. | max. | min. | max. | |
| Read cycle time | t _{RC} | 100 | - | 120 | - | 150 | - | ns |
| Address access time | t _{AA} | - | 100 | - | 120 | - | 150 | ns |
| CE1 access time | t _{CA1} | - | 100 | - | 120 | - | 150 | ns |
| CE2 access time | t _{CA2} | - | 100 | - | 120 | - | 150 | ns |
| OE access time | t _{OA} | - | 50 | - | 60 | - | 75 | ns |
| Output hold time | t _{OH} | 10 | - | 10 | - | 10 | - | ns |
| CE1 output enable time | t _{COE1} | 10 | - | 10 | - | 10 | - | ns |
| CE2 output enable time | t _{COE2} | 10 | - | 10 | - | 10 | - | ns |
| OE output enable time | t _{OOE} | 5 | - | 5 | - | 5 | - | ns |
| CE1 output disable time | t _{COD1} | - | 35 | - | 40 | - | 50 | ns |
| CE2 output disable time | t _{COD2} | - | 35 | - | 40 | - | 50 | ns |
| OE output disable time | t _{OOD} | - | 25 | - | 30 | - | 40 | ns |

Write Cycle

| Parameter | Symbol | LC3564RM,RT | | | | | | Unit |
|--------------------------------------|------------------|-------------|------|-------|------|-------|------|------|
| | | -10LV | | -12LV | | -15LV | | |
| | | min. | max. | min. | max. | min. | max. | |
| Write cycle time | t _{WC} | 100 | - | 120 | - | 150 | - | ns |
| Address setup time | t _{AS} | 0 | - | 0 | - | 0 | - | ns |
| Write pulsewidth | t _{WP} | 60 | - | 70 | - | 80 | - | ns |
| $\overline{CE1}$ setup time | t _{CW1} | 70 | - | 80 | - | 90 | - | ns |
| CE2 setup time | t _{CW2} | 70 | - | 80 | - | 90 | - | ns |
| Write recovery time | t _{WR} | 0 | - | 0 | - | 0 | - | ns |
| $\overline{CE1}$ write recovery time | t _{WR1} | 0 | - | 0 | - | 0 | - | ns |
| CE2 write recovery time | t _{WR2} | 0 | - | 0 | - | 0 | - | ns |
| Data setup time | t _{DS} | 50 | - | 55 | - | 60 | - | ns |
| Data hold time | t _{DH} | 0 | - | 0 | - | 0 | - | ns |
| $\overline{CE1}$ data hold time | t _{DH1} | 0 | - | 0 | - | 0 | - | ns |
| CE2 data hold time | t _{DH2} | 0 | - | 0 | - | 0 | - | ns |
| WE output enable time | t _{WOE} | 5 | - | 5 | - | 5 | - | ns |
| WE output disable time | t _{WOD} | - | 35 | - | 40 | - | 45 | ns |

Battery Operation

DC Recommended Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.0$ to 2.4V

| Parameter | Symbol | Ratings | | | Unit |
|----------------|----------|-------------|------|----------------|------|
| | | min. | typ. | max. | |
| Supply voltage | V_{CC} | 2.0 | 2.2 | 2.4 | V |
| Input voltage | V_{IH} | $0.8V_{CC}$ | - | $V_{CC} + 0.3$ | V |
| | V_{IL} | -0.3 | - | $0.2V_{CC}$ | V |

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.0$ to 2.4V

| Parameter | | Symbol | Conditions | | Ratings | | | Unit |
|---------------------------|-----------------------------------|-------------------|--|------------|-----------------------|-------|------|------|
| | | | | | min. | typ.* | max. | |
| Input leakage current | | I _{LI} | V _{IN} = 0V to V _{CC} | | −1.0 | - | +1.0 | μA |
| I/O leakage current | | I _{LO} | V _{CE1} = V _{IH} or V _{CE2} = V _{IL} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , V _{IO} = 0V to V _{CC} | | −1.0 | - | +1.0 | μA |
| Output high level voltage | | V _{OH} | I _{OH} = −0.5mA | | V _{CC} − 0.2 | - | - | V |
| Output low level voltage | | V _{OL} | I _{OL} = 0.5mA | | - | - | 0.2 | V |
| Operating supply current | V _{CC} − 0.2V/0.2V input | I _{CCA1} | V _{CE1} ≤ 0.2V, V _{CE2} ≥ V _{CC} − 0.2V, I _{I/O} = 0mA, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} − 0.2V | Ta ≤ 70°C | - | 0.01 | 0.85 | μA |
| | | | | Ta ≤ 85°C | - | - | 2.5 | μA |
| | CMOS input | I _{CCA2} | V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0mA, V _{IN} = V _{IH} or V _{IL} | - | - | 2 | mA | |
| | | I _{CCA3} | V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0mA, duty = 100% | min. cycle | - | - | 10 | mA |
| | | | 1 μs cycle | - | - | 5 | mA | |
| Standby supply current | V _{CC} − 0.2V/0.2V input | I _{CCS1} | V _{CE2} ≤ 0.2V or {V _{CE1} ≥ V _{CC} − 0.2V, V _{CE2} ≥ V _{CC} − 0.2V} | Ta ≤ 70°C | - | 0.01 | 0.85 | μA |
| | | | Ta ≤ 85°C | - | - | 2.5 | μA | |
| | CMOS input | I _{CCS2} | V _{CE2} = V _{IL} or V _{CE1} = V _{IH} , V _{IN} = 0V to V _{CC} | - | - | 800 | mA | |

* $V_{CC} = 2.2\text{V}$, $T_a = 25^\circ\text{C}$

AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.0$ to 2.4V

AC test conditions

Input pulse voltage level: $0.2V_{CC}$ to $0.8V_{CC}$

Input rise and fall times: 10 ns

Input/output timing level: $V_{CC}/2$

Output load: 30 pF (including jig capacitance)

Read Cycle

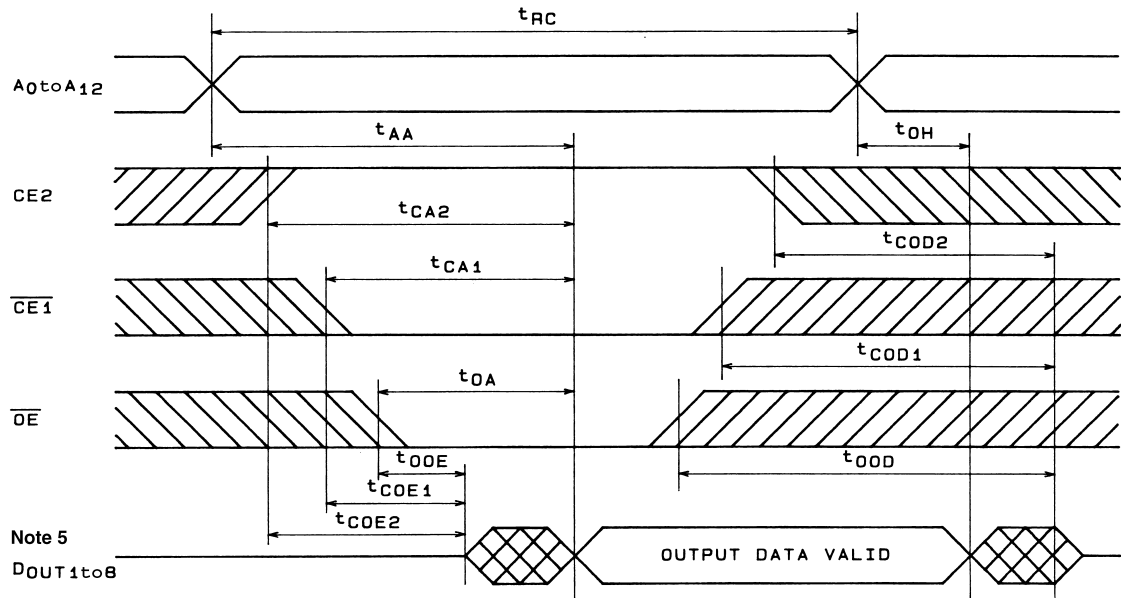
| Parameter | Symbol | LC3564RM,RT | | | | | | Unit |
|-------------------------|-------------------|-------------|------|-------|------|-------|------|------|
| | | -10LV | | -12LV | | -15LV | | |
| | | min. | max. | min. | max. | min. | max. | |
| Read cycle time | t _{RC} | 200 | - | 250 | - | 300 | - | ns |
| Address access time | t _{AA} | - | 200 | - | 250 | - | 300 | ns |
| CE1 access time | t _{CA1} | - | 200 | - | 250 | - | 300 | ns |
| CE2 access time | t _{CA2} | - | 200 | - | 250 | - | 300 | ns |
| OE access time | t _{OA} | - | 120 | - | 130 | - | 150 | ns |
| Output hold time | t _{OH} | 10 | - | 10 | - | 10 | - | ns |
| CE1 output enable time | t _{COE1} | 10 | - | 10 | - | 10 | - | ns |
| CE2 output enable time | t _{COE2} | 10 | - | 10 | - | 10 | - | ns |
| OE output enable time | t _{OOE} | 5 | - | 5 | - | 5 | - | ns |
| CE1 output disable time | t _{COD1} | - | 70 | - | 80 | - | 100 | ns |
| CE2 output disable time | t _{COD2} | - | 70 | - | 80 | - | 100 | ns |
| OE output disable time | t _{OOD} | - | 50 | - | 60 | - | 80 | ns |

Write Cycle

| Parameter | Symbol | LC3564RM,RT | | | | | | Unit |
|--------------------------------------|------------------|-------------|------|-------|------|-------|------|------|
| | | -10LV | | -12LV | | -15LV | | |
| | | min. | max. | min. | max. | min. | max. | |
| Write cycle time | t _{WC} | 200 | - | 250 | - | 300 | - | ns |
| Address setup time | t _{AS} | 0 | - | 0 | - | 0 | - | ns |
| Write pulsewidth | t _{WP} | 120 | - | 140 | - | 160 | - | ns |
| $\overline{CE1}$ setup time | t _{CW1} | 140 | - | 160 | - | 180 | - | ns |
| CE2 setup time | t _{CW2} | 140 | - | 160 | - | 180 | - | ns |
| Write recovery time | t _{WR} | 0 | - | 0 | - | 0 | - | ns |
| $\overline{CE1}$ write recovery time | t _{WR1} | 0 | - | 0 | - | 0 | - | ns |
| CE2 write recovery time | t _{WR2} | 0 | - | 0 | - | 0 | - | ns |
| Data setup time | t _{DS} | 120 | - | 130 | - | 150 | - | ns |
| Data hold time | t _{DH} | 0 | - | 0 | - | 0 | - | ns |
| $\overline{CE1}$ data hold time | t _{DH1} | 0 | - | 0 | - | 0 | - | ns |
| CE2 data hold time | t _{DH2} | 0 | - | 0 | - | 0 | - | ns |
| WE output enable time | t _{WOE} | 5 | - | 5 | - | 5 | - | ns |
| WE output disable time | t _{WOD} | - | 70 | - | 80 | - | 90 | ns |

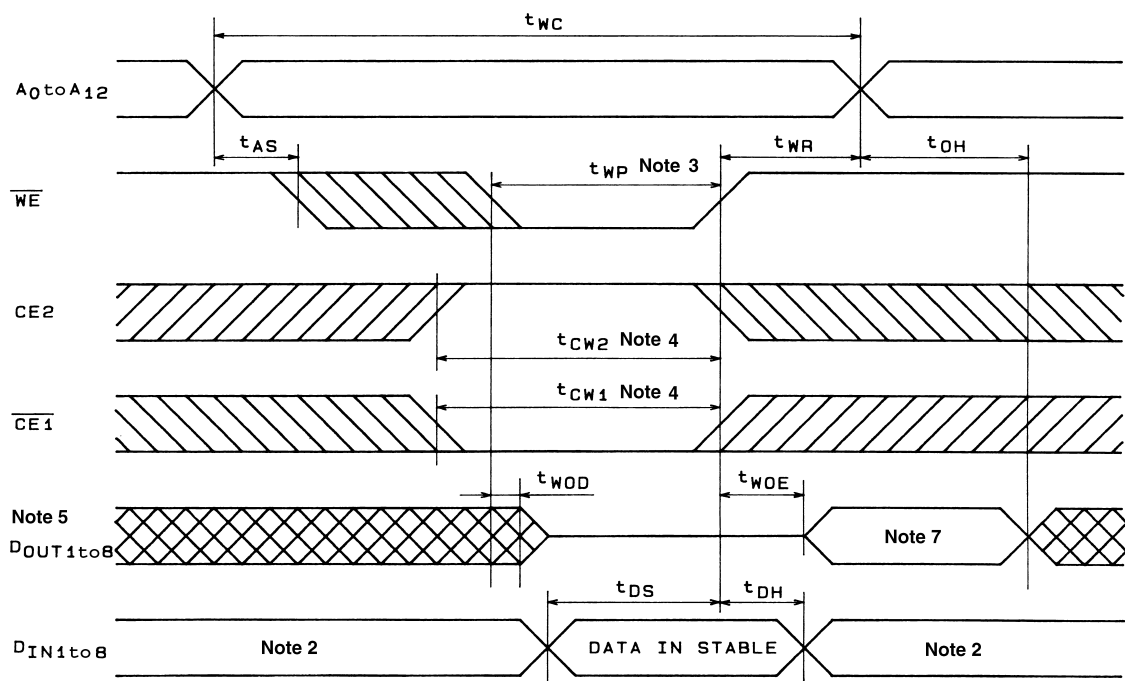
Timing Chart

Read Cycle: Note 1



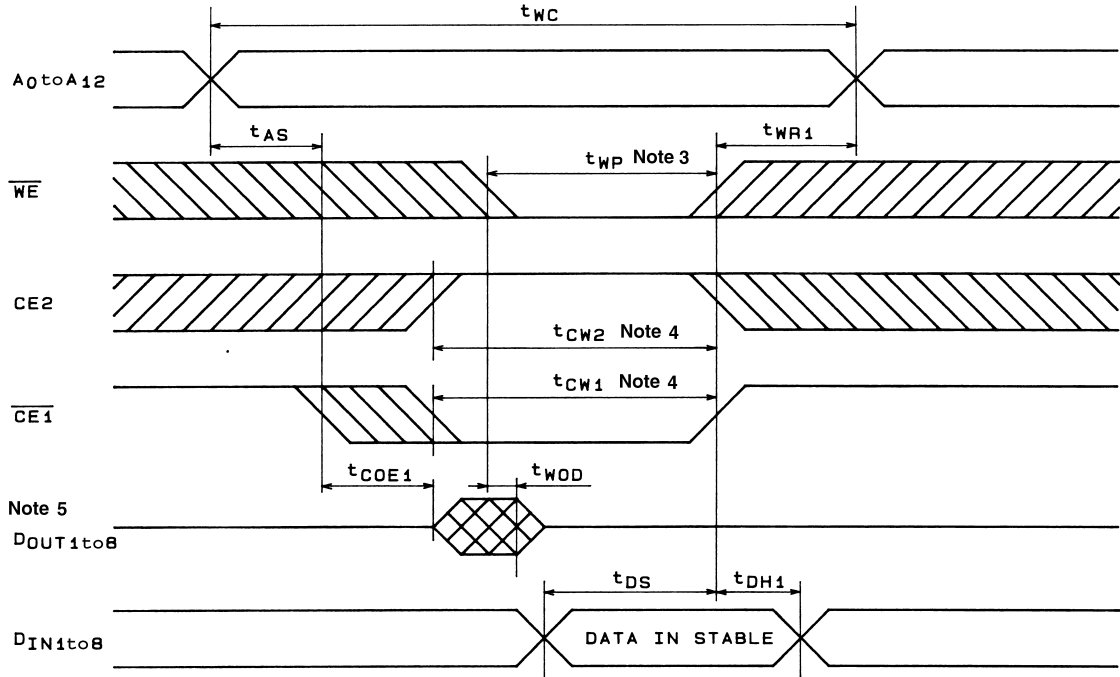
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Write Cycle 1 (\overline{WE} write): Note 6



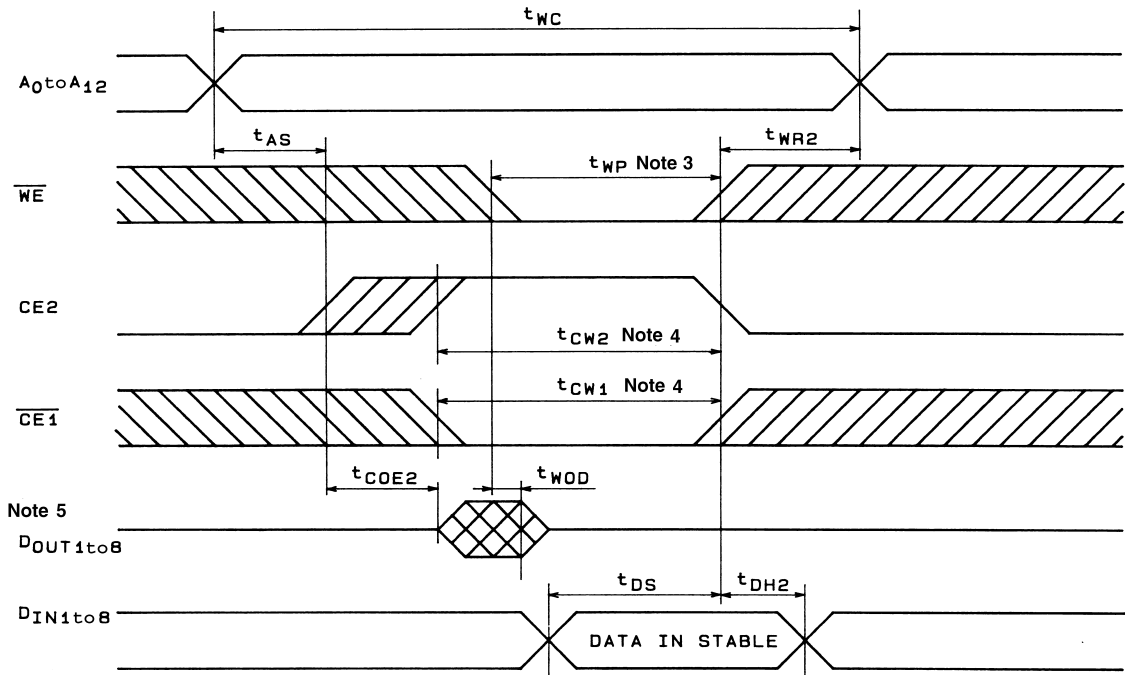
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Write Cycle 2 ($\overline{\text{CE1}}$ write): Note 6



A01513

Write Cycle 3 (CE2 write): Note 6



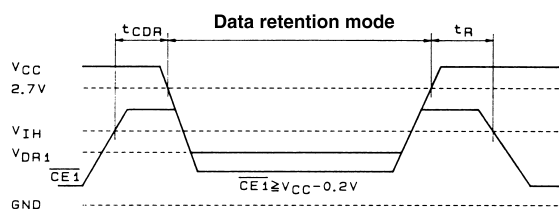
A01514

- Note: 1. We should be held high level during the read cycle
 2. Do not apply external signals that are out-of-phase with D_{OUT}
 3. t_{WP} is a period when $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are LOW and CE2 is HIGH. It is measured from when $\overline{\text{WE}}$ goes low level to when either $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ go HIGH or CE2 goes LOW, whichever occurs first.
 4. t_{CW1} and t_{CW2} are periods when $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are LOW and CE2 is HIGH. They are measured from when $\overline{\text{CE1}}$ goes LOW and CE2 goes HIGH, respectively, to when either $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ go HIGH or CE2 goes LOW, whichever occurs first.
 5. The outputs D_{OUT1} to D_{OUT8} are in a high-impedance state when $\overline{\text{OE}}$ is HIGH, $\overline{\text{CE1}}$ is HIGH, CE2 is LOW and $\overline{\text{WE}}$ is LOW.
 6. During the write cycle, $\overline{\text{OE}}$ is V_{IH} or V_{IL} .
 7. D_{OUT} has the same phase as the write data.

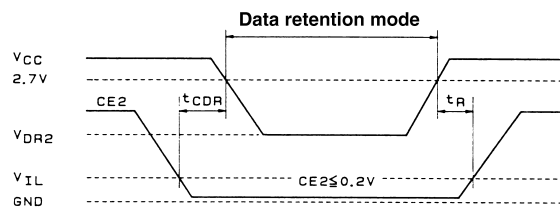
Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ **3V Operation**

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------|-----------|---|----------|------|------|------|
| | | | min. | typ. | max. | |
| Data retention supply voltage | V_{DR} | $V_{CE1} \geq V_{CC} - 0.2\text{V}$, $V_{CE2} \geq V_{CC} - 0.2\text{V}$ or $V_{CE2} \leq 0.2\text{V}$ | 2.0 | - | 3.6 | V |
| Chip enable setup time | t_{CDR} | | 0 | - | - | ns |
| Chip enable hold time | t_R | | t_{RC} | - | - | ns |

Note: t_{RC} is the read cycle time.

Data Retention Waveform 1 ($\overline{CE1}$ control)

A01515

Data Retention Waveform 2 ($CE2$ control)

A01516

Battery Operation

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------|----------|---|---------|------|------|------|
| | | | min. | typ. | max. | |
| Data retention supply voltage | V_{DR} | $V_{CE1} \geq V_{CC} - 0.2\text{V}$, $V_{CE2} \geq V_{CC} - 0.2\text{V}$ or $V_{CE2} \leq 0.2\text{V}$ | 2.0 | - | 3.6 | V |

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