



LC36256ALL, AMLL-70/85/10/12

256 K (32768 words × 8 bits) SRAM

Overview

The LC36256ALL, AMLL are fully asynchronous silicon gate CMOS static RAMs with a 32768 words × 8 bits configuration.

This series has CE chip enable pin for device select/nonselect control and an OE output enable pin for output control, and features high speed as well as low power dissipation.

Current dissipation is notably reduced during stand-by and data retention. For these reasons, this series is most suited for use in systems requiring high speed, low power consumption and long-term battery backup. Simple memory capacity expansion is also supported.

Features

- Access time

70 ns (max.) : LC36256ALL-70, LC36256AMLL-70
 85 ns (max.) : LC36256ALL-85, LC36256AMLL-85
 100 ns (max.) : LC36256ALL-10, LC36256AMLL-10
 120 ns (max.) : LC36256ALL-12, LC36256AMLL-12

- Low current dissipation

During standby

0.5 μ A (max.) / Ta = 25°C
 1 μ A (max.) / Ta = 0 to +40°C
 5 μ A (max.) / Ta = 0 to +70°C

During data retention

0.3 μ A (max.) / Ta = 25°C
 0.6 μ A (max.) / Ta = 0 to +40°C
 3 μ A (max.) / Ta = 0 to +70°C

During operation (DC)

10 mA (max.)

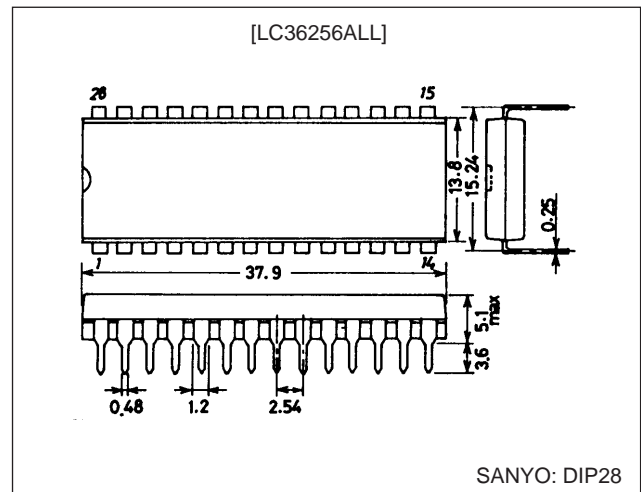
- Single 5 V power supply: 5 V \pm 10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages

DIP 28-pin (600 mil) plastic package : LC36256ALL
 SOP 28-pin (450 mil) plastic package : LC36256AMLL

Package Dimensions

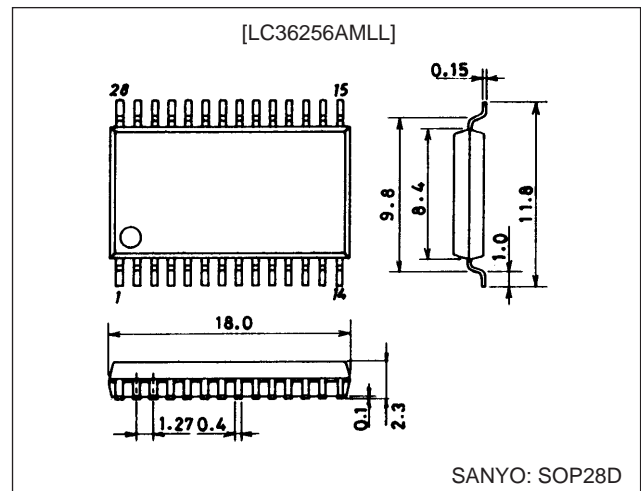
unit: mm

3012A-DIP28

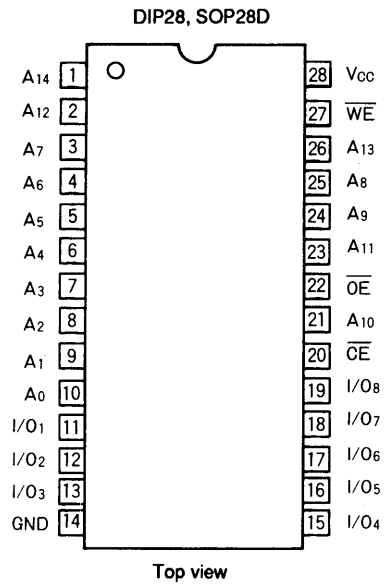


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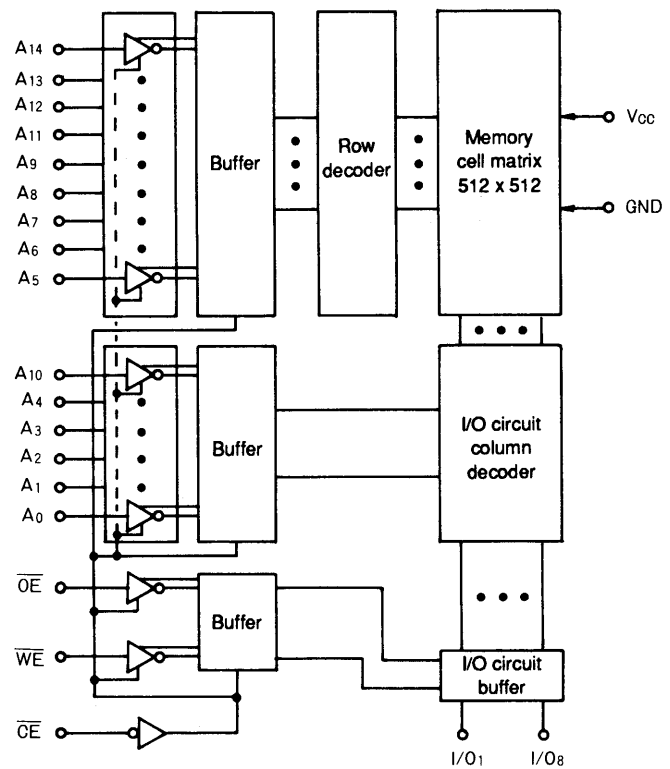
3187-SOP28D



Pin Assignment



Block Diagram



Pin Functions

A0 to A14	Address input
WE	Read/write control input
OE	Output enable input
CE	Chip enable input
I/O1 to I/O8	Data input/output
VCC, GND	Power supply pins

Functions

Mode	CE	OE	WE	I/O	Supply current
Read cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	X	L	Data input	I_{CCA}
Output disable	L	H	H	High impedance	I_{CCA}
Nonselect	H	X	X	High impedance	I_{CCS}

X : H or L

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VCC max		7.0	V
Input pin voltage	V _{IN}		-0.5* to VCC+0.5	V
I/O pin voltage	V _{I/O}		-0.5* to VCC+0.5	V
Allowable power dissipation	Pd max	LC36256ALL	1.0	W
		LC36256AMLL	0.7	W
Operating temperature range	Topr		0 to +70	°C
Storage temperature range	Tstg		-55 to +150	°C

* -3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	VCC	4.5	5.0	5.5	V
Input high level voltage	V _{IH}	2.2		VCC+0.3	V
Input low level voltage	V _{IL}	-0.3*		+0.8	V

* -3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ±10%

Parameter	Symbol	Conditions		min	typ*	max	Unit	
Input leakage current	I _{LI}	V _{IN} = 0 to V _{CC}		−0.5		+0.5	μA	
I/O leakage current	I _{LO}	V _{CE} = V _{IH} or V _{OE} = V _{IH} , V _{I/O} = 0 to V _{CC}		−0.5		+0.5	μA	
Output high level voltage	V _{OH}	I _{OH} = −1.0mA		2.4			V	
Output low level voltage	V _{OL}	I _{OL} = 2.1mA				0.4	V	
Operating supply current (DC)	I _{CCA1}	V _{CE} ≤ 0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} −0.2V			1	5	mA	
	I _{CCA2}	V _{CE} = V _{IL} , I _{I/O} =0mA			3	10	mA	
Average operating supply current	I _{CCA3}	min cycle Duty = 100% I _{I/O} = 0mA	Access time	70ns		30	50	mA
				85ns		25	50	
				100ns		23	50	
				120ns		20	50	
Standby supply current	I _{CCS1}	V _{CE} ≥ V _{CC} -0.2V		0 to +70°C			5	μA
				0 to +40°C			1	
				25°C		0.2	0.5	
	I _{CCS2}	V _{CE} = V _{IH}				0.4	2	mA

* Reference values at VCC = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	C _{I/O}	V _{I/O} = 0V			8	pF
Input capacitance	C _{IN}	V _{IN} = 0V			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ±10%

AC testing conditions

Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + C _L = 100 pF (85 ns/100 ns/120 ns) 1 TTL gate + C _L = 30 pF (70 ns) (including scope and jig capacitance)

Read Cycle

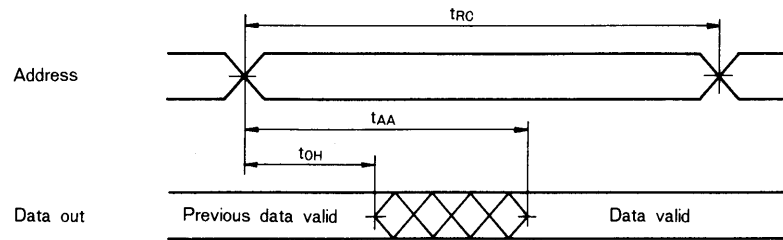
Parameter	Symbol	LC36256ALL, AMLL								Unit
		-70		-85		-10		-12		
		min	max	min	max	min	max	min	max	
Read cycle time	t _{RC}	70		85		100		120		ns
Address access time	t _{AA}		70		85		100		120	ns
CE access time	t _{CA}		70		85		100		120	ns
OE access time	t _{OA}		35		45		50		60	ns
Output hold time	t _{OH}	20		20		20		20		ns
CE output enable time	t _{COE}	10		10		10		10		ns
OE output enable time	t _{OOE}	5		5		5		5		ns
OE output disable time	t _{COD}	0	30	0	30	0	30	0	30	ns
OE output disable time	t _{OOD}	0	30	0	30	0	30	0	30	ns

Write Cycle

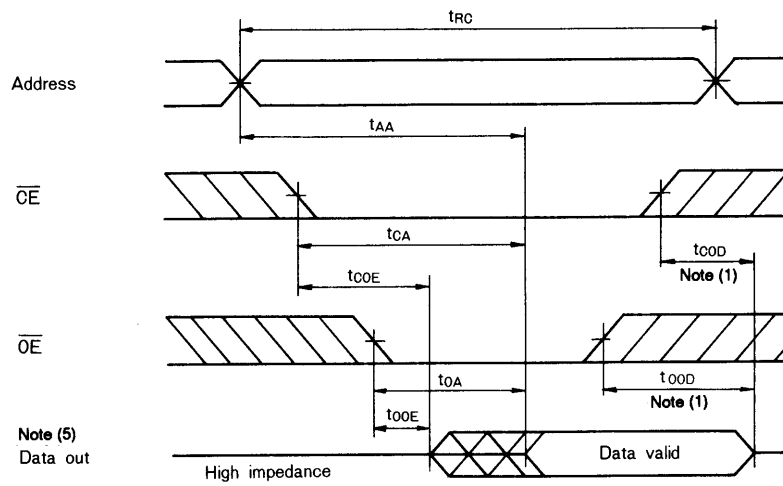
Parameter		LC36256ALL, AMLL								Unit
		-70		-85		-10		-12		
		min	max	min	max	min	max	min	max	
Write cycle time	t _{WC}	70		85		100		120		ns
Address valid to end of write	t _{AW}	65		75		80		100		ns
Address setup time	t _{AS}	0		0		0		0		ns
Write pulse width	t _{WP}	50		50		60		70		ns
CE setup time	t _{CW}	65		75		80		100		ns
Write recovery time (WE)	t _{WR}	0		0		0		0		ns
Write recovery time (CE)	t _{WR} ¹	0		0		0		0		ns
Data setup time	t _{DS}	30		30		35		40		ns
Data hold time	t _{DH}	0		0		0		0		ns
WE output enable time	t _{WOE}	10		10		10		10		ns
WE output disable time	t _{WOD}	0	25	0	25	0	25	0	25	ns

Timing Chart

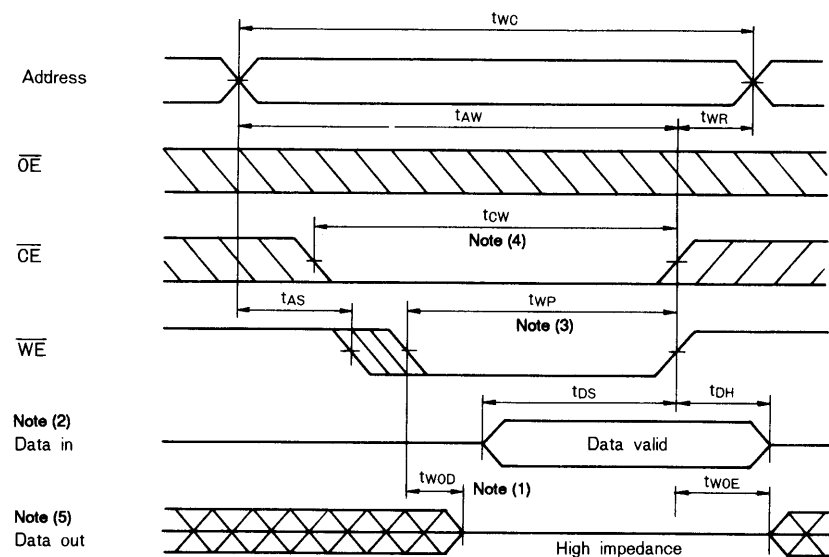
- Read Cycle (1): $CE = OE = V_{IL}$, $WE = V_{IH}$



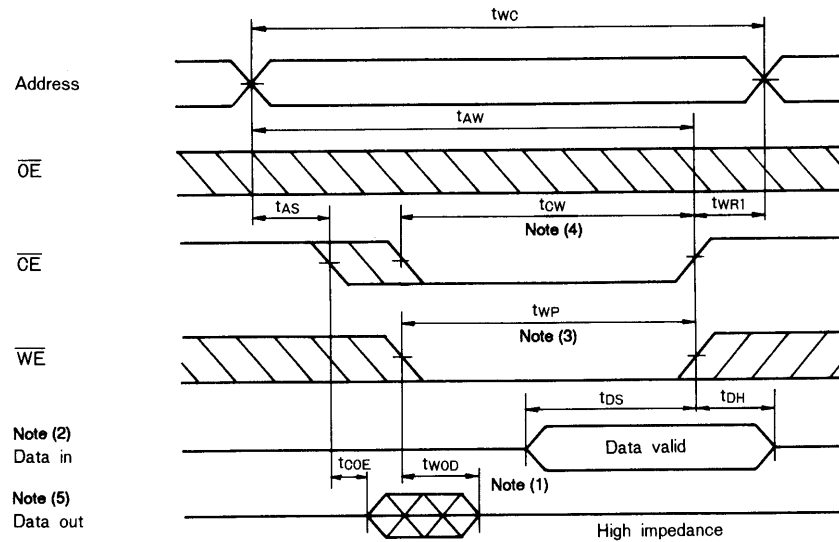
- Read Cycle (2): $WE = V_{IH}$



- Write Cycle (1): WE Control Note (6)



• Write Cycle (2): CE Control Note (6)



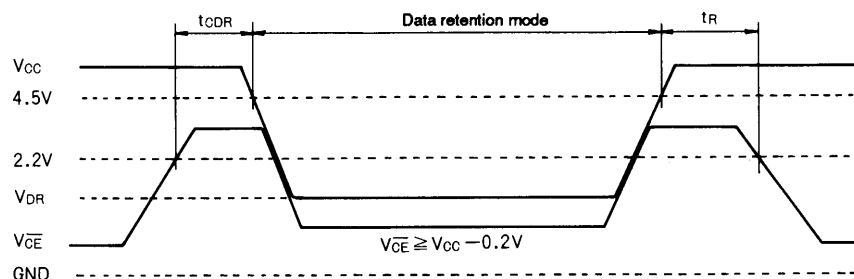
- Notes
- (1) t_{COD} , t_{OOD} , and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
 - (2) An external antiphase signal must not be applied when DOUT is in the output state.
 - (3) t_{WP} is the time interval that CE and WE are low-level and is defined as the interval from the falling of \overline{WE} to the rising of CE or WE whichever is earlier.
 - (4) t_{CW} is the time interval that CE and WE are low-level and is defined as the time from the falling of \overline{CE} to the rising of CE or WE whichever is earlier.
 - (5) DOUT goes to the high-impedance state when either OE is high-level, CE is high-level, or WE is low-level.
 - (6) When OE is high-level during the write cycle, DOUT goes to the high-impedance state.

Data Retention Characteristics at $T_a = 0$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ*	max	Unit
Data retention supply voltage	VDR	$V_{CE} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data retention supply current	ICCDR1	$V_{CC} = 3.0V$, $V_{CE} \geq 2.8V$	0 to $+70^\circ\text{C}$		3	μA
			0 to $+40^\circ\text{C}$		0.6	
			25°C	0.1	0.3	
	ICCDR2	$V_{CC} = 2.0$ to $5.5V$, $V_{CE} \geq V_{CC} - 0.2V$		0.2	5	μA
CE setup time	t_{CDR}		0			ns
CE hold time	t_R		t_{RC}^{**}			ns

* Reference values at $V_{CC} = 5V$, $T_a = 25^\circ\text{C}$ ** t_{RC} = Read Cycle time

Data Retention Waveform



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