

**SANYO**

No. ※4819

**LC36256ALL, AMLL-70W/85W/10W/12W****256 K (32768 words × 8 bits) SRAM****Preliminary****Overview**

The LC36256ALL, AMLL-70W/85W/10W/12W are fully asynchronous silicon gate CMOS static RAMs with an 32,768 words × 8 bits.

This series has  $\overline{CE}$  chip enable pin for device select/nonselect control and an  $\overline{OE}$  output enable pin for output control, and features high speed, low power dissipation, and wide temperature range.

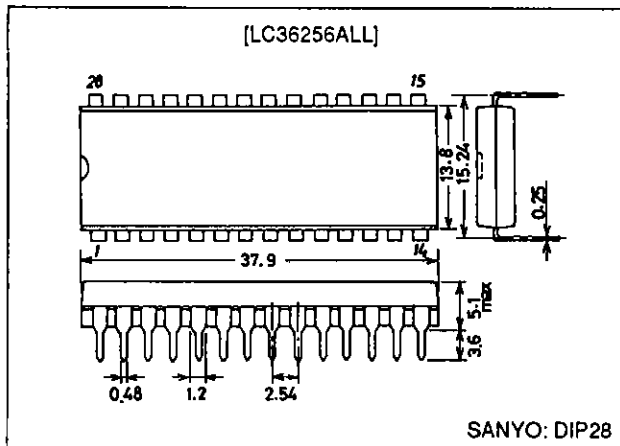
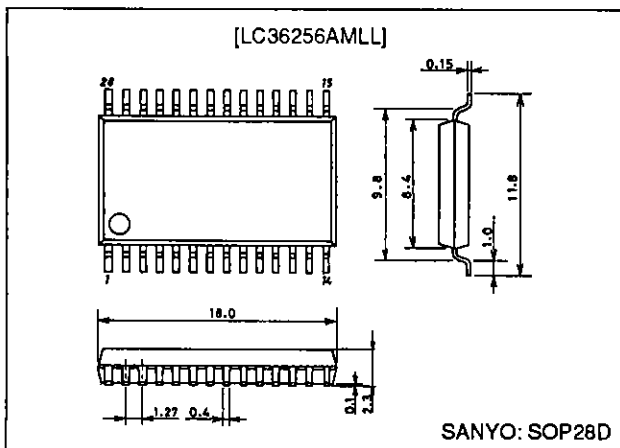
Current dissipation is notably reduced during standby and data retention. For these reasons, this series is most suited for use in systems requiring high speed, low power dissipation, and long-term battery backup. Simple memory capacity expansion is also supported.

**Features**

- Access time
  - 70 ns (max.) : LC36256ALL-70W,  
LC36256AMLL-70W
  - 85 ns (max.) : LC36256ALL-85W,  
LC36256AMLL-85W
  - 100 ns (max.) : LC36256ALL-10W,  
LC36256AMLL-10W
  - 120 ns (max.) : LC36256ALL-12W,  
LC36256AMLL-12W
- Low current dissipation
  - During standby
    - 0.5  $\mu$ A (max.) / Ta = 25°C
    - 1  $\mu$ A (max.) / Ta = -10 to +40°C
    - 5  $\mu$ A (max.) / Ta = -10 to +70°C
  - During data retention
    - 0.3  $\mu$ A (max.) / Ta = 25°C
    - 0.6  $\mu$ A (max.) / Ta = -10 to +40°C
    - 3  $\mu$ A (max.) / Ta = -10 to +70°C
  - During operation (DC)
    - 10 mA (max.)
- Single 5 V power supply: 5 V  $\pm$  10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages
  - DIP 28-pin plastic package (600 mil) : LC36256ALL
  - SOP 28D-pin plastic package (450 mil): LC36256AMLL

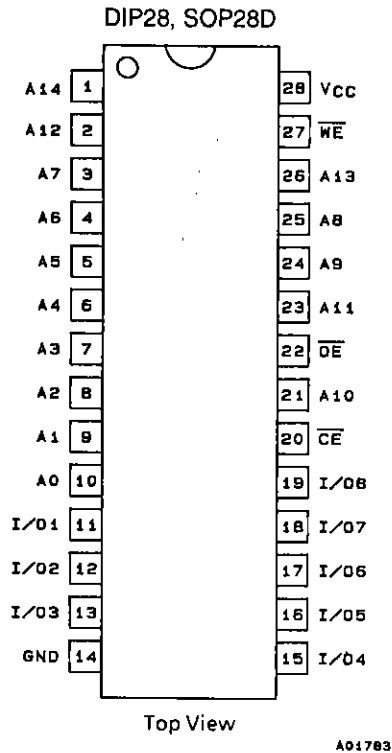
**Package Dimensions**

unit: mm

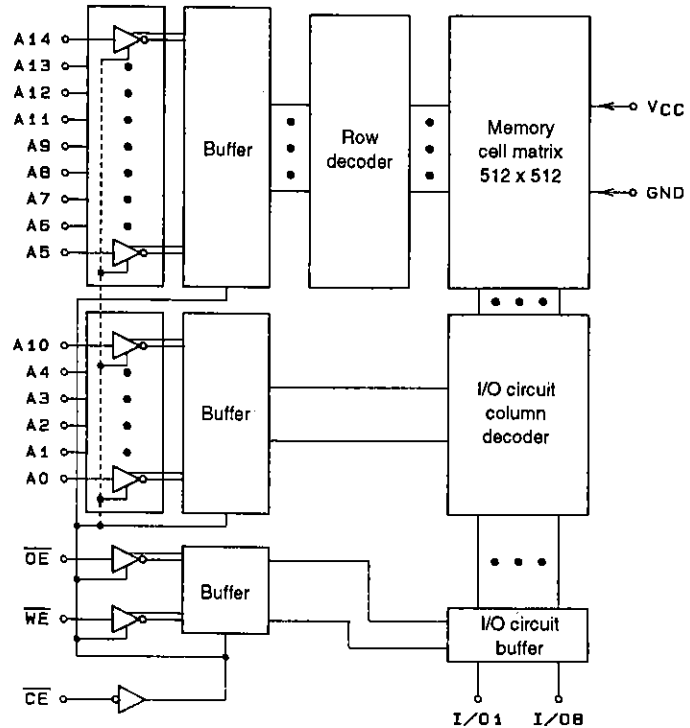
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## Pin Assignment



## Block Diagram



## Pin Functions

A <sub>0</sub> to A <sub>14</sub>	Address input
WE	Read/write control input
OE	Output enable input
CE	Chip enable input
I/O <sub>1</sub> to I/O <sub>8</sub>	Data input/output
V <sub>CC</sub> , GND	Power supply pins

## Functions Logic

Mode	CE	OE	WE	I/O	Supply current
Read cycle	L	L	H	Data output	I <sub>CCA</sub>
Write cycle	L	X	L	Data input	I <sub>CCA</sub>
Output disable	L	H	H	High impedance	I <sub>CCA</sub>
Nonselect	H	X	X	High impedance	I <sub>CCS</sub>

X: H or L

## Specifications

### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		7.0	V
Input pin voltage	$V_{IN}$		$-0.5^*$ to $V_{CC} + 0.5$	V
I/O pin voltage	$V_{IO}$		$-0.5^*$ to $V_{CC} + 0.5$	V
Allowable power dissipation	$P_d\text{ max}$	LC36256ALL	1.0	W
		LC36256AMLL	0.7	W
Operating temperature range	$T_{opr}$		$-10$ to $+70$	$^\circ\text{C}$
Storage temperature range	$T_{stg}$		$-55$ to $+150$	$^\circ\text{C}$

\*  $-3.0\text{ V}$  when pulse width is less than 50 ns

### DC Recommended Operating Ranges at $T_a = -10$ to $+70^\circ\text{C}$

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input high level voltage	$V_{IH}$	2.2		$V_{CC} + 0.3$	V
Input low level voltage	$V_{IL}$	$-0.3^*$		+0.8	V

\*  $-3.0\text{ V}$  when pulse width is less than 50 ns

### DC Electrical Characteristics at $T_a = -10$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Conditions			min	typ*	max	Unit
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$			-0.5		+0.5	$\mu A$
I/O leakage current	$I_{LO}$	$V_{CE} = V_{IH}$ or $V_{OE} = V_{IH}$ , $V_{I/O} = 0$ to $V_{CC}$			-0.5		+0.5	$\mu A$
Output high level voltage	$V_{OH}$	$I_{OH} = -1.0$ mA			2.4			V
Output low level voltage	$V_{OL}$	$I_{OL} = 2.1$ mA					0.4	V
Operating supply current (DC)	$I_{CCA1}$	$V_{CE} \leq 0.2$ V, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V $I_{I/O} = 0$ mA				1	5	mA
	$I_{CCA2}$	$V_{CE} = V_{IL}$ , $I_{I/O} = 0$ mA				3	10	mA
Average operating supply current	$I_{CCA3}$	min cycle Duty = 100% $I_{I/O} = 0$ mA	Access time	70 ns		30	50	mA
				85 ns		25	50	
				100 ns		23	50	
				120 ns		20	50	
Standby supply current	$I_{CCS1}$	$V_{CE} \geq V_{CC} - 0.2$ V		-10 to +70°C			5	$\mu A$
				-10 to +40°C			1	
				25°C		0.2	0.5	
	$I_{CCS2}$	$V_{CE} = V_{IH}$				0.4	2	mA

\* Reference values at  $V_{CC} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$

# LC36256ALL, AMLL-70W/85W/10W/12W

## Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			8	pF
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			6	pF

These parameters were obtained through sampling, and not full-lot measurement.

## AC Electrical Characteristics at Ta = -10 to +70°C, V<sub>CC</sub> = 5 V ± 10%

### AC testing conditions

- Input pulse voltage level : 0.8 V, 2.2 V
- Input rise and fall time : 5 ns
- Input - output timing level : 1.5 V
- Output load : 1 TTL gate + C<sub>L</sub> = 100 pF (85 ns/100 ns/120 ns)  
1 TTL gate + C<sub>L</sub> = 30 pF (70 ns)  
(including scope and jig capacitance)

## Read Cycle

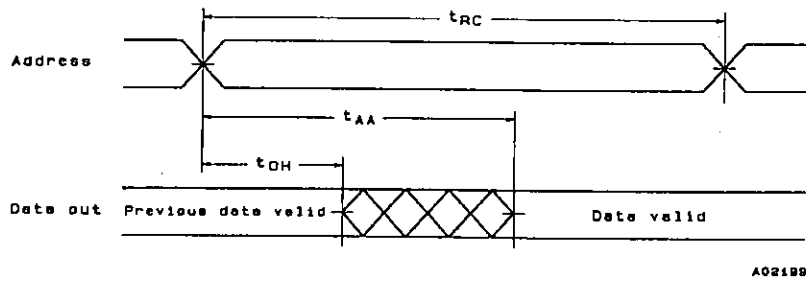
Parameter	Symbol	LC36256ALL-70W LC36256AMLL-70W		LC36256ALL-85W LC36256AMLL-85W		LC36256ALL-10W LC36256AMLL-10W		LC36256ALL-12W LC36256AMLL-12W		Unit
		min	max	min	max	min	max	min	max	
Read cycle time	t <sub>RC</sub>	70		85		100		120		ns
Address access time	t <sub>AA</sub>		70		85		100		120	ns
CE access time	t <sub>CA</sub>		70		85		100		120	ns
OE access time	t <sub>OA</sub>		35		45		50		60	ns
Output hold time	t <sub>OH</sub>	20		20		20		20		ns
CE output enable time	t <sub>COE</sub>	10		10		10		10		ns
OE output enable time	t <sub>OOE</sub>	5		5		5		5		ns
CE output disable time	t <sub>COD</sub>	0	30	0	30	0	30	0	30	ns
OE output disable time	t <sub>OOD</sub>	0	30	0	30	0	30	0	30	ns

## Write Cycle

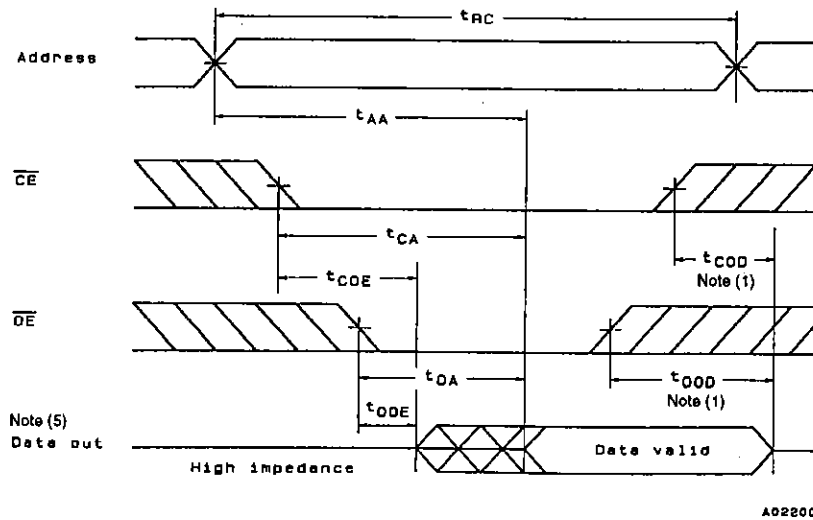
Parameter	Symbol	LC36256ALL-70W LC36256AMLL-70W		LC36256ALL-85W LC36256AMLL-85W		LC36256ALL-10W LC36256AMLL-10W		LC36256ALL-12W LC36256AMLL-12W		Unit
		min	max	min	max	min	max	min	max	
Write cycle time	t <sub>WC</sub>	70		85		100		120		ns
Address valid to end of write	t <sub>AW</sub>	65		75		80		100		ns
Address setup time	t <sub>AS</sub>	0		0		0		0		ns
Write pulse width	t <sub>WP</sub>	50		50		60		70		ns
CE setup time	t <sub>CW</sub>	65		75		80		100		ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0		0		0		0		ns
Write recovery time ( $\overline{OE}$ )	t <sub>WR1</sub>	0		0		0		0		ns
Data setup time	t <sub>DS</sub>	30		30		35		40		ns
Data hold time	t <sub>DH</sub>	0		0		0		0		ns
$\overline{WE}$ output enable time	t <sub>WOE</sub>	10		10		10		10		ns
$\overline{WE}$ output disable time	t <sub>WOD</sub>	0	25	0	25	0	25	0	25	ns

## Timing Chart

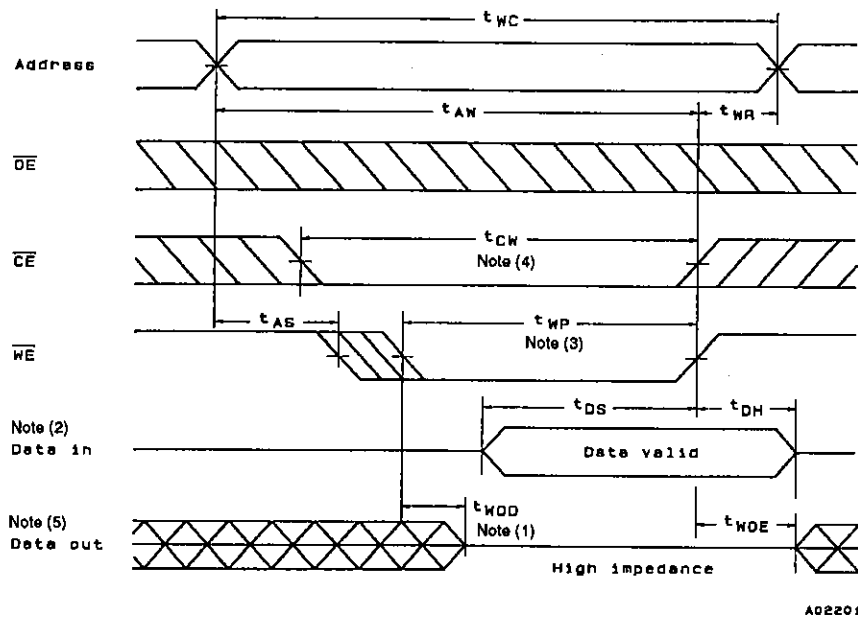
- Read Cycle (1):  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$



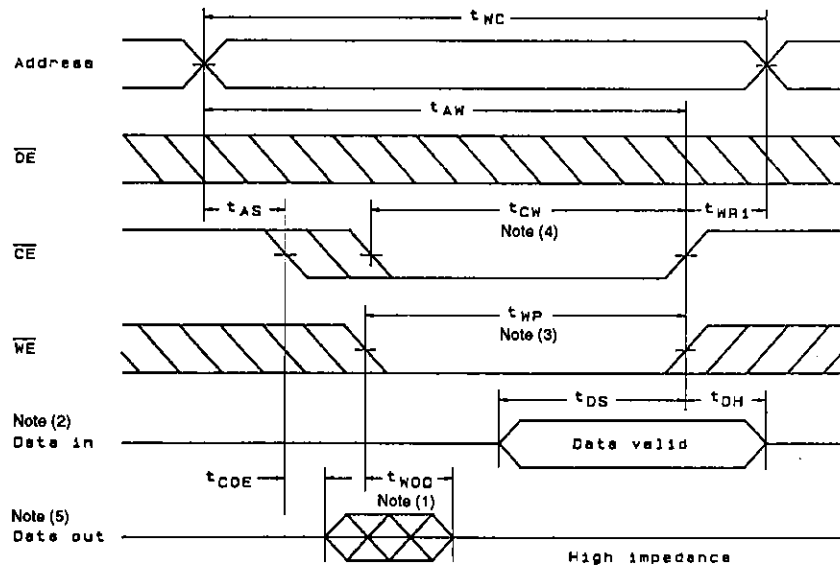
- Read Cycle (2):  $\overline{WE} = V_{IH}$



- Write Cycle (1):  $\overline{WE}$  Control Note (6)



• Write Cycle (2):  $\overline{CE}$  Control Note (6)



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- Notes: (1)  $t_{COD}$ ,  $t_{OOD}$ , and  $t_{WOD}$  are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
- (2) An external antiphase signal must not be applied when  $D_{OUT}$  is in the output state.
- (3)  $t_{WP}$  is the time interval that  $\overline{CE}$  and  $\overline{WE}$  are low-level and is defined as the interval from the falling of  $\overline{WE}$  to the rising of  $\overline{CE}$  or  $\overline{WE}$  whichever is earlier.
- (4)  $t_{CW}$  is the time interval that  $\overline{CE}$  and  $\overline{WE}$  are low-level and is defined as the time from the falling of  $\overline{CE}$  to the rising of  $\overline{CE}$  or  $\overline{WE}$ , whichever is earlier.
- (5)  $D_{OUT}$  goes to the high-impedance state when either  $\overline{OE}$  is high-level,  $\overline{CE}$  is high-level, or  $\overline{WE}$  is low-level.
- (6) When  $\overline{OE}$  is high-level during the write cycle,  $D_{OUT}$  goes to the high-impedance state.

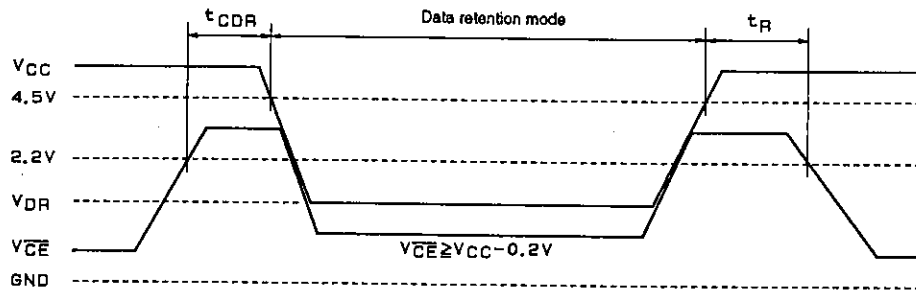
**Data Retention Characteristics at  $T_a = -10$  to  $+70^\circ\text{C}$**

Parameter	Symbol	Conditions	min	typ <sup>*1</sup>	max	Unit
Data retention supply voltage	$V_{DR}$	$V_{CE} \geq V_{CC} - 0.2 \text{ V}$	2.0		5.5	V
Data retention supply current	$I_{CCDR1}$	$V_{CC} = 3.0 \text{ V}$ , $V_{CE} \geq 2.8 \text{ V}$			3	$\mu\text{A}$
		$-10$ to $+70^\circ\text{C}$				
		$-10$ to $+40^\circ\text{C}$			0.6	
	$I_{CCDR2}$	$V_{CC} = 2.0$ to $5.5 \text{ V}$ , $V_{CE} \geq V_{CC} - 0.2 \text{ V}$		0.1	0.3	$\mu\text{A}$
$\overline{CE}$ setup time	$t_{CDR}$		0			ns
$\overline{CE}$ hold time	$t_H$		$t_{RC}$ <sup>*2</sup>			ns

\* 1. Reference values at  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$

\* 2.  $t_{RC}$  = Read Cycle time

## Data Retention Waveform



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