	No. 2666A	LC5733, 5733H
	SINGLE-CHIP 4-BIT MICROCOMPUTER WITH LCD DRIVERS FOR LOW-VOLTAGE, LOW-POWER USE	

General Description

The LC5733/5733H are single-chip 4-bit microcomputers with LCD drivers. The features of the LC5733/5733H include low-voltage operation, low power dissipation, etc. The HALT function, which can be used to stop/start the CPU operations, facilitates the low power dissipation of the system. The LC5733/5733H are ideally suited for use in melody function-provided timepiece/timer applications.

◆ Hardware Features

- ROM 2048 x 8 bits • RAM 128 x 4 bits
- Instruction execution time
 - 120 μ s 1.3V to 1.65V (LC5733 Ag version)
 - 120 μ s 2.6V to 3.6V (LC5733 Li version)
 - 60 μ s 2.0V to 3.6V (LC5733 EXTV version)
 - 17.6 μ s 4.5V to 6.0V (LC5733H EXTV version)
- Current dissipation 1.0 μ A typ at 1.55V (LC5733 Ag version): HALT mode
0.8 μ A typ at 2.9V (LC5733 Li version): HALT mode
- Input/output pins Number of input pins: 8
Number of input/output pins: 8 (8 x 8 key matrix configuration available)
Number of control output pins: 3 (Alarm output pins: 2, output pin: 1)
- LCD drivers

LCD display system	Number of drivable segments
Static	27 segments (max)
1/2bias-1/2duty	54 segments (max)
1/2bias-1/3duty	81 segments (max)

- Possible to use LCD drive output pins as output-only ports (mask option-selectable)
- On-chip melody function 3 octaves
- On-chip segment PLA
The LCD driver output can be used to support any LCD panel layout without software processing.
- On-chip step-up/step-down circuit
- Shipping style: FLP-64 (or chip)

◆ Software Features

- Powerful instruction set: 93 instructions
- Table read instruction (possible to set table in all ROM areas)
- 1-level subroutine nesting
- On-chip time-base 15-bits divider (delivers overflow signal every 32ms or 64ms/100ms/500ms when a 32.768kHz crystal OSC is used)
- HALT function

Application Development Support System

- Evaluation chip (LC5797) is available for application development and the dedicated equipment is available as the application development tools.
- SDS-410 system
Using the SDS-410, program development (editing, assembling) for microcomputer application circuit may be done. (IBM-PC or its equivalent also available)
- EVA-510 + TB-5734 + **DCB-1 + Application evaluation board + LC5797 (**Rev. 2.0 or greater)
By connecting to the SDS-410, application development program correction and debugging may be done.
- TB-5734 + **DCB-1 + Application evaluation board + LC5797
By using the EPROM (2732) with application development program data written in, mounting evaluation may be done.

* The IBM-PC is an IBM-made product.

Note) The application evaluation board is constructed by the user.

LEDs or LCDs may be used for display.

The EVA-510 is a modified version of the EVA-410 whose monitor ROM is replaced by the SCR-5734.

Since the evaluation chip and the LC5733, 5733H differ in RAM capacity, be sure to check the RAM capacity when preparing or debugging programs.

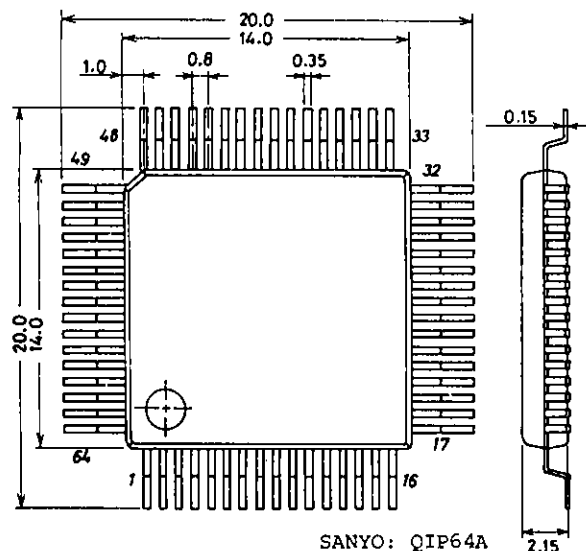
LC5733: 128 x 4 bits

LC5797: 256 x 4 bits

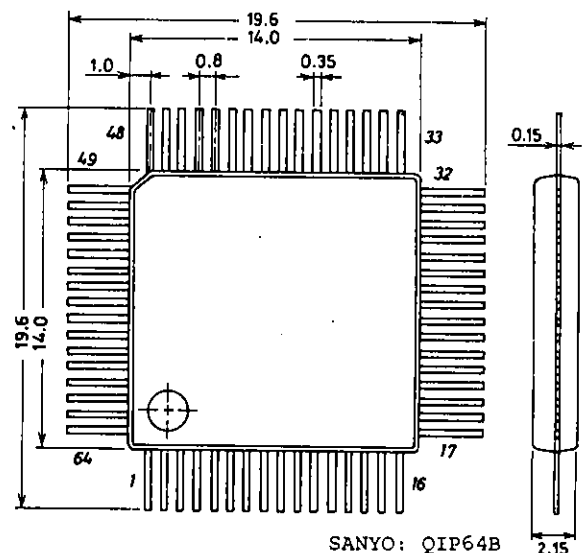
Sample Applications

- LCD game
- Multifunctional timepiece
- Timer
- Desk-top calculator

Package Dimensions 3057-Q64A1C (unit: mm)



Package Dimensions 3026B-Q64B1C (unit: mm)



When mounting the QIP package on the board, do not dip it in solder.

Note) When developing programs, take care of the DP_H value. The usable DP_H values are 0 to 7. We will be will free from any blame even if you use $DP_H=8$ to F_H to develop programs.

Pad Name and Coordinates

QIP 64 Pin Assignment					QIP 64 Pin Assignment				
	Pad No.	Pin Name	X (μm)	Y (μm)		Pad No.	Pin Name	X (μm)	Y (μm)
26	1	VDD	-300	2590	57	34	CUP1	45	-2590
27	2	S4	-485	2590	58	35	CUP2	255	-2590
28	3	S3	-710	2590	59	36	S2	460	-2590
29	4	M1	-1020	2590	60	37	S1	685	-2590
30	5	M2	-1245	2590	61	38	RES	915	-2590
31	6	M3	-1470	2590	62	39	OSCIN	1215	-2590
32	7	M4	-1700	2590	63	40	OSCOU	1440	-2590
	8	TEST	-1700	2355	64	41	TEST	1700	-2590
	9	TEST	-1700	2130	1	42	P00	1700	-2265
33	10	SEG14	-1700	1860	2	43	P01	1700	-1975
34	11	SEG15	-1700	1640	3	44	P02	1700	-1680
35	12	SEG16	-1700	1420	4	45	P03	1700	-1390
36	13	SEG17	-1700	1200	5	46	COM2	1700	-960
37	14	SEG18	-1700	980	6	47	SEG1	1700	-605
38	15	SEG19	-1700	760	7	48	SEG2	1700	-385
39	16	SEG20	-1700	540	8	49	SEG3	1700	-165
40	17	SEG21	-1700	320	9	50	SEG4	1700	55
41	18	SEG22	-1700	100	10	51	SEG5	1700	275
42	19	SEG23	-1700	-120	11	52	SEG6	1700	495
43	20	SEG24	-1700	-340	12	53	SEG7	1700	715
44	21	SEG25	-1700	-560	13	54	SEG8	1700	935
45	22	SEG26	-1700	-780	14	55	SEG9	1700	1160
46	23	SEG27	-1700	-1000	15	56	SEG10	1700	1380
47	24	COM1	-1700	-1180	16	57	SEG11	1700	1600
48	25	P13	-1700	-1405	17	58	SEG12	1700	2590
49	26	P12	-1700	-2590	18	59	SEG13	1455	2590
50	27	P11	-1470	-2590	19	60	COM3	1225	2590
51	28	P10	-1260	-2590	20	61	LIGHT	1020	2590
52	29	CFOSC1	-1040	-2590	21	62	ALM1	810	2590
53	30	CFOSC2	-840	-2590	22	63	ALM2	615	2590
54	31	TEST	-630	-2590	23	64	Vss2	330	2590
55	32	T3	-405	-2590	24	65	Vss1	110	2590
56	33	32Hz	-180	-2590	25	66	BAK	-105	2590

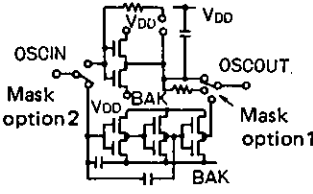
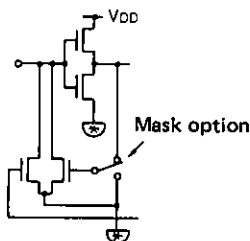
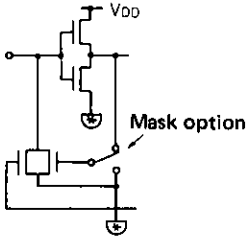
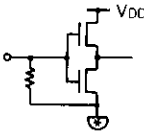
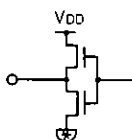
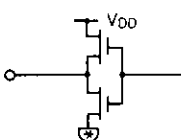
- The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.

Notes for developing an LC5730 series microcomputer-used system

The low current dissipation is a distinctive feature of the LC5730 series microcomputers. However, it is not easy to determine the total current to be dissipated in an LC5730 series microcomputer-used system by actual measurement when you develop a software, because much current flows in the peripherals of the evaluation tools.

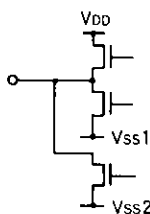
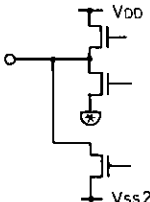
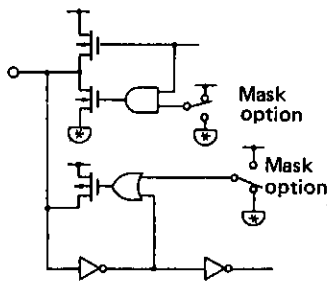
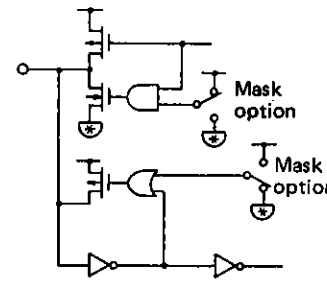
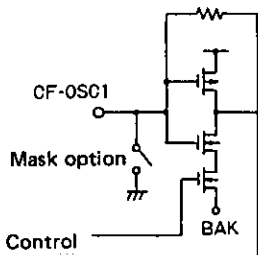
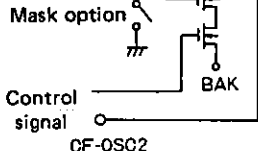
For a system which requires low current dissipation, check the current dissipation using an evaluation sample before mass-producing the system.



Pin Description

Pad No.	Pin Name	Input/Output	Circuit Configuration	Function																																		
39	OSCIN	Input		1) Crystal OSC mode A crystal is connected across OSCIN and OSCOUT for oscillation. 2) RC OSC mode R (external resistance) is connected across OSCIN and OSCOUT and C (external capacitance) is connected across OSCIN and VDD for oscillation.																																		
40	OSCOUT	Output																																				
37 36 3 2	S1 S2 S3 S4	Input		Input-only port LSI system is reset by applying VDD to S1 to S4 simultaneously.																																		
4 5 6 7	M1 M2 M3 M4	Input		Input-only port.																																		
38	RES	Input		Input pin for resetting LSI system.																																		
66	BAK			(-) power supply pin for logic unit inside the LSI. For Li version, a capacitor must be connected across BAK and VDD to prevent the logic unit from malfunctioning.																																		
61	LIGHT	Output		Output-only pin Suited for delivering signal to drive transistor for light.																																		
62 63	ALM1 ALM2	Output		Output-only pins Used to deliver *4kHz, 2kHz, 1kHz modulation signal with the execution of an instruction. Also used to deliver non-modulation signal. Used to deliver melody signal of 3 octaves with the execution of an instruction.																																		
1	VDD			(+) power supply pin.																																		
64 65	VSS2 VSS1			(-) power supply pins Ag version, Li version, EXT-V version: Mask option-selectable. <table border="1" data-bbox="965 1906 1377 2051"><thead><tr><th rowspan="2"></th><th colspan="2">Ag USE</th><th colspan="2">Li USE</th><th colspan="2">EXT-V USE</th></tr><tr><th>static</th><th>1/2 bias</th><th>static</th><th>1/2 bias</th><th>static</th><th>1/2 bias</th></tr></thead><tbody><tr><td>VDD</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>VSS1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>VSS2</td><td></td><td></td><td></td><td></td><td></td><td></td></tr></tbody></table>		Ag USE		Li USE		EXT-V USE		static	1/2 bias	static	1/2 bias	static	1/2 bias	VDD							VSS1							VSS2						
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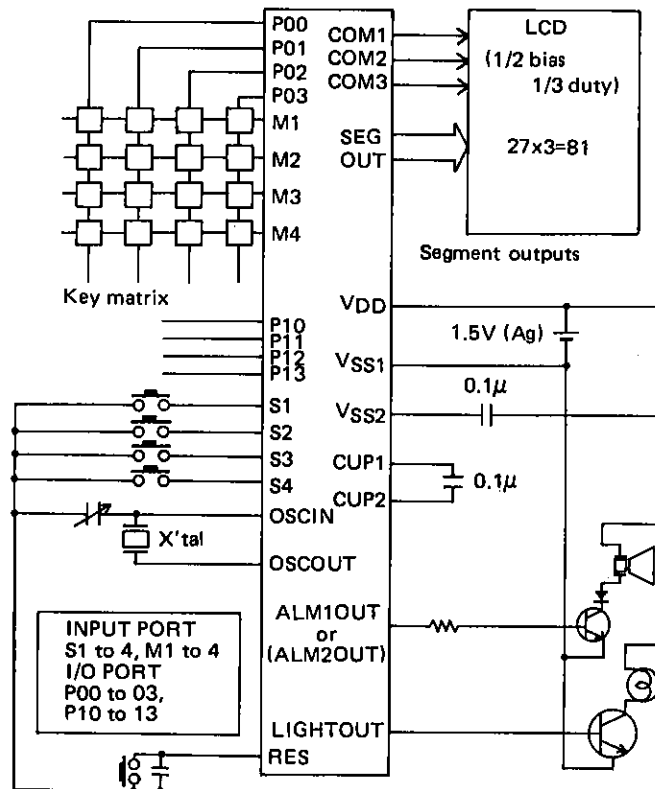
Pad No.	Pin Name	Input/Output	Circuit Configuration	Function																				
34 35	CUP1 CUP2			Pins for connecting voltage step-up (step-down) capacitor.																				
24 46 60	COM1 COM2 COM3	Output		Output pins for LCD panel common plate. The following pin is used in each case. <table border="1"><thead><tr><th></th><th>Static</th><th>1/2duty</th><th>1/3duty</th></tr></thead><tbody><tr><td>COM1</td><td>○</td><td>○</td><td>○</td></tr><tr><td>COM2</td><td>—</td><td>○</td><td>○</td></tr><tr><td>COM3</td><td>—</td><td>—</td><td>○</td></tr><tr><td>Alternating frequency</td><td>32Hz</td><td>32Hz</td><td>43Hz</td></tr></tbody></table> (Alternating frequency is for 32.768kHz crystal OSC application.)		Static	1/2duty	1/3duty	COM1	○	○	○	COM2	—	○	○	COM3	—	—	○	Alternating frequency	32Hz	32Hz	43Hz
	Static	1/2duty	1/3duty																					
COM1	○	○	○																					
COM2	—	○	○																					
COM3	—	—	○																					
Alternating frequency	32Hz	32Hz	43Hz																					
10 to 23 47 to 59	Segment Driver	Output		Output pins for LCD panel segments. Mask option permits SEG14 to SEG27 (Pad No. 10 to 23) to be used as output ports.																				
33 32 41 8 9 31	32Hz T3 TEST	Test		Test pins (not used by user)																				
42 43 44 45	P-00 P-01 P-02 P-03	Input/Output		<ul style="list-style-type: none">4-bit input/output port.Mask option can be used to select C-MOS output or P-ch open drain output.																				
28 27 26 25	P-10 P-11 P-12 P-13	Input/Output		<ul style="list-style-type: none">4-bit input/output port.Mask option can be used to select C-MOS output or P-ch open drain output.																				
29	CF-OSC1	Input		Input pin used to provide OSC and also used for internal clock generation. When no ceramic resonator is used, this input pin is set at "L" level by mask option.																				
30	CF-OSC2	Output		Output pin used to provide OSC.																				

Note) For Ag battery power supply,  is connected to VSS1, for Li battery /EXT-V power supply,  is connected to VSS2.

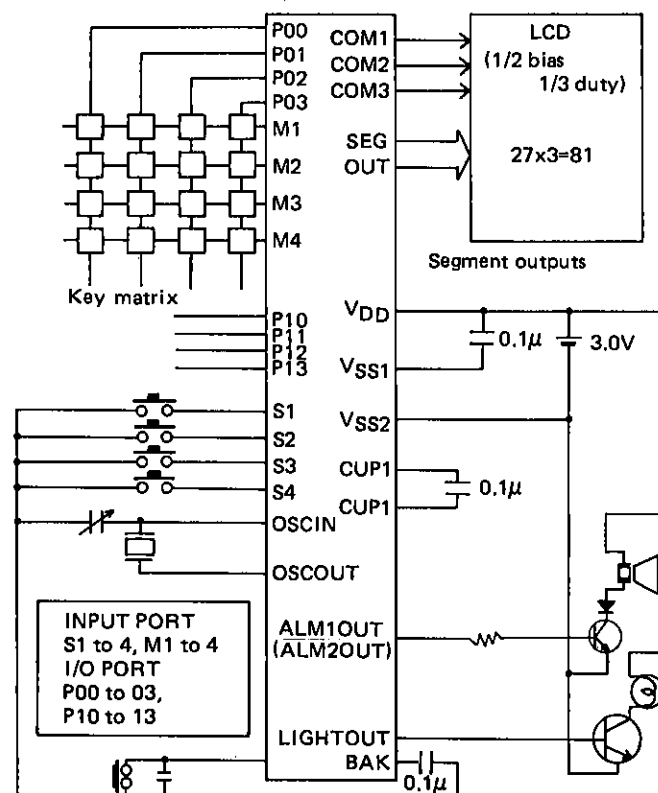
*4kHz, 2kHz, 1kHz: For 32.768kHz crystal OSC application, Proportional to OSC frequency.

Sample Application Circuits

(1) Typical application circuit for Ag version (1/2bias, 1/3duty)

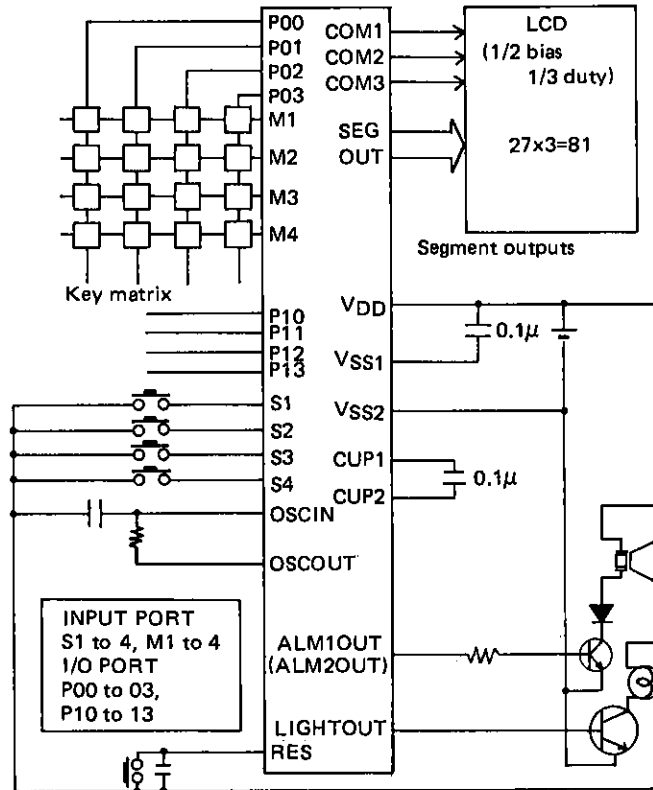


(2) Typical application circuit for Li version (1/2bias, 1/3duty)



Unit (capacitance: F)

(3) Typical application circuit for EXT-V version (1/2bias, 1/3duty)



Unit (capacitance: F)

● Ag Version

Absolute Maximum Ratings/ $T_a=25\pm2^\circ\text{C}$, $V_{DD}=0\text{V}$

			Limits	Unit
Maximum Supply Voltage	VSS1		-4.0 to +0.3	V
	VSS2		-4.0 to +0.3	V
Maximum Input Voltage	VIN1	S1-4, M1-4, P00-03, P10-13, 32Hz, TEST, OSC1N, RES	VSS1-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	32Hz, CUP2, OSCOUT, ALM1, ALM2, LIGHT P00-0.3, P10-13	VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1, COM2, COM3, CUP1	VSS2-0.3 to 0.3	V
Operating Temperature	Topr		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Conditions/ $T_a=-30$ to $+70^\circ\text{C}$, $V_{DD}=0\text{V}$

			Limits			unit
			min	typ	max	
Supply Voltage	VSS1		-1.65		-1.30	V
	VSS2		-3.3		-2.4	V
Input "H"-Level Voltage	VIH	S1-4, M1-4, RES, P00-03, P10-13	-0.2		0	V
Input "L"-Level Voltage	VIL	S1-4, M1-4, RES, P00-03, P10-13, 8Hz-IN	VSS1		VSS1 +0.2	V
Operating Frequency	fopg1	Crystal OSC (Fig. 7)	32	32.768	33	kHz
	fopg2	RC OSC (Fig. 12)		32.768		kHz

Electrical Characteristics/ $T_a=-30$ to $+70^\circ\text{C}$, $V_{DD}=0\text{V}$

			Limits			Unit
			min	typ	max	
Input Resistance	RIN1A	VSS1=-1.55V, VIL=VSS1+0.2V, "L"-level hold Tr., *1, Fig. 1	200	800	2000	kΩ
	RIN1B	VSS1=-1.55V "L"-level pull-in Tr., *1, Fig. 1	50	100	200	kΩ
	RIN2A	VSS1=-1.55V, VIH=-0.2V, "H"-level hold tr., *4, Fig. 6	100	400	2000	kΩ
	RIN3	VSS1=-1.55V, TEST, RES	10		300	kΩ
Output "H"-Level Voltage	VOH1	VSS1=-1.55V, IOH=-0.4μA, *2	-0.2			V
Output "L"-Level Voltage	VOL1	VSS1=-1.55V, IOL=0.4μA, *2			VSS2 +0.2	V
Output "H"-Level Voltage	VOH2	VSS1=-1.55V, IOH=-4μA, COM1, COM2, COM3	-0.2			V
Output "M"-Level Voltage	VOM	VSS1=-1.55V, IOH=-4μA, IOL=4μA, COM1, COM2, COM3	VSS1 -0.2		VSS1 +0.2	V
Output "L"-Level Voltage	VOL2	VSS1=-1.55V, IOL=4μA, COM1, COM2, COM3			VSS2 +0.2	V

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			Limits			Unit
			min	typ	max	
Output "H"-Level Voltage	VOH3	VSS1=-1.35V, IOH=-250μA, LIGHT	-0.65			V
Output "L"-Level Voltage	VOL3	VSS1=-1.35V, IOL=150μA, LIGHT			VSS1 +0.65	V
Output "H"-Level Voltage	VOH4	VSS1=-1.55V, IOH=-20μA, *3	-0.2			V
Output "L"-Level Voltage	VOL4	VSS1=-1.55V, IOL=20μA, *3			VSS1 +0.2	V
Output "H"-Level Voltage	VOH5	VSS1=-1.35V, IOH=-1mA, ALM1, ALM2	-0.65			V
Output "L"-Level Voltage	VOL5	VSS1=-1.35V, IOL=1mA, ALM1, ALM2			VSS1 +0.65	V
Output Current (H)	IOH	VDD-VSS1=1.55V, VOH=VSS1×0.5 *4			-100	μA
Output Current (L)	IOL	VDD-VSS1=1.55V, VOL=VSS1×0.5 *4	5			μA
Output Voltage	VSS2	VSS1=-1.35V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 2	-3.3		-2.5	V
Supply Current 1	IDD1	VSS1=-1.55V, C1=C2=0.1μF, Cg=20pF, CI ≤ 25kΩ Ta ≤ 50°C Xtal OSC, HALT mode, Fig. 2		1.0	3.0	μA
Supply Current 2	IDD2	VSS=-1.55V, C1=C2=0.1μF, Rext=470kΩ, Cext=30pF RC OSC, HALT mode, Fig. 8 Ta ≤ 50°C		5.0	15.0	μA
OSC Start Voltage	Vstt	Cg=20pF, Xtal OSC (CI ≤ 25kΩ), Fig. 3, Ta=25°C	-1.35			V
OSC Hold Voltage	VHOLD	Cg=20pF, Xtal OSC (CI ≤ 25kΩ), Fig. 3, Ta=25°C	-1.65		-1.30	V
OSC Start Time	tstt	Cg=20pF, Xtal OSC, VSS1=-1.35V (CI ≤ 25kΩ), Fig. 3, Ta=25°C			10	s
OSC Compensation	20pF	RC OSC (OSCIN side)	16	20	24	pF

● Li Version

Absolute Maximum Ratings/ $T_a=25\pm2^{\circ}\text{C}$, $V_{DD}=0\text{V}$

			Limits	Unit
Maximum Supply Voltage	VSS1		-4.0 to +0.3	V
	VSS2		-4.0 to +0.3	
Maximum Input Voltage	VIN1	OSCIN, 32Hz	VSS1-0.3 to 0.3	V
	VIN2	S1-4, M1-4, TEST, RES, P00-03, P10-13	VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOOUT1	32Hz, CUP2, OSCOUT	VSS1-0.3 to 0.3	V
	VOOUT2	SEGOUT, COM1, COM2, COM3, CUP1, LIGHT, ALM1, ALM2, P00-03, P10-13	VSS2-0.3 to 0.3	
Operating Temperature	Topr		-30 to +70	$^{\circ}\text{C}$
Storage Temperature	Tstg		-40 to +125	$^{\circ}\text{C}$

Allowable Operating Conditions/ $T_a=-30$ to $+70^{\circ}\text{C}$, $V_{DD}=0\text{V}$

			Limits			Unit
			min	typ	max	
Supply Voltage	VSS1		-3.6		-1.3	V
	VSS2		-3.6		-2.6	V
Input "H"-Level Voltage	V _{IH}	S1-4, M1-4, RES, P00-03, P10-13	-0.4		0	V
Input "L"-Level Voltage	V _{IL}	S1-4, M1-4, RES, P00-03, P10-13	VSS2		VSS2 +0.4	V
Operating Frequency	fopg1	Crystal OSC (Fig. 7)	32	32.768	33	kHz

Electrical Characteristics/ $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD} = 0\text{V}$

			Limits			Unit
			min	typ	max	
Input Resistance	R _{IN1A}	V _{SS2} = -2.9V, V _{IL} = V _{SS2} + 0.4V, "L"-level hold tr., *1, Fig. 4	150	300	1000	k Ω
	R _{IN1B}	V _{SS2} = -2.9V, "L"-level pull-in Tr., *1, Fig. 4	60	100	150	k Ω
	R _{IN2A}	V _{SS2} = -2.9V, V _{IH} = -0.4V, "H"-level hold tr., *4, Fig. 6	200	600	2000	k Ω
	R _{IN3}	V _{SS2} = -2.9V, TEST, RES	10		300	k Ω
Output "H"-Level Voltage	V _{OH1}	V _{SS2} = -2.9V, I _{OH} = -0.4 μA , *2	-0.2			V
Output "L"-Level Voltage	V _{OL1}	V _{SS2} = -2.9V, I _{OL} = 0.4 μA , *2			V _{SS2} + 0.2	V
Output "H"-Level Voltage	V _{OH2}	V _{SS2} = -2.9V, I _{OH} = -4 μA , COM1, COM2, COM3	-0.2			V
Output "M"-Level Voltage	V _{OM}	V _{SS2} = -2.9V, I _{OH} = -4 μA , I _{OL} = 4 μA , COM1, COM2, COM3	V _{SS2} /2 - 0.2		V _{SS2} /2 + 0.2	V
Output "L"-Level Voltage	V _{OL2}	V _{SS2} = -2.9V, I _{OL} = 4 μA , COM1, COM2, COM3			V _{SS2} + 0.2	V
Output "H"-Level Voltage	V _{OH3}	V _{SS2} = -2.4V, I _{OH} = -250 μA , ALM1, ALM2	-0.65			V
Output "L"-Level Voltage	V _{OL3}	V _{SS2} = -2.4V, I _{OL} = 250 μA , ALM1, ALM2			V _{SS2} + 0.65	V
Output "H"-Level Voltage	V _{OH4}	V _{SS2} = -2.4V, I _{OH} = -150 μA LIGHT	-1.5			V
Output "L"-Level Voltage	V _{OL4}	V _{SS2} = -2.4V, I _{OL} = 150 μA LIGHT			V _{SS2} + 1.5	V
Output Current (H) 1	I _{OH1}	V _{SS2} = -2.9V, V _{OH} = -0.4V, *3			-50	μA
Output Current (L) 1	I _{OL1}	V _{SS2} = -2.9V, V _{OL} = V _{SS2} + 0.4V, *3	50			μA
Output Current (H) 2	I _{OH2}	V _{SS2} = -2.9V, V _{OH} = -0.4V, *4			-450	μA
Output Current (L) 2	I _{OL2}	V _{SS2} = -2.9V, V _{OL} = V _{SS2} + 0.4V *4	450			μA
Output Voltage (halver)	V _{SS1}	V _{SS2} = -2.8V, C ₁ = C ₂ = 0.1 μF , f _{opg} = 32.768kHz, Fig. 5			-1.35	V
Supply Current	I _{DD}	V _{SS2} = -2.9V, X _{tal} OSC (C _I \leq 25k Ω) HALT mode, C ₁ = C ₂ = 0.1 μF , T _a \leq 50 $^\circ\text{C}$ C _g = 20pF, Fig. 5		0.8	2.5	μA
OSC Start Voltage 1	V _{Stt1}	C _g = 20pF	-1.35			V
OSC hold Voltage 1	V _{HOLD1}	X _{tal} OSC (C _I \leq 25k Ω), Fig. 3 T _a = 25 $^\circ\text{C}$			-1.3	V
OSC Start Time	t _{stt}	V _{SS1} = V _{SS2} = -1.35V, C _g = 20pF X _{tal} OSC (C _I \leq 25k Ω), Fig. 3, T _a = 25 $^\circ\text{C}$			10	s

• EXT-V Version (Xtal OSC, CF OSC, RC OSC)

Absolute Maximum Ratings/ $T_a=25\pm2^{\circ}\text{C}$, $V_{DD}=0\text{V}$

			Limits	Unit
Maximum Supply Voltage	VSS1		-7.0 to +0.3	V
	VSS2		-7.0 to +0.3	V
Maximum Input Voltage	VIN1	OSCIN, 32Hz, CF-OSC1	VSS2-0.3 to 0.3	V
	VIN2	S1-4, M1-4, TEST, RES, P00-03, P10-13	VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOU1	32Hz, CUP2, OSCOUT, CF-OSC2	VSS2-0.3 to 0.3	V
	VOU2	SEGOUT, COM1, COM2, COM3, CUP1, LIGHT, ALM1, ALM2, P00-03, P10-13	VSS2-0.3 to 0.3	V
Operating Temperature	Topr		-30 to +70	$^{\circ}\text{C}$
Storage Temperature	Tstg		-40 to +125	$^{\circ}\text{C}$

Allowable Operating Conditions/ $T_a=-30$ to $+70^{\circ}\text{C}$, $V_{DD}=0\text{V}$

			Limits			Unit
			min	typ	max	
Supply Voltage	VSS1		-6.0		-1.30	V
	VSS2		-6.0		-2.0	V
Input "H"-Level Voltage	VIH1	S1-4, M1-4, P00-03, P10-13	0.3X VSS2		0	V
Input "L"-Level Voltage	VIL1	S1-4, M1-4, P00-03, P10-13	VSS2		0.7X VSS2	V
Input "H"-Level Voltage	VIH2	RES	0.25X VSS2		0	V
Input "L"-Level Voltage	VIL2	RES	VSS2		0.75X VSS2	V
Operating Frequency	fopg1	Crystal OSC 1 (Fig. 7)	32	32.768	33	kHz
	fopg2	Crystal OSC2 (Fig. 7)	60	65.536	70	kHz
	fCF	CF OSC (Fig. 13), (Cycle time 16 μs at CF=500kHz)	380	455	500	kHz
	fCR	RC OSC (Fig. 12)		32.768		kHz

Electrical Characteristics/ $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD} = 0\text{V}$

			Limits			Unit
			min	typ	max	
Input Resistance	R _{IN1A}	$V_{SS2} = -2.9\text{V}$, $V_{IL} = V_{SS2} + 0.4\text{V}$, "L"-level hold tr., *1, Fig. 4	150	300	1000	k Ω
	R _{IN1B}	$V_{SS2} = -2.9\text{V}$, "L"-level pull-in Tr., *1, Fig. 4	60	100	150	k Ω
	R _{IN2A}	$V_{SS2} = -2.9\text{V}$, $V_{IH} = -0.4\text{V}$, "H"-level hold tr., *4, Fig. 6	200	600	2000	k Ω
	R _{IN3}	$V_{SS2} = -2.9\text{V}$, TEST, RES	10		300	k Ω
Output "H"-Level Voltage	V _{OH1}	$V_{SS2} = -2.9\text{V}$, $I_{OH} = -0.4\mu\text{A}$, *2	-0.2			V
Output "L"-Level Voltage	V _{OL1}	$V_{SS2} = -2.9\text{V}$, $I_{OL} = 0.4\mu\text{A}$, *2			$V_{SS2} + 0.2$	V
Output "H"-Level Voltage	V _{OH2}	$V_{SS2} = -2.9\text{V}$, $I_{OH} = -4\mu\text{A}$, COM1, COM2, COM3	-0.2			V
Output "M"-Level Voltage	V _{OM}	$V_{SS2} = -2.9\text{V}$, $I_{OH} = -4\mu\text{A}$, $I_{OL} = 4\mu\text{A}$, COM1, COM2, COM3	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	V _{OL2}	$V_{SS2} = -2.9\text{V}$, $I_{OL} = 4\mu\text{A}$ COM1, COM2, COM3			$V_{SS2} + 0.2$	V
Output "H"-Level Voltage	V _{OH3}	$V_{SS2} = -2.4\text{V}$, $I_{OH} = -2.0\text{mA}$, ALM1, ALM2	-1.0			V
Output "L"-Level Voltage	V _{OL3}	$V_{SS2} = -2.4\text{V}$, $I_{OL} = 2.0\text{mA}$, ALM1, ALM2			$V_{SS2} + 1.0$	V
Output "H"-Level Voltage	V _{OH4}	$V_{SS2} = -2.4\text{V}$, $I_{OH} = -250\mu\text{A}$, LIGHT	-0.65			V
Output "L"-Level Voltage	V _{OL4}	$V_{SS2} = -2.4\text{V}$, $I_{OL} = 250\mu\text{A}$, LIGHT			$V_{SS2} + 0.65$	V
Output Current (H) 1	I _{OH1}	$V_{SS2} = -3.0\text{V}$, $V_{OH} = -0.45\text{V}$, *3			-45	μA
Output Current (L) 1	I _{OL1}	$V_{SS2} = -3.0\text{V}$, $V_{OL} = V_{SS2} + 0.45\text{V}$, *3	45			μA
Output Current (H) 2	I _{OH2}	$V_{SS2} = -3.0\text{V}$, $V_{OH} = -0.45\text{V}$, *4			-450	μA
Output Current (L) 2	I _{OL2}	$V_{SS2} = -3.0\text{V}$, $V_{OL} = V_{SS2} + 0.45\text{V}$, *4	450			μA
Output Voltage (halver)	V _{SS1}	$V_{SS2} = -2.9\text{V}$, $C1 = C2 = 0.1\mu\text{F}$, f _{opg} = 32.768kHz, Fig. 5		-1.45	-1.35	V

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			Limits			Unit
			min	typ	max	
Supply Current 1	I _{DD1}	V _{SS2} =-3.0V, 32.768kHz Xtal OSC (C _I ≤25kΩ), T _a ≤50°C, HALT mode, C ₁ =C ₂ =0.1μF, C _g =20pF, Fig. 5		3.0	15	μA
Supply Current 2	I _{DD2}	V _{SS2} =-3.0V, 65.536kHz Xtal OSC (C _I ≤25kΩ), T _a ≤50°C, HALT mode, C ₁ =C ₂ =0.1μF, (C _d =20pF), C _g =10pF Fig. 5		8.0	30	μA
Supply Current 3	I _{DD3}	V _{SS2} =-3.0V, 455kHz CF OSC, HALT mode, C ₁ =C ₂ =0.1μF, C _{CFI} =C _{CCFO} =150pF, R _f =1MΩ, T _a ≤50°C, Fig. 10		80	300	μA
Supply Current 4	I _{DD4}	V _{SS2} =-3.0V, R _{EXT} =470kΩ, C _{ext} =30pF, C ₁ =C ₂ =0.1μF, T _a ≤50°C, Fig. 9		40	150	μA
OSC Start Voltage 1	V _{stt1}	C _g =20pF	-2.3			V
OSC Hold Voltage 1	V _{HOLD1}	32.768kHz Xtal OSC (C _I ≤25kΩ), Fig. 3, T _a =25°C			-2.0	V
OSC Start Time 1	t _{stt1}	V _{SS2} =-2.3V, C _g =20pF 32.768kHz Xtal OSC (C _I ≤25kΩ), Fig. 3, T _a =25°C			10	s
OSC Start Voltage 2	V _{stt2}	C _g =10pF (C _d =20pF), 65.536kHz Xtal OSC (C _I ≤25kΩ), Fig. 3, T _a =25°C	-2.6			V
OSC Hold Voltage 2	V _{HOLD2}				-2.4	V
OSC Start Time 2	t _{stt2}	V _{SS2} =-2.6V, C _g =10pF (C _d =20pF), T _a =25°C, 65.536kHz Xtal OSC (C _I ≤25kΩ), Fig. 3			10	s
OSC Start Voltage 3	V _{stt3}	C _{CFI} =C _{CCFO} =150pF, 455kHz CF OSC, R _f =1MΩ, Fig. 11, T _a =25°C	-2.0			V
OSC Hold Voltage 3	V _{HOLD3}				-2.0	V
OSC Start Time 3	t _{stt3}	C _{CFI} =C _{CCFO} =150pF, 455kHz CF OSC, R _f =1MΩ, Fig. 11, V _{SS2} =-2.0V, T _a =25°C			30	ms

LC5733, 5733H

LC5733H Version

• EXT-V Version (Xtal OSC, CF OSC, RC OSC)

Absolute Maximum Ratings/ $T_a=25\pm2^{\circ}\text{C}$, $V_{DD}=0\text{V}$

			Limits	Unit
Maximum Supply Voltage	VSS1		-7.0 to +0.3	V
	VSS2		-7.0 to +0.3	V
Maximum Input Voltage	VIN1	OSCIN, 32Hz, CF-OSC1	VSS2-0.3 to 0.3	V
	VIN2	S1-4, M1-4, TEST, RES, P00-0.3, P10-13	VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	32Hz, CUP2, OSCOUT, CF-OSC2	VSS2-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1, COM2, COM3, CUP1, LIGHT, ALM1, ALM2, P00-03, P10-13	VSS2-0.3 to 0.3	V
Operating Temperature	Topr		-30 to +70	$^{\circ}\text{C}$
Storage Temperature	Tstg		-40 to +125	$^{\circ}\text{C}$

Allowable Operating Conditions/ $T_a=-30$ to $+70^{\circ}\text{C}$, $V_{DD}=0\text{V}$

			Limits			Unit
			min	typ	max	
Supply Voltage	VSS1		-6.0		-2.20	V
	VSS2		-6.0		-4.5	V
Input "H"-Level Voltage	VIH1	S1-4, M1-4, P00-03, P10-13	0.3X VSS2		0	V
Input "L"-Level Voltage	VIL1	S1-4, M1-4, P00-03, P10-13	VSS2		0.7X VSS2	V
Input "H"-Level Voltage	VIH2	RES	0.25X VSS2		0	V
Input "L"-Level Voltage	VIL2	RES	VSS2		0.75X VSS2	V
Operating Frequency	fopg1	Crystal OSC 1 (Fig. 7)	32	32.768	33	kHz
	fopg2	Crystal OSC 2 (Fig. 7)	60	65.536	70	kHz
	fCF	CF OSC (Fig. 13), (Cycle time 16 μs at CF=500kHz)	380	455	500	kHz
	fCR	RC OSC (Fig. 12)		32.768		kHz

Electrical Characteristics/ $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD} = 0\text{V}$

			Limits			Unit
			min	typ	max	
Input Resistance	RIN1A	$V_{SS2} = -5.0\text{V}$, $V_{IL} = V_{SS2} + 0.4\text{V}$, "L"-level hold tr., *1, Fig. 4	70	200	600	k Ω
	RIN1B	$V_{SS2} = -5.0\text{V}$, "L"-level pull-in Tr., *1, Fig. 4	60	100	150	k Ω
	RIN2A	$V_{SS2} = -5.0\text{V}$, $V_{IH} = -0.4\text{V}$, "H"-level hold tr., *4, Fig. 6	100	400	1000	k Ω
	RIN3	$V_{SS2} = -5.0\text{V}$, TEST, RES	10		300	k Ω
Output "H"-Level Voltage	VOH1	$V_{SS2} = -5.0\text{V}$, $I_{OH} = -0.4\mu\text{A}$, *2	-0.2			V
Output "L"-Level Voltage	VOL1	$V_{SS2} = -5.0\text{V}$, $I_{OL} = 0.4\mu\text{A}$, *2			$V_{SS2} + 0.2$	V
Output "H"-Level Voltage	VOH2	$V_{SS2} = -5.0\text{V}$, $I_{OH} = -4\mu\text{A}$, COM1, COM2, COM3	-0.2			V
Output "M"-Level Voltage	VOM	$V_{SS2} = -5.0\text{V}$, $I_{OH} = -4\mu\text{A}$, $I_{OL} = 4\mu\text{A}$, COM1, COM2, COM3	$V_{SS2}/2 - 0.2$		$V_{SS2}/2 + 0.2$	V
Output "L"-Level Voltage	VOL2	$V_{SS2} = -5.0\text{V}$, $I_{OL} = 4\mu\text{A}$ COM1, COM2, COM3			$V_{SS2} + 0.2$	V
Output "H"-Level Voltage	VOH3	$V_{SS2} = -5.0\text{V}$, $I_{OH} = -2.0\text{mA}$, ALM1, ALM2	-1.0			V
Output "L"-Level Voltage	VOL3	$V_{SS2} = -5.0\text{V}$, $I_{OL} = 2.0\text{mA}$, ALM1, ALM2			$V_{SS2} + 1.0$	V
Output "H"-Level Voltage	VOH4	$V_{SS2} = -5.0\text{V}$, $I_{OH} = -250\mu\text{A}$, LIGHT	-0.65			V
Output "L"-Level Voltage	VOL4	$V_{SS2} = -5.0\text{V}$, $I_{OL} = 250\mu\text{A}$, LIGHT			$V_{SS2} + 0.65$	V
Output Current (H) 1	I _{OH1}	$V_{SS2} = -5.0\text{V}$, $V_{OH} = -0.75\text{V}$, *3			-75	μA
Output Current (L) 1	I _{OL1}	$V_{SS2} = -5.0\text{V}$, $V_{OL} = V_{SS2} + 0.75\text{V}$, *3	75			μA
Output Current (H) 2	I _{OH2}	$V_{SS2} = -5.0\text{V}$, $V_{OH} = -0.75\text{V}$, *4			-750	μA
Output Current (L) 2	I _{OL2}	$V_{SS2} = -5.0\text{V}$, $V_{OL} = V_{SS2} + 0.75\text{V}$, *4	750			μA
Output Voltage (halver)	VSS1	$V_{SS2} = -5.0\text{V}$, $C1 = C2 = 0.1\mu\text{F}$, fopg = 32.768kHz, Fig. 5			-2.4	V

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			Limits			Unit
			min	typ	max	
Supply Current 1	I _{DD1}	V _{SS2} =-5.0V, 32.768kHz Xtal OSC (C _I ≤25kΩ), T _a ≤50°C, HALT mode, C ₁ =C ₂ =0.1μF, C _g =20pF, Fig. 5		8.0	50	μA
Supply Current 2	I _{DD2}	V _{SS2} =-5.0V, 65.536kHz Xtal OSC (C _I ≤25kΩ), T _a ≤50°C, HALT mode, C ₁ =C ₂ =0.1μF, C _g =10pF (C _d =20pF), Fig. 5		20	100	μA
Supply Current 3	I _{DD3}	V _{SS2} =-5.0V, 455kHz CF OSC, HALT mode, C ₁ =C ₂ =0.1μF, C _{CFI} =C _{CFO} =150pF, R _f =1MΩ, T _a ≤50°C, Fig. 10		300	400	μA
Supply Current 4	I _{DD4}	V _{SS2} =-5.0V, R _{EXT} =470kΩ, C _{ext} =30pF, C ₁ =C ₂ =0.1μF, T _a ≤50°C, Fig. 9		200	400	μA
OSC Start Voltage 1	V _{stt1}	C _g =20pF	-2.3			V
OSC Hold Voltage 1	V _{HOLD1}	32.768kHz Xtal OSC (C _I ≤25kΩ), Fig. 3, T _a =25°C			-2.0	V
OSC Start Time 1	t _{stt1}	V _{SS2} =-2.3V, C _g =20pF 32.768kHz Xtal OSC (C _I ≤25kΩ), Fig. 3, T _a =25°C			10	s
OSC Start Voltage 2	V _{stt2}	C _g =10pF (C _d =20pF), 65.536kHz Xtal OSC (C _I ≤25kΩ),	-2.6			V
OSC Hold Voltage 2	V _{HOLD2}	Fig. 3, T _a =25°C			-2.4	V
OSC Start Time 2	t _{stt2}	T _a =25°C V _{SS2} =-2.6V, C _g =10pF (C _d =20pF) 65.536kHz Xtal OSC (C _I ≤25kΩ), Fig. 3			10	s
OSC Start Voltage 3	V _{stt3}	C _{CFI} =C _{CFO} =150pF, 455kHz CF OSC	-2.0			V
OSC Hold Voltage 3	V _{HOLD3}	R _f =1MΩ, Fig. 11, T _a =25°C			-2.0	V
OSC Start Time 3	t _{stt3}	C _{CFI} =C _{CFO} =150pF, 455kHz CF OSC, R _f =1MΩ, Fig. 11, V _{SS2} =-2.0V, T _a =25°C			30	ms

*1 S1, S2, S3, S4, M1, M2, M3, M4

*2 LCD driver output pins of SEGOUT1 to 13 and SEGOUT14 to 27.

*3 Output pins (used as output port) of SEGOUT14 to 27.

*4 P-00, P-01, P-02, P-03, P-10, P-11, P-12, P-13.

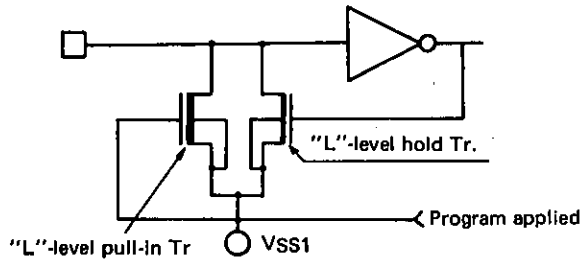


Fig. 1 Input configuration of S1-4, M1-4

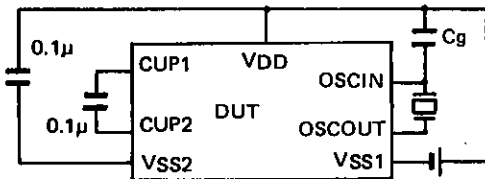


Fig. 2 Current dissipation, output voltage test circuit

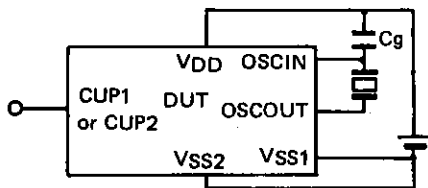


Fig. 3 Oscillation start voltage, oscillation start time, frequency stability, oscillation hold voltage test circuit.

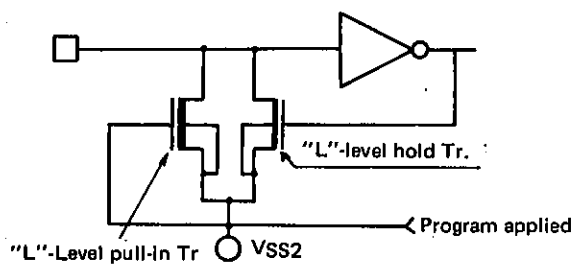


Fig. 4 Input configuration of S1-4, M1-4

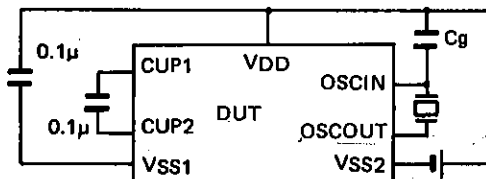


Fig. 5 Current dissipation, output voltage test circuit.

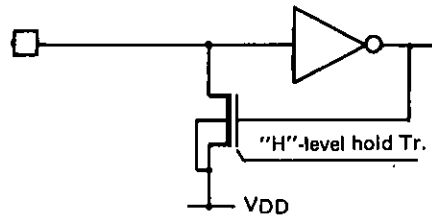


Fig. 6 Input configuration of P00-03, P10-13

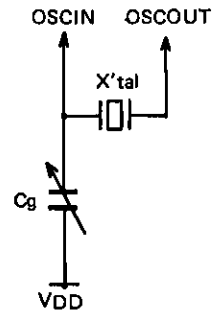


Fig. 7 Crystal oscillator

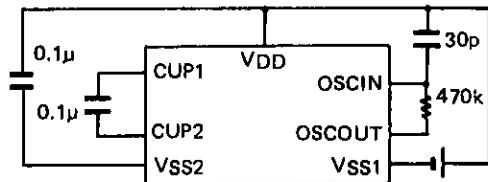


Fig. 8 Current dissipation, output voltage test circuit.

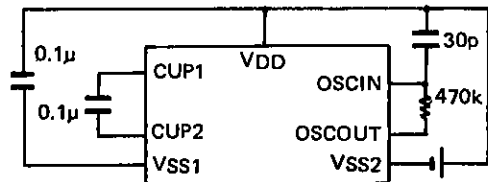


Fig. 9 Current dissipation, output voltage test circuit.

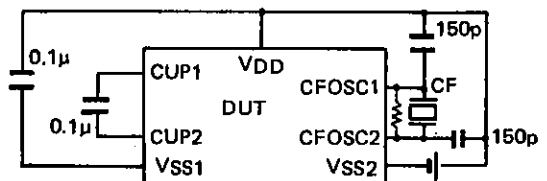


Fig. 10 Current dissipation, output voltage test circuit.

Unit (resistance: Ω, capacitance: F)

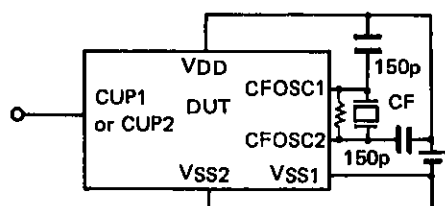


Fig. 11 Oscillation start voltage, oscillation start time, frequency stability, oscillation hold voltage test circuit.

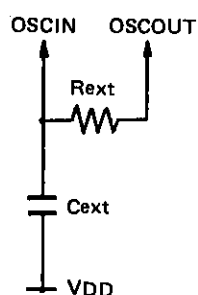


Fig. 12 RC oscillation

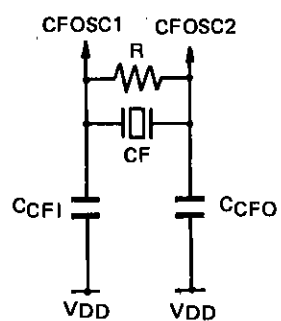


Fig. 13 CF oscillation

Unit (capacitance: F)

LC5733, 5733H

LC5733 Instruction Map

Instruction set: 93 instructions

☐ 1-cycle instruction ☐ 1-byte instruction
☐ 2-cycle instruction ☐ 2-byte instruction

LOWER UPPER	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	HALT	TAAT	TWRT	TMEL	CSP	CST	RC5	SC5	JMP X							
1	JMP*	PAGE	MTR	RTS	MPCL	MPCM	MPCH	IN	ASR0	ASR1	ASL0	ASL1	SDPL	SDPH	EDPL	EDPH
2	MVI X															
3	LDI X															
4	BAZ X								BAB0 X							
5	BANZ X								BAB1 X							
6	BCNH X								BAB2 X							
7	BCH X								BAB3 X							
8	ADC	SBC	ADD	SUB	ADN	AND	EOR	OR	ADC*	SBC*	ADD*	SUB*	ADN*	AND*	EOR*	OR*
9	ADCI	SBCI	ADDI	SUBI	ADNI	ANDI	EORI	ORI	INC	DEC	IDPL	DDPL	IDPH	DDPH	ISP	DSP
A	JSR X								IPM	LDA	LSP	LHLT	L500	STA	SSP	IPS
B	MDPL X															
C	MDPH X															
D	SIC X															
E	MSP X															
F	RCF	SCF	RLGT	SLGT	SPDR X				RBAK	SBAK	SAS X	CSEC	OUT	LDPL	LDPH	NOP

Instruction Set of LC5733

Summary of LC5733 Instructions

Symbol Meaning

AC	: Accumulator	M(DP)	: Memory addressed by DP	(), []	: Contents
ACn	: Accumulator bit	[P()]	: Contents of port ()	←	: Transfer direction, result
DP	: Data pointer	PC	: Program counter	Λ	: AND
EDP	: Save data pointer	STACK	: Stack register	V	: OR
SP	: Strobe pointer	[M(DP)]	: Contents of memory	⊕	: Exclusive OR
CF	: Carry flag		addressed by DP		
TREG	: Temporary register	STS _n	: Status register		
SCF _n	: Start condition flag n	CSTF	: Chrono start flag		
HEF _n	: Halt enable flag n	PDF	: Pull-down flag		
L(SP)	: LCD latch specified by SP	PAGE	: Page latch		
M	: Memory	PGX	: Current Page		

Instruction	Mnemonic		Instruction code								Bytes	Cycles	Function	Description	Status flag to be affected		
			D7	D6	D5	D4	D3	D2	D1	D0							
Accumulator manipulation instructions, memory manipulation instructions	RCF	Reset CF	1	1	1	1	0	0	0	0	1	1	CF ← 0	The CF is reset.	CF		
	SCF	Set CF	1	1	1	1	0	0	0	0	1	1	CF ← 1	The CF is set.	CF		
	ASR0	Shift Right AC & MSB=0	0	0	0	1	1	0	0	0	1	1	AC _n ← AC _{n+1} AC ₃ ← 0	The AC contents are shifted right and 0 is loaded to the MSB.			
	ASR1	Shift Right AC & MSB=1	0	0	0	1	1	0	0	0	1	1	AC _n ← AC _{n+1} AC ₃ ← 1	The AC contents are shifted right and 1 is loaded to the MSB.			
	ASL0	Shift Left AC & LSB=0	0	0	0	1	1	0	1	0	1	1	AC _n ← AC _{n-1} AC ₀ ← 0	The AC contents are shifted left and 0 is loaded to the LSB.			
	ASL1	Shift Left AC & LSB=1	0	0	0	1	1	0	1	0	1	1	AC _n ← AC _{n-1} AC ₀ ← 1	The AC contents are shifted left and 1 is loaded to the LSB.			
	INC	Increment M(DP)	1	0	0	1	1	0	0	0	0	1	1	M(DP), AC ← M(DP)+1	The memory M(DP) contents are incremented (+1) and are loaded to the M(DP) and AC.		
	DEC	Decrement M(DP)	1	0	0	1	1	0	0	0	1	1	1	M(DP), AC ← M(DP)-1	The memory M(DP) contents are decremented (-1) and are loaded to the M(DP) and AC.		
	TAAT	Read table data from program ROM	0	0	0	0	0	0	0	0	1	1	2	AC, TREG ← ROM (PGX, AC, M(DP))	The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the AC and TREG.		
MTR	Store TREG to M(DP)	0	0	0	1	0	0	1	0	1	0	1	M(DP) ← TREG	The TREG contents are stored to the M(DP).			
Operation instructions	ADC	Add M(DP) to AC with CF	1	0	0	0	0	0	0	0	0	1	1	AC ← (AC)+(M(DP)) ←(CF)	The AC, memory [M(DP)], CF contents are binary-added and the result is loaded to the AC.	CF	
	ADC*	Add M(DP) to AC with CF	1	0	0	0	1	0	0	0	0	1	1	AC, M(DP) ← (AC)+(M(DP)) ←(CF)	The AC, memory [M(DP)], CF contents are binary-added and the result is loaded to the AC and M(DP).	CF	
	SBC	Subtract M(DP) from AC with CF	1	0	0	0	0	0	0	0	1	1	1	AC ← (AC)+(M(DP)) ←(CF)	The memory M(DP), CF contents are binary-subtracted from the AC contents and the result is loaded to the AC.	CF	
	SBC*	Subtract M(DP) from AC with CF	1	0	0	0	1	0	0	1	1	1	1	AC, M(DP) ← (AC)+(M(DP)) ←(CF)	The memory M(DP), CF contents are binary-subtracted from the AC contents and the result is loaded to the AC and M(DP).	CF	
	ADD	Add M(DP) to AC	1	0	0	0	0	0	1	0	1	0	1	1	AC ← (AC)+(M(DP))	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC.	CF
	ADD*	Add M(DP) to AC	1	0	0	0	1	0	1	0	1	0	1	1	AC, M(DP) ← (AC)+(M(DP))	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC and M(DP).	CF
	SUB	Subtract M(DP) from AC	1	0	0	0	0	0	1	1	1	1	1	1	AC ← AC+(M(DP)) +1	The memory M(DP) contents are binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	SUB*	Subtract M(DP) from AC	1	0	0	0	1	0	1	1	1	1	1	1	AC, M(DP) ← (AC)+(M(DP)) +1	The memory M(DP) contents are binary-subtracted from the AC contents and the result is loaded to the AC and M(DP).	CF
	ADN	Add M(DP) to AC	1	0	0	0	0	1	0	0	0	1	1	1	AC ← (AC)+(M(DP))	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC.	
	ADN*	Add M(DP) to AC	1	0	0	0	1	1	0	0	0	1	1	1	AC, M(DP) ← (AC)+(M(DP))	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC and M(DP).	
	AND	AND M(DP) to AC	1	0	0	0	0	1	0	1	0	1	1	1	AC ← (AC)∧(M(DP))	The AC contents and memory [M(DP)] contents are ANDed and the result is loaded to the AC.	
	AND*	AND M(DP) to AC	1	0	0	0	1	1	0	1	0	1	1	1	AC, M(DP) ← (AC)∧(M(DP))	The AC contents and memory [M(DP)] contents are ANDed and the result is loaded to the AC and M(DP).	
	EOR	Exclusive OR M(DP) to AC	1	0	0	0	0	1	1	0	1	0	1	1	AC ← (AC)∨(M(DP))	The AC contents and memory [M(DP)] contents are exclusive-ORed and the result is loaded to the AC.	
	EOR*	Exclusive OR M(DP) to AC	1	0	0	0	1	1	1	0	1	0	1	1	AC, M(DP) ← (AC)∨(M(DP))	The AC contents and memory [M(DP)] contents are exclusive-ORed and the result is loaded to the AC and M(DP).	

Instruction	Mnemonic		Instruction code								Bytes	Cycles	Function	Description	Status flag to be affected
			D7	D6	D5	D4	D3	D2	D1	D0					
Operation instructions	OR	OR M(DR) to AC	1	0	0	0	0	1	1	1	1	1	$AC \leftarrow (AC) \vee (M(DP))$	The AC contents and memory [M(DP)] contents are ORed and the result is loaded to the AC.	
	OR*	OR M(DR) to AC	1	0	0	0	1	1	1	1	1	1	$AC, M(DP) \leftarrow (AC) \vee (M(DP))$	The AC contents and memory [M(DP)] contents are ORed and the result is loaded to the AC and M(DP).	
	ADCI X	Add Immediate data to ACC with CF	1	0	0	1	0	0	0	0	2	2	$AC \leftarrow (AC) + X + (CF)$	The AC, CF contents and Immediate data X are binary-added and the result is loaded to the AC.	CF
	SBCI X	Subtract Immediate data from AC with CF	1	0	0	1	0	0	0	1	2	2	$AC \leftarrow (AC) + \bar{X} + (CF)$	Immediate data X is binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	ADDI X	Add Immediate data to AC	1	0	0	1	0	0	1	0	2	2	$AC \leftarrow (AC) + X$	The AC contents and Immediate data X are binary-added and the result is loaded to the AC.	CF
	SUBI X	Subtract Immediate data from AC	1	0	0	1	0	0	1	1	2	2	$AC \leftarrow (AC) + \bar{X} + 1$	Immediate data X is binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	ADNI X	Add Immediate data to AC	1	0	0	1	0	1	0	0	2	2	$AC \leftarrow (AC) + X$	The AC contents and Immediate data X are binary-added and the result is loaded to the AC.	
	ANDI X	AND Immediate data to AC	1	0	0	1	0	1	0	1	2	2	$AC \leftarrow (AC) \wedge X$	The AC contents and Immediate data X are ANDed and the result is loaded to the AC.	
	EORI X	Exclusive OR Immediate data to AC	1	0	0	1	0	1	1	0	2	2	$AC \leftarrow (AC) \oplus X$	The AC contents and Immediate data X are exclusive-ORed and the result is loaded to the AC.	
Data pointer manipulation instructions	ORI X	OR Immediate data to AC	1	0	0	1	0	1	1	1	2	2	$AC \leftarrow (AC) \vee X$	The AC contents and Immediate data X are ORed and the result is loaded to the AC.	
	SDPL	Store AC to DPL	0	0	0	1	1	1	0	0	1	1	$DPL \leftarrow (AC)$	The AC contents are loaded to the DPL.	
	SDPH	Store AC to DPH	0	0	0	1	1	1	0	1	1	1	$DPH \leftarrow (AC)$	The AC contents are loaded to the DPH.	
	EDPL	Exchange DPL with EDPL	0	0	0	1	1	1	1	0	1	1	$(DPL) \rightleftharpoons (EDPL)$	The DPL contents and EDPL contents are exchanged.	
	EDPH	Exchange DPH with EDPH	0	0	0	1	1	1	1	1	1	1	$(DPH) \rightleftharpoons (EDPH)$	The DPH contents and EDPH contents are exchanged.	
	IDPL	Increment DPL	1	0	0	1	1	0	1	0	1	1	$DPL \leftarrow (DPL) + 1$	The DPL contents are incremented +1.	
	DDPL	Decrement DPL	1	0	0	1	1	0	1	1	1	1	$DPL \leftarrow (DPL) - 1$	The DPL contents are decremented -1.	
	IDPH	Increment DPH	1	0	0	1	1	1	0	0	1	1	$DPH \leftarrow (DPH) + 1$	The DPH contents are incremented +1.	
	DDPH	Decrement DPH	1	0	0	1	1	1	0	1	1	1	$DPH \leftarrow (DPH) - 1$	The DPH contents are decremented -1.	
	LDPL	Load AC from DPL	1	1	1	1	1	1	0	1	1	1	$AC \leftarrow (DPL)$	The DPL contents are loaded to the AC.	
	LDPH	Load AC from DPH	1	1	1	1	1	1	1	0	1	1	$AC \leftarrow (DPH)$	The DPH contents are loaded to the AC.	
	MDPL X	Move Immediate data to DPL	1	0	1	1	X3	X2	X1	X0	1	1	$DPL \leftarrow X$	Immediate data X is loaded to the DPL.	
Flag manipulation instructions	MDPH XL	Move Immediate Data to DPH	1	1	0	0	X3	X2	X1	X0	1	1	$DPH \leftarrow X$	Immediate data X is loaded to the DPH.	
	LHLT	Load Halt Release Flag	1	0	1	0	1	0	1	1	1	1	$AC \leftarrow (STS2)$ $STS2 \leftarrow 0$	The STS2 contents are transferred to the AC and then the STS2 is reset.	SCF1-4
	L500	Load AC from STS1	1	0	1	0	1	1	0	0	1	1	$AC \leftarrow (STS1)$ $SCF0 \leftarrow 0$	The STS1 contents are transferred to the AC and then the SCF0 is reset.	SCF0
	CSP	Chrono Stop	0	0	0	0	0	1	0	0	1	1	$CSTF \leftarrow 0$	The CSTF is reset.	CSTF
	CST	Chrono Start	0	0	0	0	0	1	0	1	1	1	$CSTF \leftarrow 1$	The CSTF is set.	CSTF
	RC5	Reset HEF0	0	0	0	0	0	1	1	0	1	1	$HEF0 \leftarrow 0$	The HEF0 is reset so that the halt mode release by an overflow from the predivider is inhibited.	HEF0

Instruction	Mnemonic		Instruction code								Bytes	Cycles	Function	Description	Status flag to be affected			
			D7	D6	D5	D4	D3	D2	D1	D0								
Stack pointer manipulation instructions	SC5	Set HEF0	0	0	0	0	0	1	1	1	1	HEF0 ← 1	The HEF0 is set so that an overflow signal from the predivider releases the halt mode.	HEF0				
	ISP	Increment SP	1	0	0	1	1	1	1	0	1	SP ← (SP)+1	The SP contents are incremented +1.					
	DSP	Decrement SP	1	0	0	1	1	1	1	1	1	SP ← (SP)−1	The SP contents are decremented −1.					
	LSP	Load AC from SP	1	0	1	0	1	0	1	0	1	AC ← (SP)	The SP contents are loaded to the AC.					
	SSP	Store AC to SP	1	0	1	0	1	1	1	0	1	SP ← (AC)	The AC contents are loaded to the SP.					
	MSP X	Move Immediate data to SP	1	1	1	0	X3	X2	X1	X0	1	1	SP ← X	Immediate data X is loaded to the SP.				
Load/store instructions	LDA	Load AC from [M(DP)]	1	0	1	0	1	0	0	1	1	AC ← [M(DP)]	The memory [M(DP)] contents are loaded to the AC.					
	STA	Store AC to [M(DP)]	1	0	1	0	1	1	0	1	1	M(DP) ← (AC)	The AC contents are loaded to the memory M(DP).					
	MVI X	Move Immediate data to M(DP)	0	0	1	0	X3	X2	X1	X0	1	1	M(DP) ← X	Immediate data X is loaded to the memory M(DP).				
	LDI X	Load AC with Immediate data	0	0	1	1	X3	X2	X1	X0	1	1	AC ← X	Immediate data X is loaded to the AC.				
CPU control instructions	HALT	HALT	0	0	0	0	0	0	0	0	1	1	The operation of CPU is stopped. The following condition causes the halt mode to be released. ● The halt release condition specified by the SIC and SC5 instruction is met.					
	SIC X	Set/Reset HALT Release Enable Flag	1	1	0	1	X3	X2	X1	X0	1	1	X0 ← X3	Operation	HEF1 to 4			
													X0=1	The HEF1 is set so that the signal from the predivider releases the halt mode.				
													X1=1	The HEF2 is set so that the rising of signal at input port S releases the halt mode.				
													X2=1	The HEF3 is set so that the rising of signal at input port M releases the halt mode.				
													X3=1	The HEF4 is set so that the 1/10-second pulse releases the halt mode.				
	NOP	No Operation	1	1	1	1	1	1	1	1	1							
	RBAK	Reset Back-up Mode	1	1	1	1	1	0	0	0	1	1	BCF ← 0	The backup mode is released.				
SBAK	Set Back-up Mode	1	1	1	1	1	0	0	1	1	1	BCF ← 1	When powered from Li battery, VSS2 is applied to the logic unit. When powered from Ag. Li battery, EXT-V, the OSC circuit is doubled in inverter size.					
Input/output instructions	IPS	Input Port-S to AC	1	0	1	0	1	1	1	1	1	1	AC ← [P(S)]	The input data at input port S is loaded to the AC.				
	IPM	Input Port-M to AC	1	0	1	0	1	0	0	0	1	1	AC ← [P(M)]	The input data at input port M is loaded to the AC.				
	RLGT	Reset Light	1	1	1	1	0	0	1	0	1	1	LIGHT ← 0	The light output is set to "L" level.				
	SLGT	Set Light	1	1	1	1	0	0	1	1	1	1	LIGHT ← 1	The light output is set to "H" level.				
	SAS X	Set Alarm Sound	1	1	1	1	1	1	0	1	0	2	2	Waveforms specified by X7 to X0 are delivered at the ALM1, ALM2.				
														X7 X6 X5 X4 X3 X2 X1 X0	X7 − X0	X7	X6	
													Control contents	Alarm tone/melody select signal	Octave Control	Musical Scal Control		

Alarm OFF at X3 to X0 = 1

Instruction	Mnemonic	Instruction code								Bytes	Cycles	Function	Description	Status flag to be affected
		D7	D6	D5	D4	D3	D2	D1	D0					
Input/output instructions	RAS	1 1 1 1 1 0 1 0 1 1 1 1 1 1 1 1								2	2	=SAS FF	The ALM1, 2 outputs are set to "L" level	
	SPDR X	1 1 1 1 0 1 X1 X0								1	1	PDF -- X	The pull-down MOS Tr at the corresponding input port is turned ON/OFF.	PDF
												Bit contents	Operation	
												X0=0	S-Terminal Pull down Tr OFF	
												X0=1	S-Terminal Pull down Tr ON	
												X1=0	M-Terminal Pull down Tr OFF	
												X1=1	M-Terminal Pull down Tr ON	
	OUT	1 1 1 1 1 1 0 0								1	1		The AC, memory [M(DP)] contents are loaded to the LCD latch L(SP) directly addressed by the SP.	
		SP=#D Move AC to CTL3										CTL3←(AC)	The AC contents are loaded to the CTL3.	
		SP=#E Write AC to P(P00-03)										P(P0)←(AC)	The AC contents are loaded to the port P0.	
		SP=#F Write AC to P(P10-13)										P(P1)←(AC)	The AC contents are loaded to the port P1.	
	IN	SP=#D Load AC from STS3										AC←(STS3)	The STS3 content is loaded to the AC.	
		SP=#E Input Port-P0 to AC										AC←[P(P0)]	The input data at port P0 is loaded to the AC.	
		SP=#F Input Port-P1 to AC										AC←[P(P1)]	The input data at port P1 is loaded to the AC.	
	TWRT	0 0 0 0 0 0 1 0								1	2		The data of ROM, on current page, addressed by the AC, M(DP) contents is loaded to the LCD latch L(SP) addressed by the SP.	
Jump instructions		SP=#D Read Table data from Program ROM & Write Table data to CTL3											The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the CTL3.	
		SP=#E Read Table data from Program ROM & Write Table data to P (P00 to 03)											The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the port P0.	
		SP=#F Read Table data from Program ROM & Write Table data to P (P10 to 13)											The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the port P1.	
	TMEL	0 0 0 0 0 0 1 1								1	2		The data of ROM, on current page, addressed by the AC, M(DP) contents is set to alarm sound data and waveforms specified by the table data are delivered at ALM1, 2. (Same as SAS instruction)	
	JMP X	0 0 0 0 1 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0	The data specified by X10 to X0 is loaded to the PC to cause an unconditional jump.	
	BAB0 X	0 1 0 0 1 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if AC0=[1]	If bit 0 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB1 X	0 1 0 1 1 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if AC1=[1]	If bit 1 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB2 X	0 1 1 0 1 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if AC2=[1]	If bit 2 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB3 X	0 1 1 1 1 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if AC3=[1]	If bit 3 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BANZ X	0 1 0 1 0 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if AC=0	If the AC is not "0", a jump occurs. If "0", the PC is incremented +1.	
	BAZ X	0 1 0 0 0 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if AC=0	If the AC is "0", a jump occurs. If not "0", the PC is incremented +1.	
	BCNH X	0 1 1 0 0 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if CF=1	If the CF is "0", a jump occurs. If "1", the PC is incremented +1.	
	BCH X	0 1 1 1 0 X0 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0								2	2	PC10←PC0←X10←X0 if CF=1	If the CF is "1", a jump occurs. If "0", the PC is incremented +1.	

Instruction	Mnemonic		Instruction code								Bytes	Cycles	Function	Description	Status flag to be affected
			D7	D6	D5	D4	D3	D2	D1	D0					
Jump instructions	PAGE	Page Set	0	0	0	1	0	0	0	1	1	1	PAGE ← [M(DP)]	The memory [M(DP)] contents are loaded to the PAGE latch.	
	JMP*	Jump to the Address modified by PAGE AC and M(DP)	0	0	0	1	0	0	0	0	1	1	PC10-PC8←(PAGE) PC7-PC4←(AC) PC3-PC0←[M(DP)]	An unconditional jump occurs to a page specified by the PAGE and an address low-order 8 bits of the PC which are loaded with the AC and memory M(DP) contents.	
Subroutine instructions	JSR X	Jump Subroutine	1	0	1	0	0	X10	X9	X8	2	2	STACK ← PC+2 PC10-PC0←X10-X0	A subroutine is called.	
	RTS	Return from Subroutine	0	0	0	1	0	0	1	1	1	1	PC ← (STACK)	A return from a subroutine occurs.	
Other instructions	MPCL	Move PC0 - PC3 to M(DP)	0	0	0	1	0	1	0	0	1	1	M(DP)←PC3-PC0	The contents of the low-order 4 bits of the PC are stored in the memory M(DP).	
	MPCM	Move PC4 - PC7 to M(DP)	0	0	0	1	0	1	0	1	1	1	M(DP)←PC7-PC4	The contents of the medium-order 4 bits of the PC are stored in the memory M(DP).	
	MPCH	Move PC8 - PC10 to M(DP)	0	0	0	1	0	1	1	0	1	1	M(DP)←PC10-PC8	The contents of the high-order 3 bits of the PC are stored in the memory M(DP).	
	CSEC	Clear SEC Counter	1	1	1	1	1	0	1	1	1	1		The high-order 5 bits of the predivider are reset and the SCF0, SCF1, SCF4 are reset.	SCF0 SCF1 SCF4

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