

**SANYO**

No. 2412A

**LC6568D, 6568H****8K-Byte ROM-Contained Single-Chip 4-Bit Microcomputers  
with FLT/LED Drivers, Comparator Input**

The LC6568D/H are single-chip 4-bit microcomputers that contain an 8K-byte ROM, 1K-bit RAM, and have 64 pins. The LC6568D/H have 57 pins for ports — 28 pins for 7 input/output common ports, 21 pins for 6 output ports, and 8 pins for 2 input ports. The LC6568D/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function and burst pulse output function. Each of the 28 pins for input/output common ports contains a driver with a withstand voltage of 15V max. and a drive current of 15mA max. and each of the 21 pins for output ports contains a high-voltage output driver of the P-channel open drain type. Since the high-voltage output driver can be used as general-purpose high-current driver as well as fluorescent tube driver, the LC6568D/H can be also widely used in applications where no fluorescent display is provided.

The LC6568D/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and also made easier-to-use in the standby function.

#### Features

- Instruction set with 81 instructions (Common to the LC6500 series)
- On-chip 8192-byte ROM, 1024-bit RAM
- Instruction cycle time: 2.77  $\mu$ s (D version,  $V_{DD} = 4$  to 6V)  
0.92  $\mu$ s (H version,  $V_{DD} = 4.5$  to 6V)
- Serial input/output interface x 1 (4 bits/8 bits program-selectable)
- I/O ports: 57 pins in all
  - Input ports 8 pins
  - Input/output common ports 28 pins: 15V max., 15mA max., LED drivable, pull-up resistance option available
  - Output ports 21 pins:  $V_{DD}$ -45V withstand voltage, FLT drivable, common with general-purpose output, pull-down resistance option available
- Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.
- Interrupt function
  - Timer interrupt: 1 line
  - INT0 to 3 pin or serial I/O interrupt: 1 line
- Stack level: 8 levels (Common with interrupt)
- Timer: 4-bit prescaler +8-bit programmable timer
- Burst pulse (64 x cycle time, duty 50%) output function
- Oscillator option
  - Circuit mode: Ceramic resonator mode, RC mode, external clock mode (384kHz to 4.33MHz)
  - Predivider option: 1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction. Provides the function to absorb the OSC stabilizing time in the ceramic resonator mode.
- Supply Voltage: 4 to 6V (D version)  
4.5 to 6V (H version)
- Package: DIP 64 shrink type, QIP64A
- Evaluation LSI: LC6595 (Evaluation chip) + EVA800-TB6568 (Evaluation chip board),  
LC65PG68 (Piggyback)
- 4-channel comparator input
- 4-channel external interrupt input (1 vector)

## Development Support Tools

The following development tools are available.

1. Document support ..... (1) Documentation LC6568 User's Manual  
(2) Development Tools User's Manual, EVA800-LC6568
2. Software support ..... (1) MS-DOS (Note) for the host system and cross-assembler software  
i. Host processor control program  
ii. LC65S.EXE cross assembler
3. Hardware support ..... (1) Evaluation chip: LC6595  
(2) Piggyback microcomputer: LC65PG68  
(3) Emulator: EVA-800 or EVA-850 emulator and evaluation boards

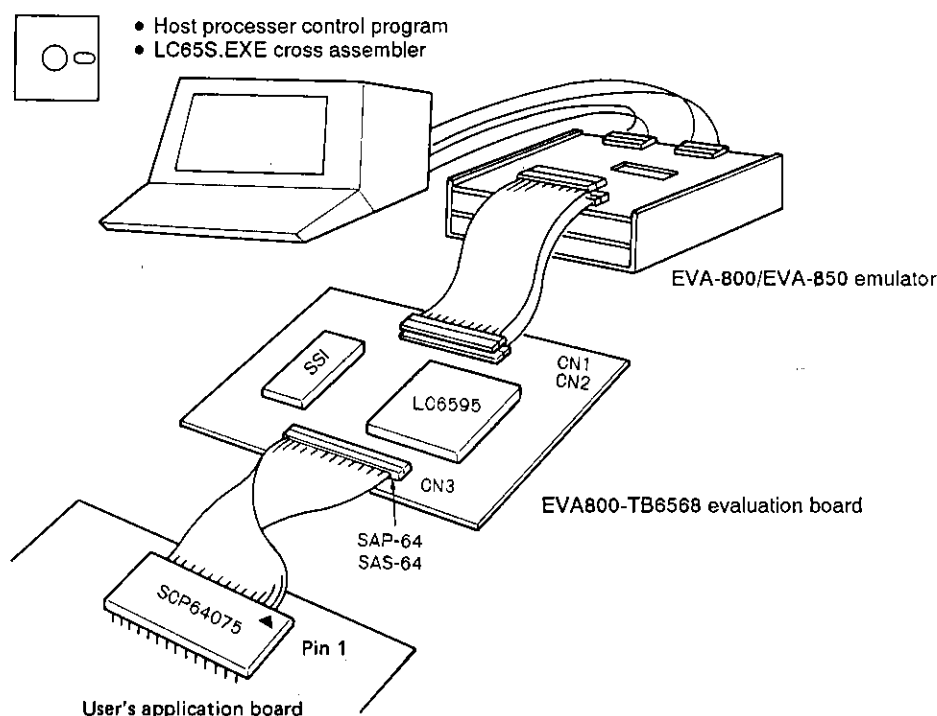


Fig. 1 Appearance of Development Support System

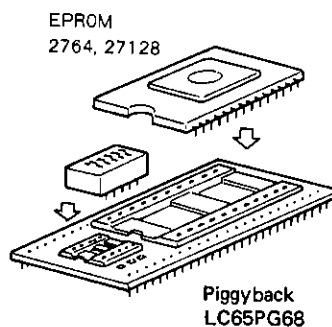
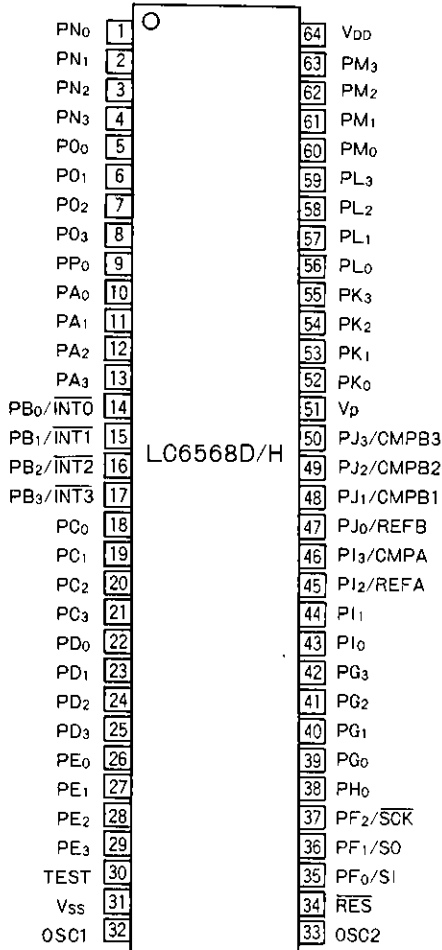


Fig. 2 Piggyback (For Program Evaluation)

(Note) MS-DOS is a registered trademark of Microsoft Corporation

Pin Assignment



OSC1, OSC2 : C, R, or ceramic resonator oscillator for OSC

PA<sub>0</sub> to 3 : Port for input only A<sub>0</sub>-3

PB<sub>0</sub> to 3 : Port for input only B<sub>0</sub>-3

PC<sub>0</sub> to 3 : Input/output common port C<sub>0</sub>-3

PD<sub>0</sub> to 3 : Input/output common port D<sub>0</sub>-3

PE<sub>0</sub> to 3 : Input/output common port E<sub>0</sub>-3

PF<sub>0</sub> to 3 : Input/output common port F<sub>0</sub>-3

PG<sub>0</sub> to 3 : Input/output common port G<sub>0</sub>-3

PH<sub>0</sub> : Input/output common port H<sub>0</sub>

PI<sub>0</sub> to 3 : Input/output common port I<sub>0</sub>-3

PJ<sub>0</sub> to 3 : Input/output common port J<sub>0</sub>-3

PK<sub>0</sub> to 3 : Port for output only K<sub>0</sub>-3

PL<sub>0</sub> to 3 : Port for output only L<sub>0</sub>-3

PM<sub>0</sub> to 3 : Port for output only M<sub>0</sub>-3

PN<sub>0</sub> to 3 : Port for output only N<sub>0</sub>-3

PO<sub>0</sub> to 3 : Port for output only O<sub>0</sub>-3

PP<sub>0</sub> : Port for output only P<sub>0</sub>

SI : 4-bit/8-bit serial input port

S0 : 4-bit/8-bit serial output port

SCK : Input/output for serial clock

INT<sub>0</sub> to 3 : Interrupt request input

V<sub>p</sub> : V<sub>p</sub> pin

RES : Reset

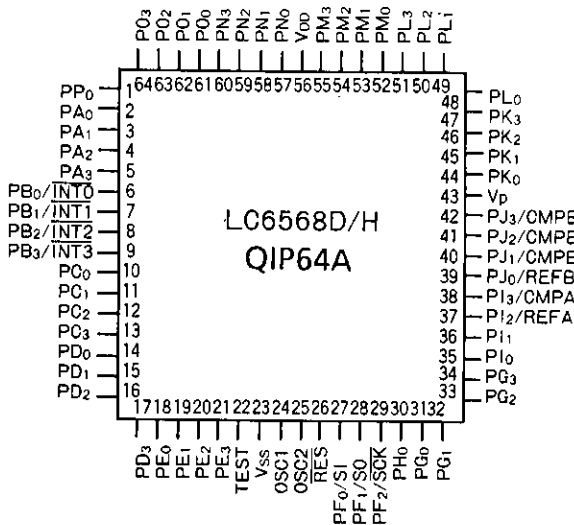
TEST : Test

CMPA : Comparator A input pin

CMPB1 to 3 : Comparator B1 to 3 input pins

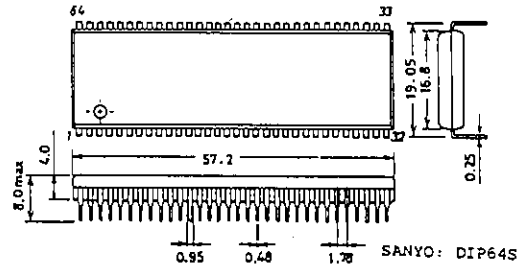
REFA : Comparator A reference voltage input pin

REFB : Comparator B reference voltage input pin

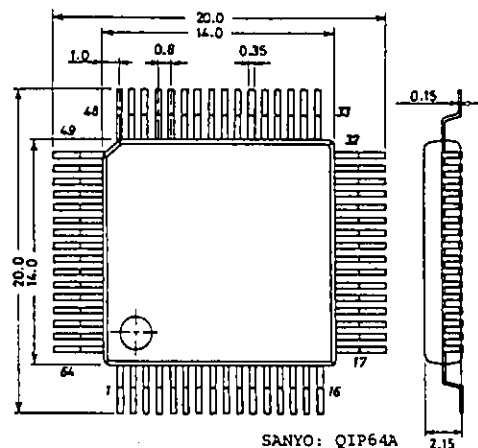


Note: When mounting the QIP version on the board, do not dip it in solder.

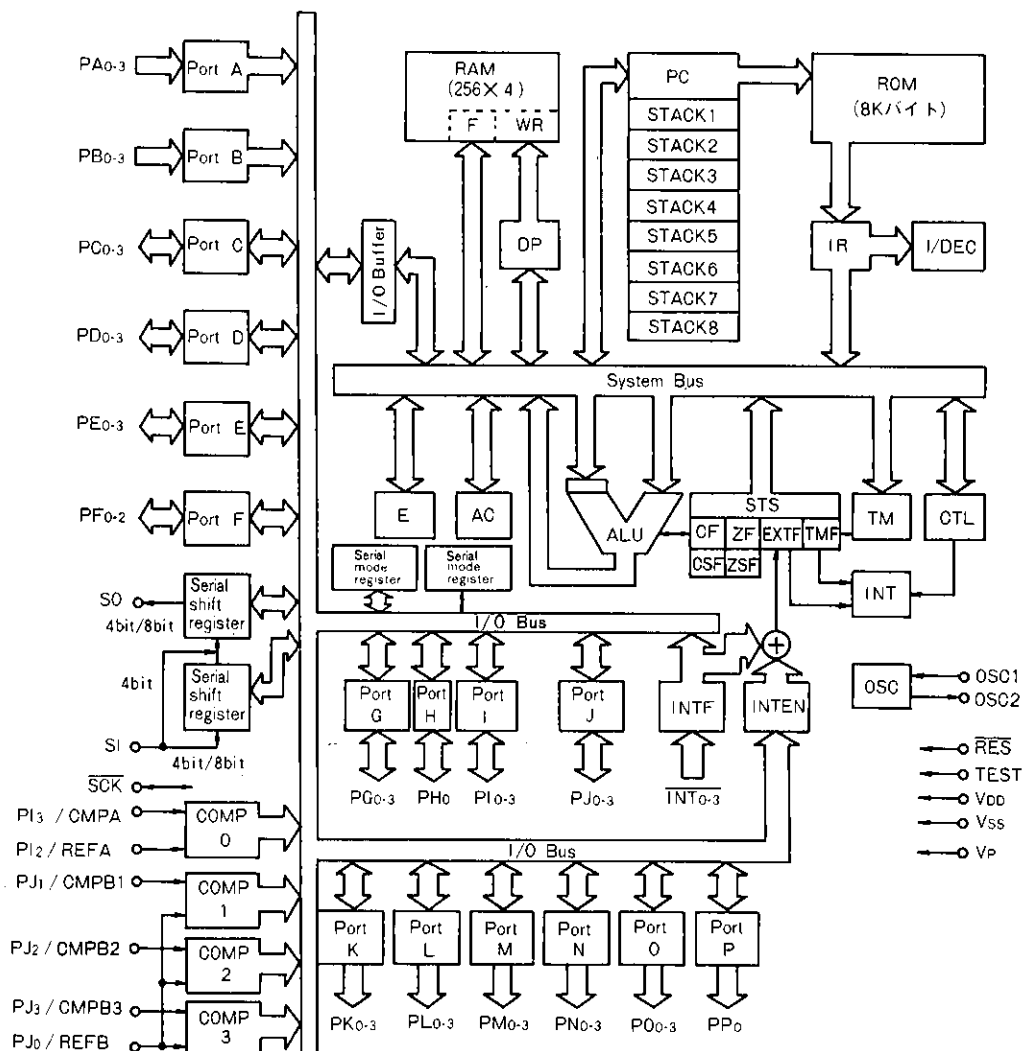
Package Dimensions 3071-D64IC  
(unit: mm)



Package Dimensions 3057-Q64AIC  
(unit: mm)



# System Block Diagram



RAM	: Data memory	ROM	: Program memory
F	: Flag	PC	: Program counter
WR	: Working register	INT	: Interrupt control
AC	: Accumulator	IR	: Instruction register
ALU	: Arithmetic and logic unit	I/DEC	: Instruction decoder
DP	: Data pointer	CF, CSF	: Carry flag, carry save flag
E	: E register	ZF, ZSF	: Zero flag, zero save flag
CTL	: Control register	EXTF	: External interrupt request
OSC	: Oscillator	TMF	: Internal interrupt request
TM	: Timer	INTF	: Interrupt request flag
STS	: Status register	INTEN	: Interrupt enable flag

(Note) SI, SO, SCK: Common to PF<sub>0</sub> to PF<sub>2</sub>  
INT<sub>0</sub> to INT<sub>3</sub>: Common to PB<sub>0</sub> to PB<sub>3</sub>  
 REFA, COMPA or PI<sub>2</sub>, PI<sub>3</sub> port: Option-selectable  
 REFB, CMPB<sub>1</sub> to CMPB<sub>3</sub> or PJ<sub>0</sub> to PJ<sub>3</sub> port: Option-selectable

## Pin Description

Pin Name	Pins	I/O	Functions	Options	During Reset
V <sub>DD</sub> V <sub>SS</sub>	1 1	—	Power supply	—	—
OSC1	1	Input	<ul style="list-style-type: none"> <li>Pin for externally connecting R, C or a ceramic resonator for system clock generation.</li> <li>For the external clock mode, the OSC2 pin is open.</li> </ul>	(1) External clock input (2) 2-pin RC OSC (3) 2-pin ceramic resonator OSC (4) Predivider option 1: No predivider 2: 1/3 predivider 3: 1/4 predivider	—
OSC2	1	Output			
PA <sub>0</sub> PA <sub>1</sub> PA <sub>2</sub> PA <sub>3</sub>	4	Input	<ul style="list-style-type: none"> <li>Input port A<sub>0</sub> to 3 (Low-threshold input)</li> <li>4-bit input (IP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> </ul>	—	—
PB <sub>0</sub> /INT <sub>0</sub> PB <sub>1</sub> /INT <sub>1</sub> PB <sub>2</sub> /INT <sub>2</sub> PB <sub>3</sub> /INT <sub>3</sub>	4	Input	<ul style="list-style-type: none"> <li>Input port B<sub>0</sub> to 3</li> <li>4-bit input (IP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Standby is controlled by the PB<sub>3</sub>.</li> <li>The PB<sub>3</sub> pin must be free from chattering during the HALT instruction execution cycle.</li> <li>PB<sub>0</sub> to 3: Common with INT<sub>0</sub> to 3</li> <li>Program-selectable (1 interrupt vector, 4 senses)</li> </ul>	—	<ul style="list-style-type: none"> <li>Individual interrupt flag (INT<sub>0</sub>F to INT<sub>3</sub>F): Reset</li> <li>Individual interrupt enable flag (INT<sub>0</sub>EN to INT<sub>3</sub>EN): Disable mode</li> </ul>
PC <sub>0</sub> PC <sub>1</sub> PC <sub>2</sub> PC <sub>3</sub>	4	Input/Output	<ul style="list-style-type: none"> <li>Input/output common port C<sub>0</sub> to 3.</li> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> <li>Output ("H" or "L") during reset may be specified by option.</li> </ul>	(1) Open drain type output (2) With pull-up resistance (3) Output during reset: "H" (4) Output during reset: "L" <ul style="list-style-type: none"> <li>(1), (2): Specified bit by bit.</li> <li>(3), (4): Specified in a group of 4 bits.</li> </ul>	<ul style="list-style-type: none"> <li>"H" output</li> <li>"L" output (Option-selectable)</li> </ul>
PD <sub>0</sub> PD <sub>1</sub> PD <sub>2</sub> PD <sub>3</sub>	4	Input/Output	<ul style="list-style-type: none"> <li>Input/output common port D<sub>0</sub> to 3.</li> <li>The functions, options are the same as for the PC<sub>0</sub> to 3.</li> </ul>	Same as for the PC <sub>0</sub> to 3.	Same as for the PC <sub>0</sub> to 3.
PE <sub>0</sub> PE <sub>1</sub> PE <sub>2</sub> PE <sub>3</sub>	4	Input/Output	<ul style="list-style-type: none"> <li>Input/output common port E<sub>0</sub> to 3.</li> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> <li>PE<sub>0</sub>: With burst pulse (64T<sub>cyc</sub>) output function</li> </ul>	(1) Open drain type output (2) With pull-up resistance (1), (2): Specified bit by bit.	"H" output

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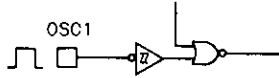
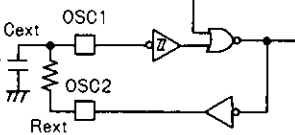
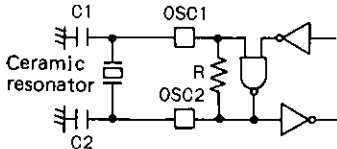
Pin Name	Pins	I/O	Functions	Options	During Reset
PF <sub>0</sub> /SI PF <sub>1</sub> /SO PF <sub>2</sub> /SCK	3	Input/ Output	<ul style="list-style-type: none"> <li>Input/output port F<sub>0</sub> to 2 The functions, options are the same as for the PE<sub>0</sub> to 3. However, no burst pulse output function is provided.</li> <li>PF<sub>0</sub> to 2: Also used for serial interface. Program-selectable. SI: Serial input port SO: Serial output port SCK: Serial clock input/output</li> </ul>	Same as for the PE <sub>0</sub> to 3.	Sample as for the PE <sub>0</sub> to 3. Serial port: Disable
PG <sub>0</sub> PG <sub>1</sub> PG <sub>2</sub> PG <sub>3</sub>	4	Input/ Output	<ul style="list-style-type: none"> <li>Input/output common port G<sub>0</sub> to 3. The functions, options are the same as for the PE<sub>0</sub> to 3. However, no burst pulse output function is provided.</li> </ul>	Same as for the PE <sub>0</sub> to 3.	Same as for the PE <sub>0</sub> to 3.
PH <sub>0</sub>	1	Input/ Output	<ul style="list-style-type: none"> <li>Input/output common port H<sub>0</sub>. The functions, options are the same as for the PG<sub>0</sub> to 3. This port consists of a single bit.</li> </ul>	Same as for the PG <sub>0</sub> to 3.	Same as for the PG <sub>0</sub> to 3.
PI <sub>0</sub> PI <sub>1</sub> PI <sub>2</sub> /REFA PI <sub>3</sub> /CMPA	4	Input/ Output	<ul style="list-style-type: none"> <li>Input/output common port I<sub>0</sub> to 3. (Port input/output option selected mode) The functions, options are the same as for the PG<sub>0</sub> to 3.</li> </ul>	Same as for the PG <sub>0</sub> to 3.	Same as for the PG <sub>0</sub> to 3.
	2	Input	<ul style="list-style-type: none"> <li>Comparator input option selected mode REFA: Comparator reference voltage input CMPA: Comparator input</li> </ul>		
PJ <sub>0</sub> /REFB PJ <sub>1</sub> /CMPB <sub>1</sub> PJ <sub>2</sub> /CMPB <sub>2</sub> PJ <sub>3</sub> /CMPB <sub>3</sub>	4	Input/ Output	<ul style="list-style-type: none"> <li>Input/output common port J<sub>0</sub> to 3. (Port input/output option selected mode) The functions, options are the same as for the PG<sub>0</sub> to 3.</li> </ul>	Same as for the PG <sub>0</sub> to 3.	Same as for the PG <sub>0</sub> to 3.
	4	Input	<ul style="list-style-type: none"> <li>Comparator input option selected mode REFB: Common reference voltage input for CMPB<sub>1</sub> to 3 CMPB<sub>1</sub> to 3: Comparator input</li> <li>4-bit input together with CMPA (BANK IP)</li> <li>Single-bit decision (BANK BP, BNP) (at DPL = 9)</li> </ul>		

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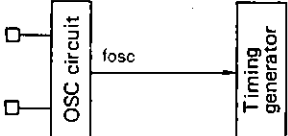
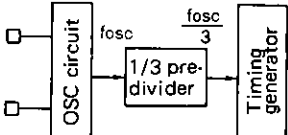
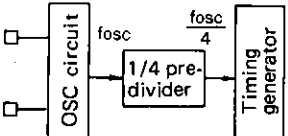
Pin Name	Pins	I/O	Functions	Options	During Reset
PK <sub>0</sub> PK <sub>1</sub> PK <sub>2</sub> PK <sub>3</sub>	4	Output	<ul style="list-style-type: none"> <li>Output port K<sub>0</sub> to 3 (Segment driver output)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> </ul>	(1) Open drain type output (2) With pull-down resistance • (1), (2): Specified bit by bit.	"L" output
PL <sub>0</sub> PL <sub>1</sub> PL <sub>2</sub> PL <sub>3</sub>	4	Output	<ul style="list-style-type: none"> <li>Output port L<sub>0</sub> to 3 (Segment driver output)</li> </ul> The functions, options are the same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
PM <sub>0</sub> PM <sub>1</sub> PM <sub>2</sub> PM <sub>3</sub>	4	Output	<ul style="list-style-type: none"> <li>Output port M<sub>0</sub> to 3 (Digit driver Output)</li> </ul> The functions, options are the same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
PN <sub>0</sub> PN <sub>1</sub> PN <sub>2</sub> PN <sub>3</sub>	4	Output	<ul style="list-style-type: none"> <li>Output port N<sub>0</sub> to 3 (Digit driver output)</li> </ul> The functions, options are the same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
PO <sub>0</sub> PO <sub>1</sub> PO <sub>2</sub> PO <sub>3</sub>	4	Output	<ul style="list-style-type: none"> <li>Output port O<sub>0</sub> to 3 (Digit driver output)</li> </ul> The functions, options are the same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
PP <sub>0</sub>	1	Output	<ul style="list-style-type: none"> <li>Output port P<sub>0</sub> (Digit driver output)</li> </ul> The functions, options are the same as for the PK <sub>0</sub> to 3. This port consists of a single bit.	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
$\overline{\text{RES}}$	1	Input	<ul style="list-style-type: none"> <li>System reset input</li> <li>For power-up reset, "L" level is applied for 4 clock cycles or more.</li> </ul>	—	—
TEST	1	Input	<ul style="list-style-type: none"> <li>LSI test pin</li> </ul> Normally connected to V <sub>SS</sub>	—	—
V <sub>p</sub>	1	—	<ul style="list-style-type: none"> <li>Power supply pin for pull-down resistance</li> </ul>	—	—

### Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. External Clock		<ul style="list-style-type: none"> <li>Input: Schmitt type.</li> </ul>
2. 2-pin RC OSC		<ul style="list-style-type: none"> <li>Input: Schmitt type.</li> </ul>
3. Ceramic Resonator OSC		

(Note) High-speed version: Ceramic resonator OSC option or external clock option only

### Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider		<ul style="list-style-type: none"> <li>Applicable to all of 3 OSC options.</li> <li>The OSC frequency, external clock do not exceed 1444 kHz. (LC6568D)</li> <li>The OSC frequency, external clock do not exceed 4330 kHz. (LC6568H)</li> <li>Refer to Table of OSC, Predivider Option (Table 2).</li> </ul>
2. 1/3 predivider		<ul style="list-style-type: none"> <li>Applicable to only 2 options of external clock, ceramic resonator OSC.</li> <li>The OSC frequency, external clock do not exceed 4330 kHz.</li> <li>Refer to Table of OSC, Predivider Option (Table 2).</li> </ul>
3. 1/4 predivider		<ul style="list-style-type: none"> <li>Applicable to only 2 options of external clock, ceramic resonator OSC.</li> <li>The OSC frequency, external clock do not exceed 4330 kHz.</li> <li>Refer to Table of OSC, Predivider Option (Table 2).</li> </ul>



### Options of Ports C, D Output Level during Reset

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports C, D
2. Output during reset: "L" level	All of 4 bits of ports C, D

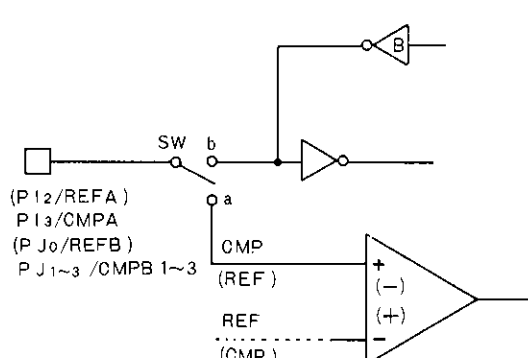
### Options of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (bitwise).

Option Name	Circuit	Applicable Ports
1. Open drain type output		Ports C, D, E, F, G, H, I, J
		Ports K, L, M, N, O, P
2. Output with pull-up resistance		Ports C, D, E, F, G, H, I, J (Note) Not applicable to PI2/REFA, PI3/CMFA, PJ0/REFA, PJ1 to 3/CMP1 to 3 ports at the comparator input function option selected mode
3. Output with pull-down resistance		Ports K, L, M, N, O, P

Port input/output	Option
Comparator input	

- For six ports of PI<sub>2</sub>/REFA, PI<sub>3</sub>/CMPA, PJ<sub>0</sub>/REFB, PJ<sub>1</sub>/CMPB1, PJ<sub>2</sub>/CMPB2, PJ<sub>3</sub>/CMPB3, either of the two options – port input/output, comparator input – may be selected. (Note)
- Selection between port input/output and comparator input may be made in bit units.
  - Port input/output
  - Comparator input

Pin	Circuit Configuration	Conditions, etc.						
PI <sub>2</sub> /REFA PI <sub>3</sub> /CMPA PJ <sub>0</sub> /REFB PJ <sub>1</sub> /CMPB1 PJ <sub>2</sub> /CMPB2 PJ <sub>3</sub> /CMPB3	 <p>(PI<sub>2</sub>/REFA) (PI<sub>3</sub>/CMPA) (PJ<sub>0</sub>/REFB) PJ<sub>1~3</sub> /CMPB 1~3</p> <p>SW b a CMP (REF) REF (CMP)</p> <table><tr><th>Option</th><th>SW</th></tr><tr><td>Port input/output option</td><td>b</td></tr><tr><td>Comparator input option</td><td>a</td></tr></table>	Option	SW	Port input/output option	b	Comparator input option	a	Selection of (b) port input/output option permits either of the two port output type options (OD, PU) to be selected.
Option	SW							
Port input/output option	b							
Comparator input option	a							

(Note) Selection of option for PI<sub>3</sub>/CMPA provides automatic selection of option for PI<sub>2</sub>/REFA.  
 Selection of option for PJ<sub>1</sub>/CMPB1, PJ<sub>2</sub>/CMPB2, PJ<sub>3</sub>/CMPB3 provides automatic selection of option for PJ<sub>0</sub>/REFB.

## LC6568D

1. Absolute Maximum Ratings/ $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ 

			min	typ	max	unit
Maximum Supply Voltage	$V_{DD}$ max		$V_{DD}$	−0.3	+7.0	V
Output Voltage	$V_O(1)$		OSC2	Allowable up to voltage generated		V
	$V_O(2)$		Port K, L, M, N, O, P0	$V_{DD}-45$	$V_{DD}+0.3$	V
Input Voltage	$V_I(1)$		OSC1 (Note 1)	−0.3	$V_{DD}+0.3$	V
	$V_I(2)$		TEST, $\overline{\text{RES}}$			
	$V_I(3)$		Port A, B	−0.3	+15	V
Input/Output Voltage	$V_{IO}(1)$		$V_p$	$V_{DD}-45$	$V_{DD}+0.3$	V
	$V_{IO}(2)$		Port of OD type (Port C, D, E, F0 to F2, G, H0, I, J)	−0.3	+15	V
			Port of PU type (Port C, D, E, F0 to F2, G, H0, I, J)	−0.3	$V_{DD}+0.3$	V
Peak Output Current	$I_{OP}(1)$		Port C, D, E, F0 to F2, G, H0, I, J	−2	+15	mA
	$I_{OP}(2)$		Port K, L	−10	0	mA
	$I_{OP}(3)$		Port M, N, O, P0	−30	0	mA
Allowable Power Dissipation	$P_d$ max	$T_a = -30$ to $+70^\circ\text{C}$	DIP 64S		600	mW
			QIP 64		430	mW
Operating Temperature	$T_{opr}$			−30	+70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$			−55	+125	$^\circ\text{C}$
Average Output Current	$I_{OA}(1)$	Per pin over the period of 100msec.	Port C, D, E, F0 to F2, G, H0, I, J	−2	+15	mA
	$I_{OA}(2)$	Per pin over the period of 100msec.	Port K, L	−10	0	mA
	$I_{OA}(3)$	Per pin over the period of 100msec.	Port M, N, O, P0	−30	0	mA
	$\Sigma I_{OA}(1)$	Total current of PC0 to 3, PD0 to 3, PE0 to 3 (Note 2)		−30	+50	mA
	$\Sigma I_{OA}(2)$	Total current of PF0 to 2, PG0 to 3, PH0, PI0 to 3, PJ0 to 3 (Note 2)		−30	+50	mA
	$\Sigma I_{OA}(3)$	Total current of PK0 to 3, PL0 to 3, PM0 to 3 (Note 2)		−50	0	mA
	$\Sigma I_{OA}(4)$	Total current of PN0 to 3, PO0 to 3, PP0 (Note 2)		−50	0	mA

2. Allowable Operating Conditions/ $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{DD} = 4.0$  to  $6.0\text{V}$   
unless otherwise specified

			min	typ	max	unit
Operating Supply Voltage	$V_{DD}$		$V_{DD}$	4.0	6.0	V
Standby Supply Voltage	$V_{ST}$	RAM, register hold (Note 3)	$V_{DD}$	1.8	6.0	V
"H"-Level Input Voltage	$V_{IH}(1)$		Port A	1.9	+13.5	V
	$V_{IH}(2)$	Output Nch Tr OFF	Port of OD type (Port C to J)	$0.7V_{DD}$	+13.5	V
	$V_{IH}(3)$	Output Nch Tr OFF	Port of PU type (Port C to J)	$0.7V_{DD}$	$V_{DD}$	V
	$V_{IH}(4)$	Output Nch Tr OFF	SCK, SI of OD type	$0.8V_{DD}$	+13.5	V

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				min	typ	max	unit
“H”-Level Input Voltage	V <sub>IH</sub> (5)	Output Nch Tr OFF	SCK, SI of PU type	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH</sub> (6)	Fig. 7	High V <sub>t</sub> input circuit of Port B <sub>3</sub>	V <sub>DD</sub> −0.5		+13.5	V
	V <sub>IH</sub> (7)	Fig. 7	Low V <sub>t</sub> input circuit of Port B <sub>3</sub>	0.5V <sub>DD</sub>		+13.5	V
	V <sub>IH</sub> (8)	Fig. 3	V <sub>DD</sub> : 1.8 to 6.0V	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH</sub> (9)		PB <sub>0</sub> to 2, INT <sub>0</sub> to 3	0.8V <sub>DD</sub>		+13.5	V
“L”-Level Input Voltage	V <sub>IH</sub> (10)	External clock mode	OSC1	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IL</sub> (1)		PA <sub>0</sub> to 3	V <sub>SS</sub>		+0.5	V
	V <sub>IL</sub> (2)		PC to PJ, TEST	V <sub>SS</sub>		0.3V <sub>DD</sub>	V
	V <sub>IL</sub> (3)		PB <sub>0</sub> to 2, SCK, SI, INT <sub>0</sub> to 3	V <sub>SS</sub>		0.25V <sub>DD</sub>	V
	V <sub>IL</sub> (4)		RES	V <sub>SS</sub>		0.25V <sub>DD</sub>	V
	V <sub>IL</sub> (5)	Fig. 7	PB <sub>3</sub>	V <sub>SS</sub>		0.9	V
	V <sub>IL</sub> (6)	Fig. 7	V <sub>DD</sub> : 1.8 to 6.0V	V <sub>SS</sub>		0.3	V
Operating Frequency (Cycle Time)	V <sub>IL</sub> (7)	External clock mode	OSC1	V <sub>SS</sub>		0.25V <sub>DD</sub>	V
	f <sub>op</sub>		OSC1	384		1444	kHz
Ceramic Resonator Oscillation Constants	(TCYC)		OSC2	(10.4)		(2.77)	(μS)
			OSC1	See Fig. 1, Table 1.			
External Clock Conditions				OSC2			
Frequency	f <sub>EXT</sub>		OSC1 (Fig. 4)	See Table 2.			
“H”-Level/“L”-Level Clock Pulse Width	t <sub>EXTH</sub> /t <sub>EXTL</sub>		OSC1 (Fig. 4)	90	ns		
Rise/Fall Time	t <sub>EXTR</sub> /t <sub>EXTF</sub>		OSC1 (Fig. 4)		30	ns	
2-pin RC Oscillation							
External Capacitance	C <sub>EXT</sub>		OSC1, OSC2 (Fig. 9)	220±5%	pF		
External Resistance	R <sub>EXT</sub>		OSC1, OSC2 (Fig. 9)	6.8±1%	kΩ		

**3. Electrical Characteristics/T<sub>a</sub> = −30 to +70°C, V<sub>SS</sub> = 0V, V<sub>DD</sub> = 4.0 to 6.0V**

				min	typ	max	unit
unless otherwise specified							
“H”-Level Input Current	I <sub>IH</sub> (1)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr)	Port of OD type (Port C to J)			+5.0	μA
		V <sub>IN</sub> =+13.5V	Port A, B				
	I <sub>IH</sub> (2)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr)	Port of PU type (Port C to J)			+1.0	μA
“L”-Level Input Current	I <sub>IL</sub> (1)	V <sub>IN</sub> =V <sub>DD</sub> Output Nch Tr OFF	OSC1 (External clock mode)				
		V <sub>IN</sub> =V <sub>SS</sub>	Port of OD type (Port C to J)	−1.0			μA
	I <sub>IL</sub> (2)	Output Nch Tr OFF	Port of PU type (Port C to J)	−1.3	−0.35		mA
“H”-Level Output Voltage	I <sub>IL</sub> (3)	V <sub>IN</sub> =V <sub>SS</sub>	RES	−45	−10		μA
	V <sub>OH</sub> (1)	I <sub>OH</sub> =−50μA	Port of PU type (Port C to J)	V <sub>DD</sub> −1.2			V
	V <sub>OH</sub> (2)	I <sub>OH</sub> =−3mA	Port K, L	V <sub>DD</sub> −1.8			V
	V <sub>OH</sub> (3)	I <sub>OH</sub> =−15mA	Port M, N, O, P <sub>0</sub>	V <sub>DD</sub> −1.8			V

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## LC6568D

				min	typ	max	unit
“L”-Level Output Voltage	VOL(1)	I <sub>OL</sub> =10mA, Other ports: ΣI <sub>OL</sub> max	Port C, D, E, F <sub>0</sub> to F <sub>2</sub> , G, H <sub>0</sub> , I, J			1.5	V
	VOL(2)	I <sub>OL</sub> =2mA, Each port: I <sub>OL</sub> =2mA	Port C, D, E, F <sub>0</sub> to F <sub>2</sub> , G, H <sub>0</sub> , I, J			0.5	V
	VOL(3)	V <sub>p</sub> =-35V, Output Pch Tr OFF Output open	Port of PD type (Port K to P)			-33	V
Output OFF Leakage Current	I <sub>OFF</sub> (1)	Output Pch Tr OFF V <sub>OUT</sub> =V <sub>DD</sub>	Port of OD type (Port K to P)			+30	μA
	I <sub>OFF</sub> (2)	Output Pch Tr OFF V <sub>OUT</sub> =V <sub>DD</sub> -40V	Port of OD type (Port K to P)	-30			μA
Hysteresis Voltage	V <sub>HYS</sub>		RES, INT <sub>0</sub> to 3 SCK, SI, OSC1 of Schmitt type (Note 5)	0.1V <sub>DD</sub>			V
Pull-up Resistance	R <sub>PP</sub>	V <sub>DD</sub> : 5.0V	Port of PU type (Port C to J)		14		kΩ
Pull-down Resistance	R <sub>PD</sub>	V <sub>DD</sub> : 5.0V	Port of PD type (Port K to P)	50		200	kΩ
Current Dissipation	Operation mode, Output Nch Tr, Pch Tr OFF, V <sub>IN</sub> =V <sub>DD</sub>						
2-Pin RC Oscillation Mode	I <sub>DDOP</sub> (1)	Fig. 9 f <sub>osc</sub> =750kHz (typ)	V <sub>DD</sub>		2.5	8	mA
Ceramic Resonator	I <sub>DDOP</sub> (2)	Fig. 1 4MHz, 1/3 predivider	V <sub>DD</sub>		8	15	mA
Oscillation Mode	I <sub>DDOP</sub> (3)	Fig. 1 4MHz, 1/4 predivider	V <sub>DD</sub>		8	15	mA
	I <sub>DDOP</sub> (4)	Fig. 1 3MHz, 1/3 predivider	V <sub>DD</sub>		6.5	14	mA
	I <sub>DDOP</sub> (5)	Fig. 1 3MHz, 1/4 predivider	V <sub>DD</sub>		6.5	14	mA
	I <sub>DDOP</sub> (6)	Fig. 1 400kHz	V <sub>DD</sub>		1.0	4.5	mA
	I <sub>DDOP</sub> (7)	Fig. 1 800kHz	V <sub>DD</sub>		2.0	6	mA
External Clock Mode	I <sub>DDOP</sub> (8)	384kHz to 1444kHz, 1/1 predivider	V <sub>DD</sub>		3.5	9	mA
		1152kHz to 4330kHz, 1/3 predivider	V <sub>DD</sub>		8	15	mA
		1536kHz to 4330kHz, 1/4 predivider	V <sub>DD</sub>		8	15	mA
Standby Mode	I <sub>DDST</sub>	V <sub>IN</sub> =V <sub>DD</sub> Output Nch Tr OFF Output Pch Tr OFF Output pin open			0.05	10	μA
Ceramic Resonator Oscillation							
Oscillation Frequency	f <sub>CFOSC</sub> (Note 4)	1/1 (10μs) 400K	OSC1, OS2 (Fig. 1)	392	400	408	kHz
		1/1 (5μs) 800K	OSC1, OSC2 (Fig. 1)	784	800	816	kHz
		1/3 (4μs) 3M 1/4 (5.33μs)	OSC1, OSC2 (Fig. 1)	2.94	3	3.06	MHz
		1/3 (3μs) 4M 1/4 (4μs)	OSC1, OSC2 (Fig. 1)	3.92	4	4.08	MHz
Oscillation Stabilizing Period	t <sub>CFS</sub>					10	ms
RC Oscillation							
Oscillation Frequency	f <sub>CRS</sub>	1/1 predivider C <sub>ext</sub> =220pF±5% R <sub>ext</sub> =6.8kΩ±1% f=1MHz	OSC1, OSC2 (Fig. 9)	554	750	1235	kHz
Pin Capacitance	CP	Other than pins to be tested: V <sub>IN</sub> =V <sub>SS</sub>			10		pF

## LC6568D

4. Serial Interface Characteristics/ $V_{SS} = 0V$ ,  $T_a = -30^{\circ}C$  to  $+70^{\circ}C$ , $V_{DD} = 4.0V$  to  $6.0V$  unless otherwise specified

				min	typ	max	unit
Serial Clock							
Input Clock Cycle Time	tCKCY(1)	Fig. 5	$\overline{SCK}$	3.0			$\mu s$
Output Clock Cycle Time	tCKCY(2)	Fig. 5	$\overline{SCK}$		64 x TCYC		$\mu s$
Input Clock	tCKL(1)	Fig. 5	$\overline{SCK}$	1.0			$\mu s$
"L"-Level Pulse Width							
Output Clock	tCKL(2)	Fig. 5	$\overline{SCK}$		32 x TCYC		$\mu s$
"L"-Level Pulse Width							
Input Clock	tCKH(1)	Fig. 5	$\overline{SCK}$	1.0			$\mu s$
"H"-Level Pulse Width							
Output Clock	tCKH(2)	Fig. 5	$\overline{SCK}$		32 x TCYC		$\mu s$
"H"-Level Pulse Width							
Serial Input							
Data Setup Time	tICK	Specified for $\uparrow$ of $\overline{SCK}$ , Fig. 5	SI	0.5			$\mu s$
Data Hold Time	tCKI	Specified for $\uparrow$ of $\overline{SCK}$ , Fig. 5	SI	0.5			$\mu s$
Serial Output							
Output Delay Time	tCKO	Specified for $\downarrow$ of $\overline{SCK}$ , Nch OD only: External 1kohm, external 50pF Fig. 5	SO			0.5	$\mu s$
Pulse Output							
Period	tpCY	Fig. 6	PE0		64 x TCYC		$\mu s$
"H"-Level Pulse Width	tpH	TCYC=4 x System clock period, Nch OD only: External 1kohm, external 50pF	PE0		32 x TCYC $\pm 10\%$		$\mu s$
"L"-Level Pulse Width	tpL		PE0		32 x TCYC $\pm 10\%$		$\mu s$

5. Comparator Characteristics/ $V_{SS} = 0V$ ,  $T_a = -30^{\circ}C$  to  $+70^{\circ}C$ ,  $V_{DD} = 4.5V$  to  $6.0V$   
unless otherwise specified

				min	typ	max	unit
Comparator Characteristics							
Input Voltage Range	VCMIN		PI3, PJ1 to 3	$V_{SS}+1.0$	$V_{DD}-1.5$		V
Response Speed	TRS	100mV overdrive mode				50	$\mu s$
Offset Voltage	VOFS	VCMIN= $V_{SS}+1.0V$ to $V_{DD}-1.5V$			$\pm 20$	$\pm 100$	mV

(Note 1) When oscillated internally under the oscillating conditions in Fig. 1, up to the oscillation amplitude generated is allowable.

(Note 2) Average over the period of 100msec.

(Note 3) Operating supply voltage  $V_{DD}$  must be held until the standby mode is entered after the execution of the HALT instruction.

The PB3 pin must be free from chattering during the HALT instruction execution cycle.

(Note 4) fCFOSC represents an oscillatable frequency.

(Note 5) The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

(Note 6) When mounting the QIP version on the board, do not dip it in solder.

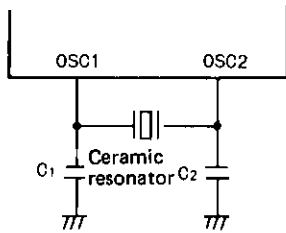


Fig. 1 Ceramic Resonator Oscillation Circuit

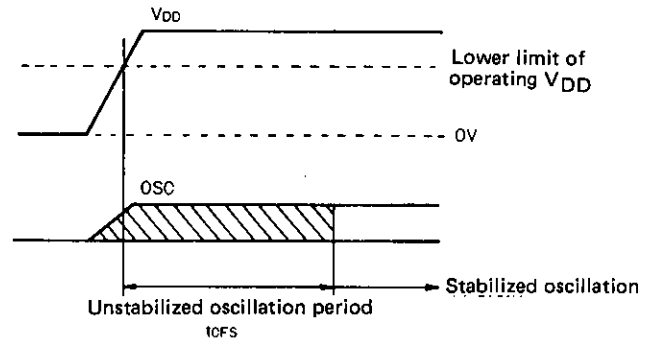


Fig. 2 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for LC6568D Ceramic Resonator Oscillation

4 MHz (Murata) CSA4.00MG	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%
4 MHz (Kyocera) KBR4.0MS	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%
3 MHz (Murata) CSA3.00MG	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%
3 MHz (Kyocera) KBR3.0MS	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%

800 kHz (Murata) CSB800D	C1	220pF $\pm$ 10%
	C2	220pF $\pm$ 10%
800 kHz (Kyocera) KBR800H	C1	220pF $\pm$ 10%
	C2	220pF $\pm$ 10%
400 kHz (Murata) CSB400P	C1	330pF $\pm$ 10%
	C2	330pF $\pm$ 10%
400 kHz (Kyocera) KBR400B	C1	330pF $\pm$ 10%
	C2	330pF $\pm$ 10%

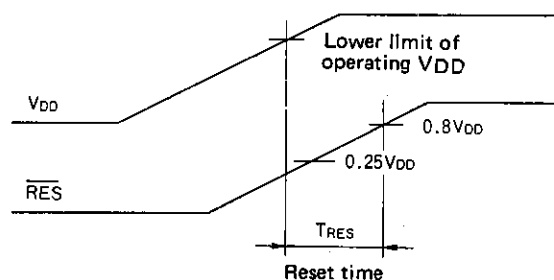
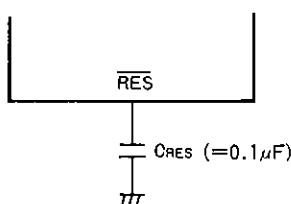


Fig. 3 Reset Circuit and Reset Time

(Note 7) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at CRES=0.1μF. If the rise time of the power supply is long, the value of CRES must be increased so that the reset time becomes 10ms or greater.

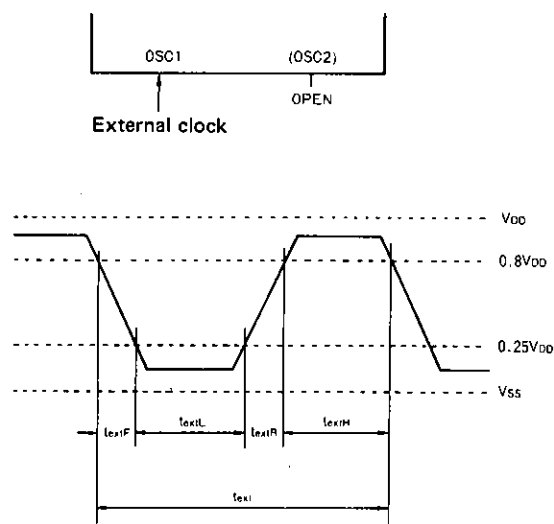


Fig. 1 External Clock Input Waveform

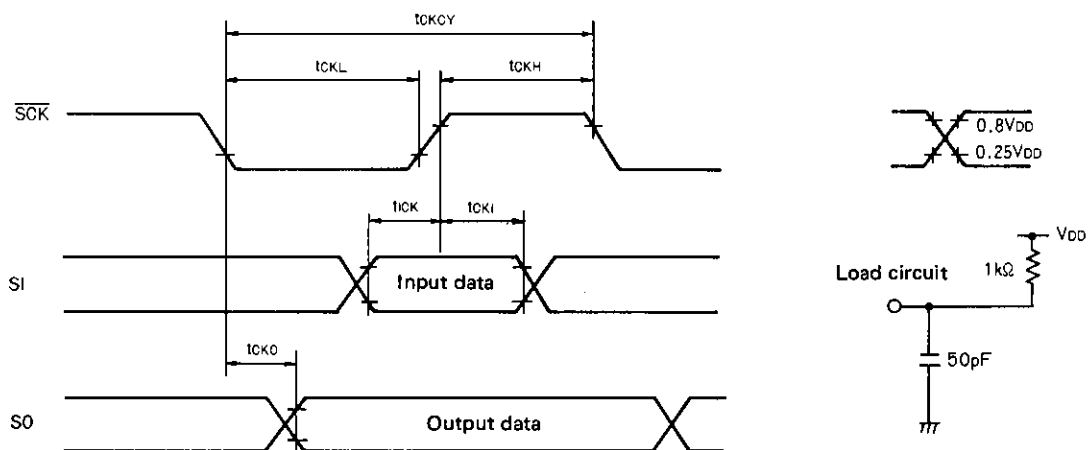


Fig. 5 Serial Input/Output Timing

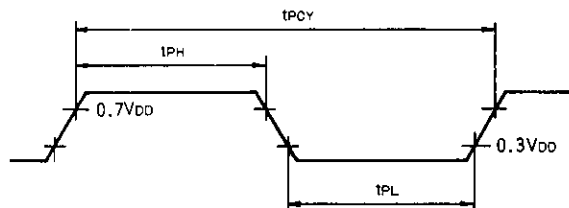


Fig. 6 Pulse Output Timing at Port E0

The load conditions are the same as in Fig. 5.



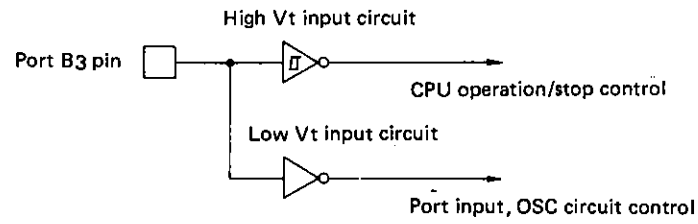


Fig. 7 Port B3 High Vt/Low Vt Input Circuit

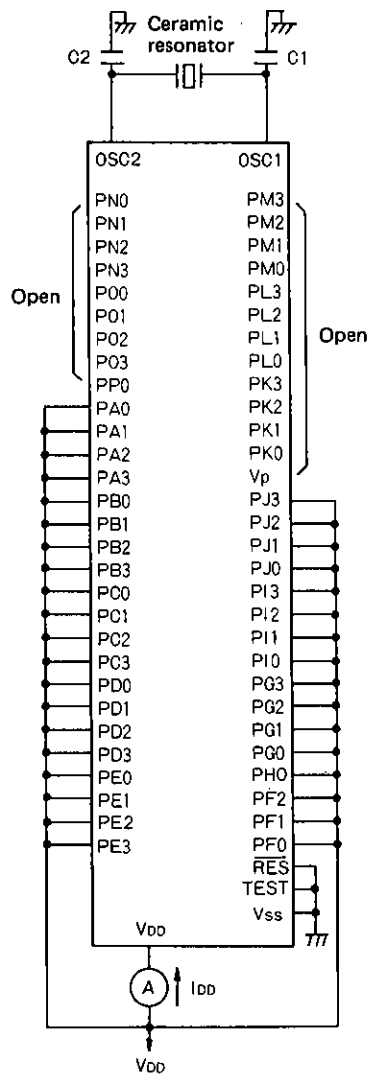


Fig. 8 IDDOP Test Circuit (f=4MHz)

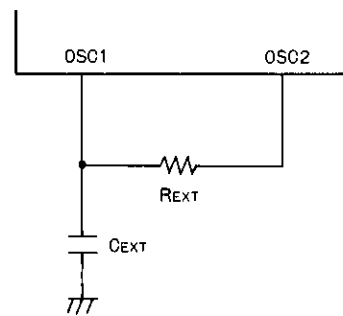


Fig. 9 RC Oscillation Circuit

Table 2 LC6568D

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.)  $V_{DD} = 4$  to  $6V$

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator Option	400 kHz	1/1 (10 $\mu s$ )	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 $\mu s$ )	Unusable with 1/3, 1/4 predivider
	3 MHz	1/3 (4 $\mu s$ ) 1/4 (5.33 $\mu s$ )	Unusable with 1/1 predivider
	4 MHz	1/3 (3 $\mu s$ ) 1/4 (4 $\mu s$ )	Unusable with 1/1 predivider
External Clock Option or External Clock Drive by RC OSC Option	384 to 1444 kHz 1152 to 4330 kHz 1536 to 4330 kHz	1/1 (10.4 to 2.77 $\mu s$ ) 1/3 (10.4 to 2.77 $\mu s$ ) 1/4 (10.4 to 3.70 $\mu s$ )	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option or CR OSC option.		
RC OSC Option	Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the predivider option, frequency, $V_{DD}$ range must be the same as for the external clock option.		

#### RC Oscillation Characteristic of the LC6568D

Fig. 10 shows the RC oscillation characteristic of the LC6568D. For the variation range of RC OSC frequency of the LC6568D, the following are guaranteed at the external constants only shown below.

External constants  $C_{ext} = 220pF$ ,  $R_{ext} = 6.8k\Omega$

$554kHz \leq f_{CRS} \leq 1235kHz$  ( $T_a = -30^\circ C$  to  $+70^\circ C$ ,  $V_{DD} = 4.0$  to  $6.0V$ )

If any other constants than specified above are used, the range of  $R_{ext} = 4k\Omega$  to  $20k\Omega$ ,  $C_{ext} = 150pF$  to  $390pF$  must be observed. (See Fig. 10.)

(Note 8) The oscillation frequency at  $V_{DD} = 5.0V$ ,  $T_a = 25^\circ C$  must not exceed  $750kHz$ .

(Note 9) The oscillation frequency at  $V_{DD} = 4$  to  $6V$ ,  $T_a = -30$  to  $+70^\circ C$  must be within the operation clock frequency range ( $384kHz$  to  $1444kHz$ ).

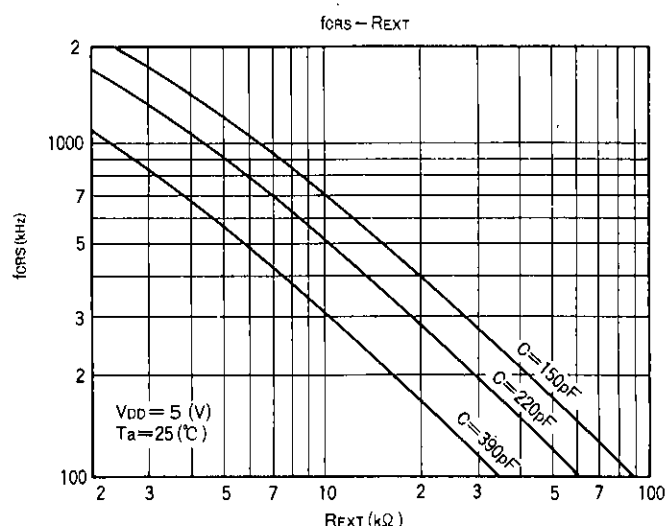


Fig. 10 RC Oscillation Frequency Data (Typ.)

## LC6568H

1. Absolute Maximum Ratings/ $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ 

			min	typ	max	unit
Maximum Supply Voltage	$V_{DD}$ max	$V_{DD}$	-0.3		+7.0	V
Output Voltage	$V_O(1)$	OSC2	Allowable up to voltage generated			V
	$V_O(2)$	Port K, L, M, N, O, P0	$V_{DD}-45$		$V_{DD}+0.3$	V
Input Voltage	$V_I(1)$	OSC1 (Note 1)	-0.3		$V_{DD}+0.3$	V
	$V_I(2)$	TEST, $\overline{RES}$				
	$V_I(3)$	Port A, B	-0.3		+15	V
Input/Output Voltage	$V_{IO}(1)$	Vp	$V_{DD}-45$		$V_{DD}+0.3$	V
		Port of OD type	-0.3		+15	V
		(Port C, D, E, F0 to F2, G, H0, I, J)				
	$V_{IO}(2)$	Port of PU type	-0.3		$V_{DD}+0.3$	V
		(Port C, D, E, F0 to F2, G, H0, I, J)				
Peak Output Current	$I_{OP}(1)$	Port C, D, E, F0 to F2, G, H0, I, J)	-2		+15	mA
	$I_{OP}(2)$	Port K, L	-10		0	mA
	$I_{OP}(3)$	Port M, N, O, P0	-30		0	mA
Allowable Power Dissipation	$P_d$ max	$T_a = -30$ to $+70^\circ\text{C}$				
		DIP64S			600	mW
		QIP 64			430	mW
Operating Temperature	$T_{opr}$		-30		+70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-55		+125	$^\circ\text{C}$
Average Output Current	$I_{OA}(1)$	Per pin over the period of 100msec.	Port C, D, E, F0 to F2, G, H0, I, J)	-2	+15	mA
	$I_{OA}(2)$	Per pin over the period of 100msec.	Port K, L	-10	0	mA
	$I_{OA}(3)$	Per pin over the period of 100msec.	Port M, N, O, P0	-30	0	mA
	$\Sigma I_{OA}(1)$	Total current of PC0 to 3, PD0 to 3, PE0 to 3 (Note 2)		-30	+50	mA
	$\Sigma I_{OA}(2)$	Total current of PF0 to 2, PG0 to 3, PH0, PI0 to 3, PJ0 to 3 (Note 2)		-30	+50	mA
	$\Sigma I_{OA}(3)$	Total current of PK0 to 3, PL0 to 3, PM0 to 3 (Note 2)		-50	0	mA
	$\Sigma I_{OA}(4)$	Total current of PN0 to 3, PO0 to 3, PP0 (Note 2)		-50	0	mA

2. Allowable Operating Conditions/ $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{DD} = 4.5$  to  $6.0\text{V}$  unless otherwise specified

			min	typ	max	unit
Operating Supply Voltage	$V_{DD}$		4.5		6.0	V
Standby Supply Voltage	$V_{ST}$	RAM, register hold (Note 3)	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH}(1)$		1.9		+13.5	V
	$V_{IH}(2)$	Output Nch Tr OFF	Port of OD type	0.7 $V_{DD}$	+13.5	V
			(Port C to J)			
	$V_{IH}(3)$	Output Nch Tr OFF	Port of PU type	0.7 $V_{DD}$	$V_{DD}$	V
			(Port C to J)			

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## LC6568H

				min	typ	max	unit
"L"-Level Input Voltage	V <sub>IH</sub> (4)	Output Nch Tr OFF	$\overline{SCK}$ , SI	0.8V <sub>DD</sub>		+13.5	V
	V <sub>IH</sub> (5)	Output Nch Tr OFF	of OD type $\overline{SCK}$ , SI	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH</sub> (6)	Fig. 7	of PU type High V <sub>t</sub>	V <sub>DD</sub> -0.5		+13.5	V
	V <sub>IH</sub> (7)	Fig. 7	input circuit of PB <sub>3</sub>	Low V <sub>t</sub>	0.5V <sub>DD</sub>	+13.5	V
	V <sub>IH</sub> (8)	Fig. 3	input circuit of PB <sub>3</sub>	RES	0.8V <sub>DD</sub>	V <sub>DD</sub>	V
	V <sub>IH</sub> (9)	V <sub>DD</sub> : 1.8 to 6.0V	PB <sub>0</sub> to 2, INT <sub>0</sub> to 3	0.8V <sub>DD</sub>		+13.5	V
	V <sub>IH</sub> (10)	External clock mode	OSC1	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IL</sub> (1)		PA <sub>0</sub> to 3	V <sub>SS</sub>		+0.5	V
	V <sub>IL</sub> (2)		PCto PJ	V <sub>SS</sub>		0.3V <sub>DD</sub>	V
	V <sub>IL</sub> (3)		TEST				
			PB <sub>0</sub> to 2	V <sub>SS</sub>		0.25V <sub>DD</sub>	V
			$\overline{SCK}$ , SI'				
			INT <sub>0</sub> to 3				
	V <sub>IL</sub> (4)		RES	V <sub>SS</sub>		0.25V <sub>DD</sub>	V
Operating Frequency (Cycle Time) Ceramic Resonator Oscillation Constants External Clock Conditions	V <sub>IL</sub> (5)	Fig. 7	PB <sub>3</sub>	V <sub>SS</sub>		0.9	V
	V <sub>IL</sub> (6)	Fig. 7	PB <sub>3</sub>	V <sub>SS</sub>		0.3	V
	V <sub>IL</sub> (7)	V <sub>DD</sub> : 1.8 to 6.0V	PB <sub>3</sub>	V <sub>SS</sub>		0.3	V
		External clock mode	OSC1	V <sub>SS</sub>		0.25V <sub>DD</sub>	V
	f <sub>op</sub>		OSC1	384		4330	kHz
	(T <sub>CYC</sub> )		OSC2	(10.4)		(0.92)	(μs)
			OSC1	See Fig. 1, Table 1.			
			OSC2				
	Frequency	f <sub>EXT</sub>	1/1 predivider	OSC1 (Fig. 4)	See Table 2.		
	"H"-Level/"L"-Level	t <sub>EXH</sub> , t <sub>EXTL</sub>		OSC1 (Fig. 4)	90		ns
	Clock Pulse Width						
	Rise/Fall Time	t <sub>EXTR</sub> , t <sub>EXTF</sub>		OSC1 (Fig. 4)		30	ns

3. Electrical Characteristics/T<sub>a</sub> = -30 to +70°C, V<sub>SS</sub> = 0V, V<sub>DD</sub> = 4.5 to 6.0V

				min	typ	max	unit
unless otherwise specified							
"H"-Level Input Current	I <sub>IH</sub> (1)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr)	Port of OD type (Port C to J) Port A, B			+5.0	μA
		V <sub>IN</sub> =+13.5V					
"L"-Level Input Current	I <sub>IH</sub> (2)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr)	Port of PU type (Port C to J)			+1.0	μA
		V <sub>IN</sub> =V <sub>DD</sub>	OSC1 (External clock mode)				
"H"-Level Output Voltage	I <sub>IL</sub> (1)	Output Nch Tr OFF V <sub>IN</sub> =V <sub>SS</sub>	Port of OD type (Port C to J) Port A, B	-1.0			μA
			OSC1 (External clock mode)				
"H"-Level Output Voltage	I <sub>IL</sub> (2)	Output Nch Tr OFF V <sub>IN</sub> =V <sub>SS</sub>	Port of PU type (Port C to J)	-1.3	-0.35		mA
	I <sub>IL</sub> (3)	V <sub>IN</sub> =V <sub>SS</sub>	RES	-45	-10		μA
	V <sub>OH</sub> (1)	I <sub>OH</sub> =-50μA	Port of PU type (Port C to J)	V <sub>DD</sub> -1.2			V
	V <sub>OH</sub> (2)	I <sub>OH</sub> =-3mA	Port K, L	V <sub>DD</sub> -1.8			V
	V <sub>OH</sub> (3)	I <sub>OH</sub> =-15mA	Port M, N, O, P <sub>0</sub>	V <sub>DD</sub> -1.8			V

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## LC6568H

				min	typ	max	unit
“L”-Level Output Voltage	VOL(1)	IOL=10mA, Other ports: $\Sigma I_{OLmax}$	Port C, D, E, F0 to F2, G, H0, I, J)			1.5	V
	VOL(2)	IOL=2mA, Each port: IOL=2mA	Port C, D, E, F0 to F2, G, H0, I, J)			0.5	V
	VOL(3)	Vp=-35V, Output Pch Tr OFF Output open	Port of PD type (Port K to P)			-33	V
Output OFF Leakage Current	IOFF(1)	Output Pch Tr OFF VOUT=VDD	Port of OD type (Port K to P)			+30	$\mu A$
	IOFF(2)	Output Pch Tr OFF VOUT=VDD-40V	Port of OD type (Port K to P)	-30			$\mu A$
Hysteresis Voltage	VHYS		RES, INT0 to 3, SCK, SI, OSC1 of Schmitt type (Note 5)	0.1VDD			V
Pull-up Resistance	Rpp	VDD: 5.0V	Port of PU type (Port C to J)		14		k $\Omega$
Pull-down Resistance	Rpd	VDD: 5.0V	Port of PD type (Port K to P)	50		200	k $\Omega$
Current Dissipation	Operation mode, Output Nch Tr, Pch Tr OFF, VIN=VDD						
	IDDOP(1)	4MHz OSC (Fig. 8)	VDD		8	15	mA
	IDDOP(2)	External Clock mode 384kHz to 4330kHz	VDD		8	15	mA
	IDDST	Standby mode Output Nch, Pch Tr OFF Output pin open VIN=VDD	VDD		0.05	10	$\mu A$
Ceramic Resonator Oscillation							
Oscillation Frequency	fCFOSC (Note 4)	1/1 (1 $\mu s$ ) 4MHz	OSC1 OSC2 (Fig. 1)	3.92	4.00	4.08	MHz
Oscillation Stabilizing Period	tCFS	Fig. 2				10	ms
Pin Capacitance	CP	f=1MHz Other than pins to be tested: VIN=VSS			10		pF

## 4. Serial Interface Characteristics/VSS=0V, Ta=-30°C to +70°C,

VDD = 4.5V to 6.0V unless otherwise specified

				min	typ	max	unit
Serial Clock							
Input Clock Cycle Time	tCKCY(1)	Fig. 5	$\overline{SCK}$	3.0			$\mu s$
Output Clock Cycle Time	tCKCY(2)	Fig. 5	$\overline{SCK}$		64 x TCYC		$\mu s$
Input Clock	tCKL(1)	Fig. 5	$\overline{SCK}$	1.0			$\mu s$
“L”-Level Pulse Width							
Output Clock	tCKL(2)	Fig. 5	$\overline{SCK}$		32 x TCYC		$\mu s$
“L”-Level Pulse Width							
Input Clock	tCKH(1)	Fig. 5	$\overline{SCK}$	1.0			$\mu s$
“H”-Level Pulse Width							
Output Clock	tCKH(2)	Fig. 5	$\overline{SCK}$		32 x TCYC		$\mu s$
“H”-Level Pulse Width							

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**LC6568H**

					min	typ	max	unit
<b>Serial Input</b>								
Data Setup Time	t <sub>ICK</sub>	Specified for ↑ of $\overline{\text{SCK}}$ , Fig. 5	SI		0.5			μs
Data Hold Time	t <sub>CKI</sub>	Specified for ↑ of $\overline{\text{SCK}}$ , Fig. 5	SI		0.5			μs
<b>Serial Output</b>								
Output Delay Time	t <sub>CKO</sub>	Specified for ↓ of $\overline{\text{SCK}}$ , Nch OD only: External 1kohm, external 50pF Fig. 5	SO				0.5	μs
<b>Pulse Output</b>								
Period	t <sub>PCY</sub>	Fig. 6 T <sub>CYC</sub> =4 x System clock period, Nch OD only: External 1kohm, external 50pF	PE0		64 x T <sub>CYC</sub>			μs
"H"-Level Pulse Width	t <sub>PH</sub>		PE0		32 x T <sub>CYC</sub> ±10%			μs
"L"-Level Pulse Width	t <sub>PL</sub>		PE0		32 x T <sub>CYC</sub> ±10%			μs

**5. Comparator Characteristics/V<sub>SS</sub> = 0V, T<sub>a</sub> = -30°C to +70°C V<sub>DD</sub> = 4.5V to 6.0V  
unless otherwise specified**

					min	typ	max	unit
<b>Comparator Characteristics</b>								
Input Voltage Range	V <sub>CMIN</sub>		PI3, PJ1 to 3	V <sub>SS</sub> +1.0		V <sub>DD</sub> -1.5		V
Response Speed	TRS	100mV overdrive mode					50	μs
Offset Voltage	V <sub>OFS</sub>	V <sub>CMIN</sub> =V <sub>SS</sub> +1.0V to V <sub>DD</sub> -1.5V			±20	±100		mV

(Note 1) When oscillated internally under the oscillating conditions in Fig. 1, up to the oscillation amplitude generated is allowable.

(Note 2) Average over the period of 100msec.

(Note 3) Operating supply voltage V<sub>DD</sub> must be held until the standby mode is entered after the execution of the HALT instruction.

The PB<sub>3</sub> pin must be free from chattering during the HALT instruction execution cycle.

(Note 4) f<sub>COSC</sub> represents an oscillatable frequency.

(Note 5) The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

(Note 6) When mounting the QIP version on the board, do not dip it in solder.

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

- ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

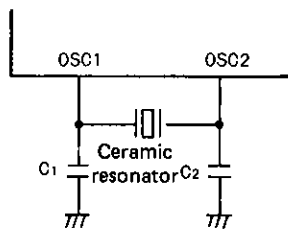


Fig. 1 Ceramic Resonator Oscillation Circuit

Table 1 Constants Guaranteed for LC6568H Ceramic Resonator Oscillation

4 MHz (Murata) CSA4.00MG	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%
4 MHz (Kyocera) KBR4.0MS	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%
3 MHz (Murata) CSA3.00MG	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%
3 MHz (Kyocera) KBR3.0MS	C1	33pF $\pm$ 10%
	C2	33pF $\pm$ 10%

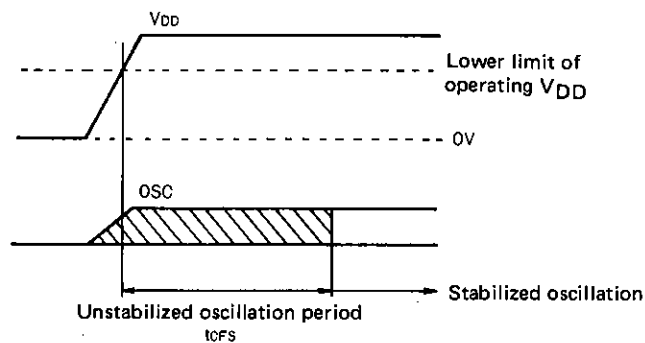


Fig. 2 Oscillation Stabilizing Period

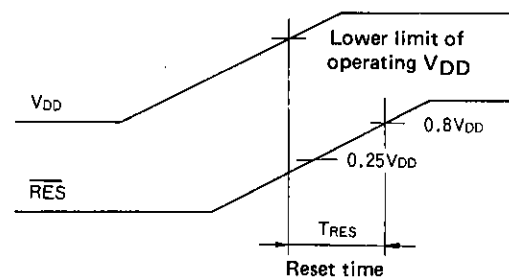
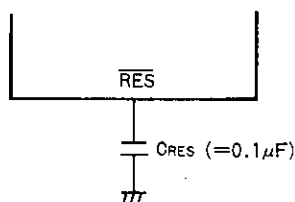


Fig. 3 Reset Circuit and Reset Time

(Note 7) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at  $C_{RES} = 0.1\mu F$ . If the rise time of the power supply is long, the value of  $C_{RES}$  must be increased so that the reset time becomes 10ms or greater.

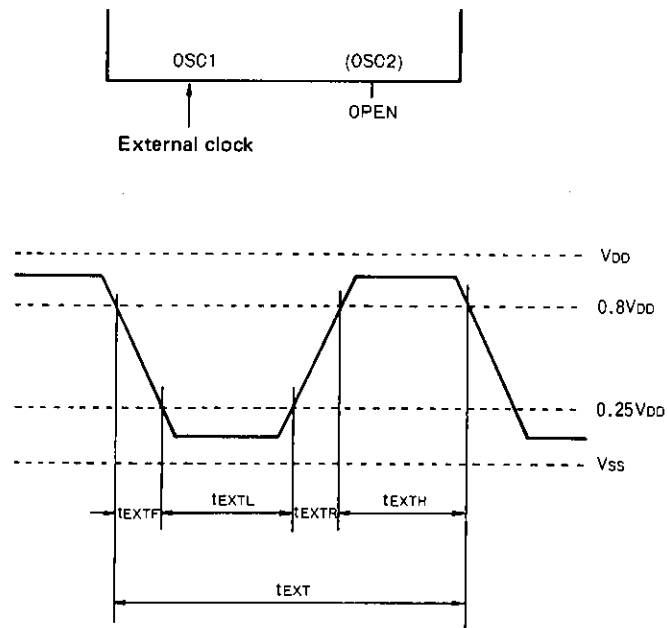


Fig. 4 External Clock Input Waveform

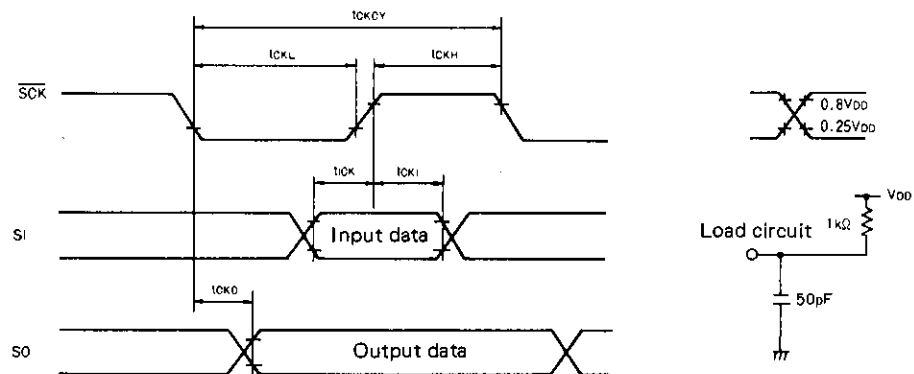


Fig. 5 Serial Input/Output Timing

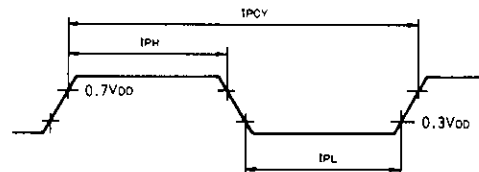


Fig. 6 Pulse Output Timing at Port E0

The load conditions are the same as in Fig. 5.



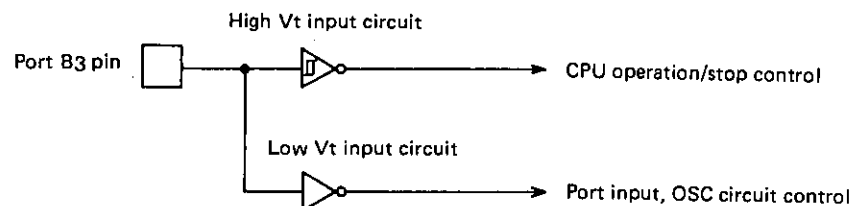


Fig. 7 Port B3 High Vt/Low Vt Input Circuit

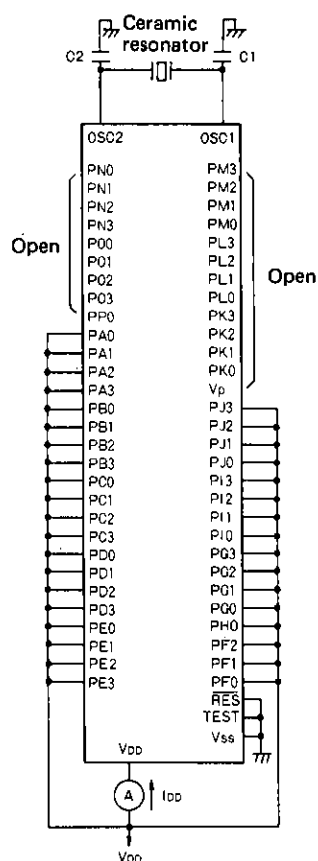


Fig. 8 IDDOP Test Circuit (f=4MHz)

Table 2 LC6568H

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.)  $V_{DD} = 4.5$  to  $6V$

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator OSC Option	4 MHz	1/1 (1 $\mu s$ )	
External Clock Option	384 to 4330 kHz	1/1 (10.4 to 0.92 $\mu s$ )	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option.		

## Notes for Program Evaluation

- When evaluating the LC6568D/H with the evaluation chip (LC6595, LC65PG68), the following must be observed.

Classi- fication	Item	Function	
		Mass-production chip	Evaluation chip
Notes for option	OSC divider	3 selections (1/1, 1/3, 1/4) by option (Note) For H version, 1/1 divider only is available.	3 selections (1/1, 1/3, 1/4) available by 2 pins of DIV pin, 3OR4 pin. DIV pin, 3OR4 pin must be set according to option specified for mass-production chip.
	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and Port D can be brought to "H" and "L" by CHL pin and DHL pin respectively. CHL pin and DHL pin must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected bitwise.	Only Nch OD without PU. [Evaluation chip-applied evaluation] External resistor (10kohms) on evaluation board must be connected to necessary port. [Simulation chip-applied evaluation] Resistor must be connected to necessary port on application board.
	PU resistor configuration	PU resistor brought to Hi-Z at "L" output mode (Pch Tr is turned OFF).	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode. For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.
	Port output configuration PD/OD	PD or OD can be selected bitwise.	Only Pch OD without PD. [Evaluation chip-applied evaluation] External resistor (100kohms) on evaluation board must be connected to necessary port. [Simulation chip-applied evaluation] Resistor must be connected to necessary port on application board. In this case, load power source must be also supplied on application board.
	Port function, port input/output or comparator input	If the input instruction (IP, BP) is executed with port input/output or comparator input function not option-selected, "0" is input from the port bits not specified as port input/output or comparator input.	The input pins with options not selected are in floating state. That is, the data input from such pins are indeterminate. If the input instruction (IP, BP, BNP) for these input pins, unpredictable data is input from them. Do not use any input instruction for such input pins.
Notes for OSC	OSC constants -1	[2-pin RC OSC] Catalog-guaranteed constants in catalog.	[2-pin RC OSC] Different from mass-production chip in circuit design and characteristic. Frequency must be adjusted to OSC frequency of mass-production chip by adjusting variable resistor.
		[2-pin ceramic resonator OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin ceramic resonator OSC] Different from mass-production chip in circuit design and characteristic. Wiring capacitance may provide unstable OSC. External constants must be fine-adjusted according to service conditions.

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Classification	Item	Function	
		Mass-production chip	Evaluation chip
Notes for OSC	OSC constants -2	[2-pin ceramic resonator OSC] Feedback resistor is contained.	[2-pin ceramic resonator OSC] No feedback resistor is contained. Feedback resistor of 1Mohm must be connected externally.
Notes for electrical characteristics	OSC frequency	OSC frequency characteristic as indicated in catalog.	Different from mass-production chip in circuit design, and characteristic. ES, CS must be used to evaluate characteristic in detail.
	Operating current, standby current	Current characteristic as indicated in catalog.	Different from mass-production chip in circuit design, characteristic. The standby current cannot be evaluated in detail. However, the standby current can be confirmed roughly in the manner discussed later. Be sure to confirm the standby current. ES, CS must be used to evaluate characteristic in detail.
	Operating voltage	Supply voltage range as indicated in catalog.	Evaluation chip must be also used at $V_{DD}=5V\pm5\%$ at which EPROM, other LSI are used. Therefore, $V_{DD}=5V\pm5\%$ only can be used for evaluation of mass-production microcomputers.
	Operating temperature	Temperature range as indicated in catalog.	Evaluation chip and simulation chip must be used at $10^{\circ}\text{C}$ to $40^{\circ}\text{C}$ for evaluation.
Notes for I/O port circuit configuration	Port A	Input-only port	Port A is an input/output common port. Do not use the output instructions (OP, SPB, RPB). When performing evaluation, do not fail to turn OFF the pull-up resistance option switch for port A on the evaluation chip board.
	Port F3	The PF3 is not available. Even when the output instruction (OP, SPB, RPB) is executed, no operation is performed.	The PF3 exists. However, do not use the output instruction (OP, SPB, RPB) for this pin. When the output instruction is executed and "0" is output to the pin, the interrupt circuit is affected.
		When the IP instruction is executed "0" is always input to AC from pin PF3.	When the IP instruction is executed, "1" is always input to AC from pin PF3. However, "0" is input if "0" has been output to pin PF3 by the OP instruction.

The EVA800-TB6568 board and LC65PG68 incorporates an LC6568 evaluation IC and a gate array.

Actual performance may differ from evaluation performance because of the gate array which is used to emulate interrupts and control bidirectional port,  $\text{PH}_0$ .

### 1. Operation

The gate array can go out of sync with the LC6586D/H due to slight variations in the reset rise time. If this occurs, the LC6568 evaluation IC will not accept interrupts or  $\text{PH}_0$  port instructions for several ms after program startup.

When running programs, always ensure that interrupts or  $\text{PH}_0$  port instructions are processed correctly.

### 2. Characteristics

When output driver options have been selected, ports  $\text{PB}_{0..7}$  and  $\text{PH}_0$  have a breakdown voltage of 15V in the case of volume fabrication devices. In the LC6568 evaluation IC, however, these ports have a withstanding voltage equal to  $V_{DD}$ . Take care that test circuit designs do not exceed this limit.

## &lt; Confirmation methods for the standby function &gt;

The standby current at the standby mode of the simulation chip can be evaluated not exactly but approximately. Then, do the following steps.

## (a) Confirmation of the standby state

Be sure to confirm whether or not the LSI enters the standby mode when the standby conditions are satisfied.

(i) When the OSC1 and OSC2 oscillation option is selected, confirm on an oscilloscope that the oscillation stops in the standby mode.

(ii) Confirmation by the current dissipation

Remove the EPROM when confirming whether or not the LSI enters the standby mode. The  $I_{DD}$  of the LSI can determine whether or not the LSI is now in the standby mode.

When the LSI is in the operating mode, more than some  $100\mu\text{A}$  current is transmitted. When in the standby mode, the current of the  $I_{DD}$  is  $150\mu\text{A}$  or less if the DIV, 3OR4, CHL, DHL are all set to "H" (excluding the load current). If the DIV, 3OR4, CHL, DHL, —, etc. are all set to "L", the current of the  $I_{DD}$  is approximately  $20\mu\text{A}$ .

## (b) Confirmation by the load current

Your program must be designed so that the current is not transmitted to the input/output ports prior to the execution of the HALT instruction. This can reduce the useless dissipation of the load current at the standby mode and be confirmed on an oscilloscope.

(i) Design your program so that the current is not transmitted to the output ports prior to the execution of the HALT instruction.

(ii) Design your program and peripherals so that the input ports and input/output ports are not brought to the floating state at the standby mode.

If brought to the floating state, current flows in the microcomputer input circuit section, causing more current dissipation. Therefore, the backup enable time is shortened extremely in applications where the capacitor backup is used. (For the evaluation chip, there is appreciable current because the option circuit section to select the port input/output or comparator input is partly in the floating state.)

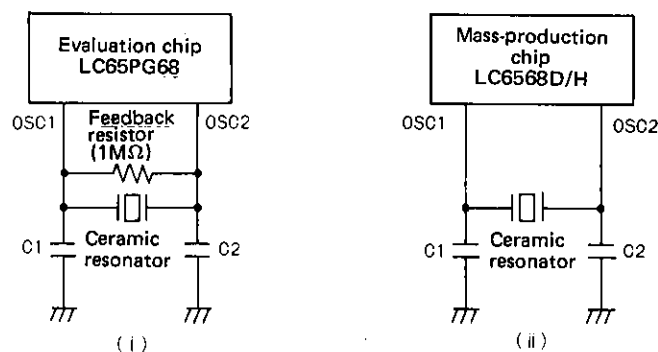
## Ceramic resonator oscillation constants when the EVA800-TB6568 is used

When developing your program using the eva-chip board EVA800-TB6568, adjust the capacitor value according to the stray capacitance of the circuit because the ceramic resonator oscillation constants depend on the conditions for evaluation and the cable length, etc.

Note) When the evaluation chip is used in the 2-pin ceramic resonator oscillation mode, no feedback resistor is contained unlike the mass-production chip.

Connect a feedback resistor of  $1\text{M}\Omega$  externally as shown below.

Since constants R, C are also differ from those for the mass-production chip, adjust the capacitor value according to the stray capacitance of the circuit.



2-pin Ceramic Resonator Oscillation Circuit for  
Evaluation Chip and Mass-production Chip

## LC6568 INSTRUCTION SET

Symbol	Description		
AC	: Accumulator	M(DP)	: Memory addressed by DP
ACt	: Accumulator bit t	P(DP <sub>L</sub> )	: Input/output port addressed by DP <sub>L</sub>
CF	: Carry flag	PC	: Program counter
CTL	: Control register	STACK	: Stack register
DP	: Data pointer	TM	: Timer
E	: E register	TMF	: Timer (internal) interrupt request flag
EXTF	: External interrupt request flag	At, Hs, La	: Working register
Fn	: Flag bit n	ZF	: Zero flag
M	: Memory	P(DP <sub>L</sub> )	: Pseudo input/output port specified by DP <sub>L</sub>
		{ }, !	: Contents
		-	: Transfer and direction
		+	: Addition
		-	: Subtraction
		Λ	: AND
		V	: OR
		∨	: Exclusive OR

Instruction group		Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks												
			D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>																		
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1												
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF													
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF													
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← (AC)	The AC contents are complemented.	ZF													
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF													
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	The AC contents are decremented -1.	ZF CF													
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC <sub>0</sub> ← (CF), AC <sub>n+1</sub> ← (AC <sub>n</sub> ), CF ← (AC <sub>3</sub> )	The AC contents are shifted left through the CF.	ZF CF													
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.														
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)	The AC contents and the E contents are exchanged.														
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← (M(DP)) + 1	The M(DP) contents are incremented +1.	ZF CF													
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← (M(DP)) - 1	The M(DP) contents are decremented -1.	ZF CF													
	SMB bit	Set M data bit	0 0 0 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1	A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is set.														
RMB bit	Reset M data bit	0 0 1 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0	A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is reset.	ZF														
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF													
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF													
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF													
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF													
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF													
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(DP))	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF													
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF													
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	(M(DP)) + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. <table><tr><td>Comparison result</td><td>CF</td><td>ZF</td></tr><tr><td>(M(DP)) &gt; (AC)</td><td>0</td><td>0</td></tr><tr><td>(M(DP)) = (AC)</td><td>1</td><td>1</td></tr><tr><td>(M(DP)) &lt; (AC)</td><td>1</td><td>0</td></tr></table>	Comparison result	CF	ZF	(M(DP)) > (AC)	0	0	(M(DP)) = (AC)	1	1	(M(DP)) < (AC)	1	0	ZF CF	
	Comparison result	CF	ZF																			
(M(DP)) > (AC)	0	0																				
(M(DP)) = (AC)	1	1																				
(M(DP)) < (AC)	1	0																				
CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 1 2 1 1 0	2 2	2	{1 3 1 2 1 1 0} + (AC) + 1	The AC contents and the immediate data {1 3 1 2 1 1 0} are compared and the ZF and CF are set/reset. <table><tr><td>Comparison result</td><td>CF</td><td>ZF</td></tr><tr><td>{1 3 1 2 1 1 0} &gt; (AC)</td><td>0</td><td>0</td></tr><tr><td>{1 3 1 2 1 1 0} = (AC)</td><td>1</td><td>1</td></tr><tr><td>{1 3 1 2 1 1 0} &lt; (AC)</td><td>1</td><td>0</td></tr></table>	Comparison result	CF	ZF	{1 3 1 2 1 1 0} > (AC)	0	0	{1 3 1 2 1 1 0} = (AC)	1	1	{1 3 1 2 1 1 0} < (AC)	1	0	ZF CF		
Comparison result	CF	ZF																				
{1 3 1 2 1 1 0} > (AC)	0	0																				
{1 3 1 2 1 1 0} = (AC)	1	1																				
{1 3 1 2 1 1 0} < (AC)	1	0																				
CLI data	Compare DP <sub>L</sub> with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 3 1 2 1 1 0	2 2	2	(DP <sub>L</sub> ) ∨ {1 3 1 2 1 1 0}	The DP <sub>L</sub> contents and the immediate data {1 3 1 2 1 1 0} are compared.	ZF														
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	1 3 1 2 1 1 0	1	1	AC ← {1 3 1 2 1 1 0}	The immediate data {1 3 1 2 1 1 0} is loaded in the AC.	ZF	* 1												
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).														
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	The M(DP) contents are loaded in the AC.	ZF													
	XM data	Exchange AC with M, then modify DP <sub>H</sub> with immediate data	1 0 1 0	0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>	1	2	(AC) ↔ (M(DP)) DP <sub>H</sub> ← (DP <sub>H</sub> ) ∨ OM <sub>2</sub> M <sub>1</sub> M <sub>0</sub>	The AC contents and the M(DP) contents are exchanged and then the DP <sub>H</sub> contents are modified with the contents of (DP <sub>H</sub> ) ∨ OM <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .	ZF	The ZF is set/reset according to the result of (DP <sub>H</sub> ) ∨ OM <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .												
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ (M(DP))	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP <sub>H</sub> contents at the time of instruction execution.												
	XI	Exchange AC with M, then increment DP <sub>L</sub>	1 1 1 1	1 1 1 0	1	2	(AC) ↔ (M(DP)) DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1	The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP <sub>L</sub> ) + 1.												
	XD	Exchange AC with M, then decrement DP <sub>L</sub>	1 1 1 1	1 1 1 1	1	2	(AC) ↔ (M(DP)) DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1	The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are decremented -1.	ZF	The ZF is set/reset according to the result of (DP <sub>L</sub> ) - 1.												
RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.															

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		O <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>						
Data pointer manipulation instructions	LDZ data	Load DPH with Zero and DPL with immediate data respectively	1 0 0 0 13 12 11 10	1	1	DPH ← 0 DPL ← 13 12 11 10	The DPH and DPL are loaded with 0 and the immediate data 13 12 11 10 respectively.		
	LHI data	Load DPH with immediate data	0 1 0 0 13 12 11 10	1	1	DPH ← 13 12 11 10	The DPH is loaded with the immediate data 13 12 11 10.		
	IND	Increment DPL	1 1 1 0 1 1 1 0	1	1	DPL ← (DPL) + 1	The DPL contents are incremented +1.	ZF	
	DED	Decrement DPL	1 1 1 0 1 1 1 1	1	1	DPL ← (DPL) - 1	The DPL contents are decremented -1.	ZF	
	TAL	Transfer AC to DPL	1 1 1 1 0 1 1 1	1	1	DPL ← (AC)	The AC contents are transferred to the DPL.		
	TLA	Transfer DPL to AC	1 1 1 0 1 0 0 1	1	1	AC ← (DPL)	The DPL contents are transferred to the AC.	ZF	
	XAH	Exchange AC with DPH	0 0 1 0 0 0 1 1	1	1	(AC) ↔ (DPH)	The AC contents and the DPH contents are exchanged.		
Working register manipulation instructions	XA0 XA1 XA2 XA3	Exchange AC with working register At	1 1 1 0 0 0 0 0 1 1 1 0 0 1 0 0 1 1 1 0 1 0 0 0 1 1 1 0 1 1 0 0	1 1 1 1	1 1 1 1	(AC) ↔ (A0) (AC) ↔ (A1) (AC) ↔ (A2) (AC) ↔ (A3)	The AC contents and the contents of working register At are exchanged. At is assigned one of A0, A1, A2, A3 according to t <sub>1</sub> t <sub>0</sub> .		
	XHa XHO XH1	Exchange DPH with working register Ha	1 1 1 1 1 0 0 0 1 1 1 1 1 1 0 0	1 1 1	1 1 1	(DPH) ↔ (H0) (DPH) ↔ (H1)	The DPH contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.		
	XLa XLO XL1	Exchange DPL with working register La	1 1 1 1 0 0 0 0 1 1 1 1 0 1 0 0	1 1 1	1 1 1	(DPL) ↔ (L0) (DPL) ↔ (L1)	The DPL contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a.		
	SFB flag	Set flag bit	0 1 0 1 B3 B2 B1 B0	1	1	F <sub>n</sub> ← 1	The flag specified with B3 B2 B1 B0 is set.		
	RFB flag	Reset flag bit	0 0 0 1 B3 B2 B1 B0	1	1	F <sub>n</sub> ← 0	The flag specified with B3 B2 B1 B0 is reset.	ZF	The flags are divided into 4 groups of F <sub>0</sub> to F <sub>3</sub> , F <sub>4</sub> to F <sub>7</sub> , F <sub>8</sub> to F <sub>11</sub> , F <sub>12</sub> to F <sub>15</sub> . The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B3 B2 B1 B0.
Flag manipulation instructions	JMP addr	Jump in the current bank	0 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	PC ← PC <sub>11</sub> (or PC <sub>11</sub> ), P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	A jump to the address specified with the PC <sub>12</sub> PC <sub>11</sub> (or PC <sub>11</sub> ) and immediate data P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> occurs.		If the BANK and SB instructions are executed consecutively, the bank is changed.
	JPEA	Jump in the current page modified by E and AC	1 1 1 1 1 0 1 0	1	1	PC <sub>7~0</sub> ← (E, AC)	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1	1	STACK ← (PC) + 1 PC <sub>11~6</sub> , PC <sub>1~0</sub> → 0 PC <sub>5~2</sub> ← P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	STACK ← (PC) + 2 PC <sub>11~0</sub> → OP <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0 0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0 0 0 1 0	1	1	PC ← (STACK) CF ZF ← CSF, ZSF	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1 1 1 0 1	1	1	PC <sub>11</sub> ← (PC <sub>11</sub> )	The bank is changed. (Effective only when immediately followed by the JMP instruction) The pseudo I/O port is specified. (Effective when immediately followed by the IP, OP, SPB, RPB, BP, BNP instruction)		
	SB	Set bank	0 1 1 0 0 1 1 10	1	1	PC <sub>12</sub> PC <sub>11</sub> ← 11, 10	The bank is changed. Effective only when used immediately before the JMP instruction.		
Branch instructions	BA <sub>t</sub> addr	Branch on AC bit	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if AC <sub>t</sub> = 1	If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if AC <sub>t</sub> = 0	If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMI addr	Branch on M bit	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (M(DP), t <sub>1</sub> t <sub>0</sub> ) = 1	If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (M(DP), t <sub>1</sub> t <sub>0</sub> ) = 0	If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNMO to BNMO3 according to the value of t.
	BPT addr	Branch on Port bit	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2 2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (P(DPL), t <sub>1</sub> t <sub>0</sub> ) = 1	If a single bit of port P(DPL) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BPO to BP3 according to the value of t.

Instruction group	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>						
Branch instructions	BNP <sub>t</sub> addr	Branch on no Port bit	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 0 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (P(DP <sub>L</sub> .t) = 0)	If a single bit of port P(DP <sub>L</sub> ) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if CF = 1	If the CF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if CF = 0	If the CF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BF <sub>n</sub> addr	Branch on flag bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if F <sub>n</sub> = 1	If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNF <sub>n</sub> addr	Branch on no flag bit	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if F <sub>n</sub> = 0	If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← (P(DP <sub>L</sub> ))	Port P(DP <sub>L</sub> ) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP <sub>L</sub> ) ← (AC)	The AC contents are outputted to port P(DP <sub>L</sub> ).		
	SPB bit	Set port bit	0 0 0 0	0 1 B <sub>1</sub> B <sub>0</sub>	1	2	P(DP <sub>L</sub> .B <sub>1</sub> B <sub>0</sub> ) ← 1	A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B <sub>1</sub> B <sub>0</sub>	1	2	P(DP <sub>L</sub> .B <sub>1</sub> B <sub>0</sub> ) ← 0	A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	CTL ← (CTL) V B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	CTL ← (CTL) A B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are reset.	ZF	
	WTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E). (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

\*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, -----, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.