



LC72358N, 72362N, 72366

Single-Chip PLL Microcontrollers

Overview

The LC72358N, LC72362N, and LC72366 are 1.33 μ s instruction execution time single-chip microcontrollers for electronic tuning applications. These products incorporate a high-speed locking circuit and a high-performance direct PLL circuit that can control the local oscillator C/N characteristics. These products have 256 or 512 bytes of RAM and 16K, 24K or 32K bytes of program ROM on chip, and incorporate a three-channel serial I/O interface, a six-channel A/D converter and other interfaces.

Features

- ROM
 - LC72358N: 8K steps (8191×16 bits)
 - LC72362N: 12K steps (12287×16 bits)
 - LC72366: 16K steps (16383×16 bits)
 - The subroutine area in both products is 4K steps (4095×16 bits).
- RAM
 - LC72358N, 72362N: 512×4 bits (banks 0 to 7)
 - LC72366: $1K \times 4$ bits (banks 0 to F)
- Stack: Eight levels
- Serial I/O: Three channels (8-bit 3-wire format)
 - There are three internal serial clocks: 12.5 kHz, 37.5 kHz and 187.5 kHz.
- External interrupts:
 - Two channels (the INT0 and INT1 pins)
 - Switching between rising and falling edge detection is supported.
- Internal interrupts:
 - Three channels
 - Two internal timer interrupt channels
 - The timers provide eight interrupt periods: 100 μ s, 1 ms, 2 ms, 5 ms, 10 ms, 50 ms, 125 ms and 250 ms.
 - One serial I/O interrupt channel
- Multiple interrupt levels:
 - Four levels
 - Hardware priority order
 - INT0 pin > INT1 pin > SI/O pin > internal timer 0 > internal timer 1
- A/D converter: Six channels (6-bit successive approximation type)
- General-purpose ports
 - Input ports: 10
 - Output ports: 28
 - I/O ports: 25 (These pins can be switched between input and output in bit units.)
- PLL block
 - Built-in sub-charge pump for high-speed locking
 - Support for dead zone control
 - Built-in unlock detection circuit
 - Twelve reference frequencies: 1, 3, 3.125, 5, 6.25, 9, 10, 12.5, 25, 30, 50 and 100 kHz
- Universal counter: 20 bits
 - Supports frequency and period measurement with counting periods of 1, 4, 8 and 32 ms.
- Timers: Timer interrupt periods
 - 100 μ s, 1 ms, 2 ms, 5 ms, 10 ms, 50 ms, 125 ms and 250 ms
- Beep: Six frequencies: 2.08 kHz, 2.25 kHz, 2.5 kHz, 3.0 kHz, 3.75 kHz, 4.17 kHz.
- Reset: Built-in voltage detection type reset circuit
- Cycle time: 1.33 μ s (all instructions execute in one cycle)
- Halt mode: The microcontroller operating clock is stopped in halt mode.
 - There are four types of event that clear halt mode: interrupt requests, timer FF overflows, key inputs, and hold pin inputs.
- Operating supply voltage: 4.5 to 5.5 V (3.5 to 5.5 V when only the controller block operates)
- Package: QFP80E (QIP80E)
- OTP version: LC72P366
- Development tools: EmulatorRE32N
 - Evaluation chipLC72EV350
 - Evaluation chip boardEB-72EV350

This LSI can easily use CCB that is SANYO's original bus format.



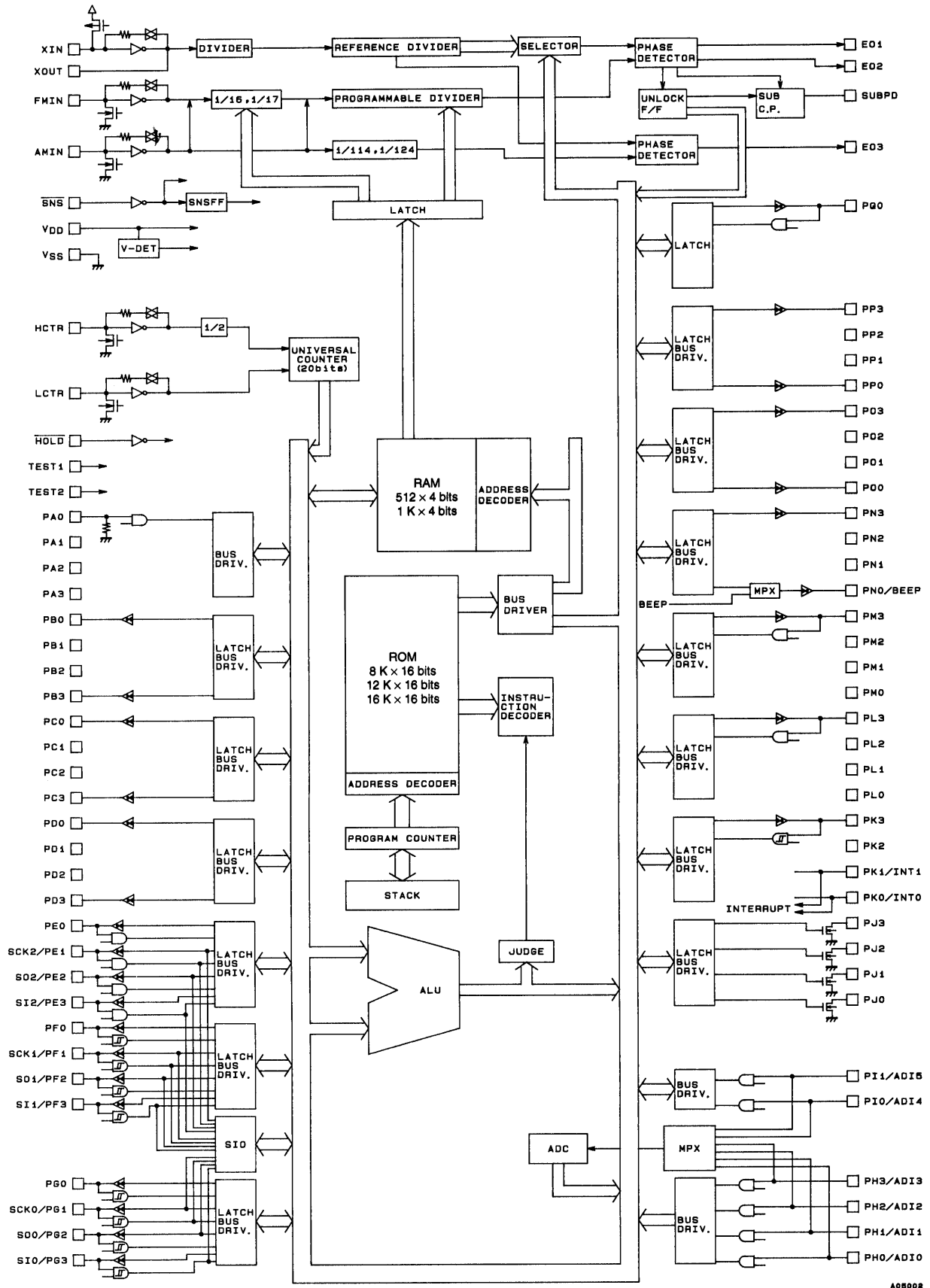
- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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63096HA (OT)/62295TH (OT) No. 5065-1/13

Block Diagram



A05008

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +6.5	V
Input voltage	V_{IN}	All input pins	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_{OUT(1)}$	J port	-0.3 to +15	V
	$V_{OUT(2)}$	All output ports other than $V_{OUT(1)}$	-0.3 to $V_{DD} + 0.3$	V
Output current	$I_{OUT(1)}$	J port	0 to 5	mA
	$I_{OUT(2)}$	D, E, F, G, K, L, M, N, O, P and Q ports, EO1, EO2, EO3, SUBPD	0 to 3	mA
	$I_{OUT(3)}$	B and C ports	0 to 1	mA
Allowable power dissipation	$P_d\text{ max}$	$T_a = -40\text{ to }+85^\circ\text{C}$	400	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-45 to +125	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -40\text{ to }+85^\circ\text{C}$, $V_{DD} = 3.5\text{ to }5.5\text{ V}$

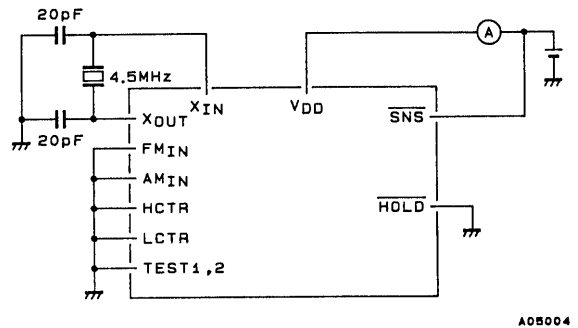
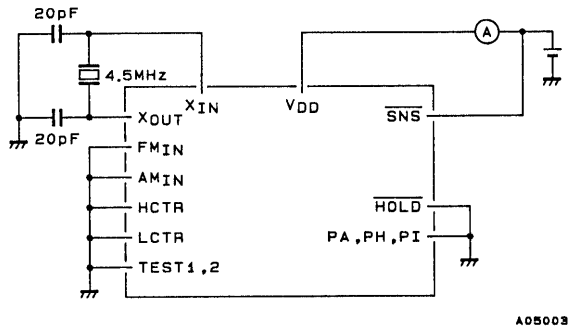
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD(1)}$	CPU and PLL operating	4.5	5.0	5.5	V
	$V_{DD(2)}$	CPU operating	3.5		5.5	V
	$V_{DD(3)}$	Memory retention	1.3		5.5	V
Input high level voltage	$V_{IH(1)}$	E, H, I, L, M and Q ports, HCTR and LCTR (when selected for input)	$0.7 V_{DD}$		V_{DD}	V
	$V_{IH(2)}$	F, G and K ports, LCTR (period measurement mode), HOLD	$0.8 V_{DD}$		V_{DD}	V
	$V_{IH(3)}$	\overline{SNS}	2.5		V_{DD}	V
	$V_{IH(4)}$	A port	$0.6 V_{DD}$		V_{DD}	V
Input low level voltage	$V_{IL(1)}$	E, H, I, L, M and Q ports, HCTR and LCTR (when selected for input)	0		$0.3 V_{DD}$	V
	$V_{IL(2)}$	A, F, G and K ports, LCTR (period measurement mode)	0		$0.2 V_{DD}$	V
	$V_{IL(3)}$	\overline{SNS}	0		1.3	V
	$V_{IL(4)}$	\overline{HOLD}	0		$0.4 V_{DD}$	V
Input frequency	$f_{IN(1)}$	XIN	4.0	4.5	5.0	MHz
	$f_{IN(2)}$	FMIN: $V_{IN(2)}$, $V_{DD(1)}$	10		150	MHz
	$f_{IN(3)}$	FMIN: $V_{IN(3)}$, $V_{DD(1)}$	10		130	MHz
	$f_{IN(4)}$	AMIN (H): $V_{IN(3)}$, $V_{DD(1)}$	2.0		40	MHz
	$f_{IN(5)}$	AMIN (L): $V_{IN(3)}$, $V_{DD(1)}$	0.5		10	MHz
	$f_{IN(6)}$	HCTR: $V_{IN(3)}$, $V_{DD(1)}$	0.4		12	MHz
	$f_{IN(7)}$	LCTR: $V_{IN(3)}$, $V_{DD(1)}$	100		500	kHz
	$f_{IN(8)}$	LCTR (period measurement): $V_{IH(2)}$, $V_{IL(2)}$, $V_{DD(1)}$	1		20×10^3	Hz
Input amplitude	$V_{IN(1)}$	XIN	0.5		1.5	Vrms
	$V_{IN(2)}$	FMIN	0.10		1.5	Vrms
	$V_{IN(3)}$	FMIN, AMIN, HCTR, LCTR	0.07		1.5	Vrms
Input voltage range	$V_{IN(4)}$	ADI0 to ADI5	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level current	$I_{IH}(1)$	XIN: $V_I = V_{DD} = 5.0\text{ V}$	2.0	5.0	15	μA
	$I_{IH}(2)$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0\text{ V}$	4.0	10	30	μA
	$I_{IH}(3)$	A, E, F, G, H, I, K, L, M and Q ports, $\overline{\text{SNS}}$, $\overline{\text{HOLD}}$, HCTR, LCTR, with no pull-down resistor on A port. $V_I = V_{DD} = 5.0\text{ V}$, with the E, F, G, K, L, M and Q ports selected for input.			3.0	μA
	$I_{IH}(4)$	A port: pull-down resistor present, $V_I = V_{DD} = 5.0\text{ V}$		50		μA
Input low level current	$I_{IL}(1)$	XIN: $V_I = V_{SS}$	2.0	5.0	15	μA
	$I_{IL}(2)$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	μA
	$I_{IL}(3)$	A, E, F, G, H, I, K, L, M and Q ports, $\overline{\text{SNS}}$, $\overline{\text{HOLD}}$, HCTR, LCTR, with no pull-down resistor on A port. $V_I = V_{SS}$, with the E, F, G, K, L, M and Q ports selected for input.			3.0	μA
Input floating voltage	V_{IF}	A port: pull-down resistor present			$0.05 V_{DD}$	V
Pull-down resistance	$R_{PD}(1)$	A port: pull-down resistor present, $V_{DD} = 5\text{ V}$	75	100	200	k Ω
Hysteresis	V_H	F, G and K ports, LCTR (period measurement mode)	$0.1 V_{DD}$	$0.2 V_{DD}$		V
Output high level voltage	$V_{OH}(1)$	B and C ports: $I_O = -1\text{ mA}$	$V_{DD} - 2.0$	$V_{DD} - 1.0$		V
	$V_{OH}(2)$	D, E, F, G, K, L, M, N, O, P and Q ports: $I_O = -1\text{ mA}$	$V_{DD} - 1.0$			V
	$V_{OH}(3)$	EO1, EO2, EO3, SUBPD: $I_O = -500\text{ }\mu\text{A}$	$V_{DD} - 1.0$			V
	$V_{OH}(4)$	XOUT: $I_O = -200\text{ }\mu\text{A}$	$V_{DD} - 1.0$			V
Output low level voltage	$V_{OL}(1)$	B and C ports: $I_O = 50\text{ }\mu\text{A}$		1.0	2.0	V
	$V_{OL}(2)$	D, E, F, G, K, L, M, N, O, P and Q ports: $I_O = 1\text{ mA}$			1.0	V
	$V_{OL}(3)$	EO1, EO2, EO3, SUBPD: $I_O = 500\text{ }\mu\text{A}$			1.0	V
	$V_{OL}(4)$	XOUT: $I_O = 200\text{ }\mu\text{A}$			1.5	V
	$V_{OL}(5)$	J port: $I_O = 5\text{ mA}$			2.0	V
Output off leakage current	$I_{OFF}(1)$	B, C, D, E, F, G, K, L, M, N, O, P and Q ports	-3.0		+3.0	μA
	$I_{OFF}(2)$	EO1, EO2, EO3, SUBPD	-100		+100	nA
	$I_{OFF}(3)$	J port	-5.0		+5.0	μA
A/D conversion error		ADI0 to ADI5: $V_{DD}(1)$	-1/2		+1/2	LSB
Reject pulse width	P_{REJ}	$\overline{\text{SNS}}$			50	μs
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Pull-down resistance	$R_{PD}(2)$	TEST1, TEST2		10		k Ω
Current drain	$I_{DD}(1)$	$V_{DD}(1)$: $f_{IN}(2) = 130\text{ MHz}$, $T_a = 25^\circ\text{C}$		12	24	mA
	$I_{DD}(2)$	$V_{DD}(2)$: Halt mode*, $T_a = 25^\circ\text{C}$ (Figure 1)		0.45	(0.9)	mA
	$I_{DD}(3)$	$V_{DD} = 5.5\text{ V}$, oscillator stopped, $T_a = 25^\circ\text{C}$ (Figure 2)			5	μA
	$I_{DD}(4)$	$V_{DD} = 2.5\text{ V}$, oscillator stopped, $T_a = 25^\circ\text{C}$ (Figure 2)			1	μA

Note: Execute 20 STEP instructions every 1 ms. With the PLL, counters and other functions all stopped.
() Value: LC72366

Test Circuit



Note: All of the pins PB to PG and PJ to PQ must be left open.
Here, the pins PE to PG, PK to PM, and PQ are selected for output.

Note: All of the pins PA to PQ must be left open.

Figure 1: $I_{DD}(2)$ in Halt ModeFigure 2: $I_{DD}(3)$ and $I_{DD}(4)$ in Backup Mode

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Pin Functions

Pin No.	Symbol	I/O	I/O type	Function
30 29 28 27	PA0 PA1 PA2 PA3	I	Pull-down resistor included Input	Key return signal input-only ports. The threshold voltage is set to a relatively low value. When a key matrix is formed in combination with the PB and PC ports, up to three simultaneous key presses can be detected. The pull-down resistors are set by the IOS instruction with PWn = 2 for all four pins at the same time and cannot be set on an individual pin basis. Input is disabled in clock stop mode.
26 25 24 23 22 21 20 19	PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	O	Unbalanced CMOS push-pull	Key source signal output-only ports. Since the output transistor circuit is an unbalanced CMOS structure, diodes to prevent shorting due to multiple key presses are not required. In clock stop mode, these pins go to the output high-impedance state. During the power-on reset, these pins go to the output high-impedance state and hold that state until an output instruction is executed.
18 17 16 15	PD0 PD1 PD2 PD3	O	CMOS push-pull	Output-only ports. In clock stop mode, these pins go to the output high-impedance state. During the power-on reset, these pins go to the output high-impedance state and hold that state until an output instruction is executed.
14 13 12 11 10 9 8 7 6 5 4 3	PE0 PE1/SCK2 PE2/SO2 PE3/SI2 PF0 PF1/SCK1 PF2/SO1 PF3/SI1 PG0 PG1/SCK0 PG2/SO0 PG3/SI0	I/O	CMOS push-pull	General-purpose I/O port/serial I/O pin shared-function ports. The F and G port inputs are Schmitt inputs. The E ports is a normal input. The IOS instruction switches these ports between general-purpose I/O ports and serial I/O ports, and between input and output for general-purpose I/O ports. • When used as general-purpose I/O ports these pins: Can be set for input or output in bit units (bit I/O), and are set for use as general-purpose I/O ports by the IOS instruction with PWn = 0. b0 = SI/O 0 0general-purpose port b1 = SI/O 1 1SI/O port b2 = SI/O 2 are set for input or output by the IOS instruction in bit units. PE.....PWn = 4 0Input PF.....PWn = 5 1Output PGPWn = 6 • When used as serial I/O ports these pins: Are set for serial I/O port use by the IOS instruction with PWn = 0, and are accessed by reading and writing the serial I/O data buffer with the INR and OUTR instructions. Note: Pin setup states when used as serial I/O ports: PE0, PF0, PG0General-purpose I/O PE1, PF1, PG1SCK output in internal clock mode SCK input in external clock mode PE2, PF2, PG2.....SO output PE3, PF3, PG3.....SI input In clock stop mode, input is disabled and these pins go to the high-impedance state. During the power-on reset, these pins become general-purpose input ports.
1 80	XIN XOUT	I O	—	Connections for a 4.5 MHz crystal oscillator
78 77	EO1 EO2	O	CMOS tristate	Main charge pump outputs These pins output a high level when the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, and a low level when that frequency is lower. These pins go to the high-impedance state when the frequencies match. These pins go to the high-impedance state when the HOLD pin is set low in the hold enable state. In clock stop mode, during the power-on reset and in the PLL stop state, these pins go to the high-impedance state.

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Pin No.	Symbol	I/O	I/O type	Function															
76 73 31	V_{SS} V_{DD} V_{DD}	—	—	Power supply connections															
75	FMIN	I	Input	FM VCO (local oscillator) input This pin is selected by the PLL instruction CW1 (b1, b0 are ignored). Capacitor coupling must be used for signal input. Input is disabled when the HOLD pin is set low in the hold enable state. Input is disabled in clock stop mode, during the power-on reset, and in the PLL stop state.															
74	AMIN	I	Input	AM VCO (local oscillator) input This pin is selected and the band set by the PLL instruction CW1 (b1, b0). <table border="1"><tr><td>b1</td><td>b0</td><td>Band</td></tr><tr><td>1</td><td>0</td><td>2 to 40 MHz (SW)</td></tr><tr><td>1</td><td>1</td><td>0.5 to 10 MHz (MW, LW)</td></tr></table> Capacitor coupling must be used for signal input. Input is disabled when the HOLD pin is set low in the hold enable state. Input is disabled in clock stop mode, during the power-on reset, and in the PLL stop state.	b1	b0	Band	1	0	2 to 40 MHz (SW)	1	1	0.5 to 10 MHz (MW, LW)						
b1	b0	Band																	
1	0	2 to 40 MHz (SW)																	
1	1	0.5 to 10 MHz (MW, LW)																	
72	SUBPD	O	CMOS tristate	Sub-charge pump output This pin, in combination with the main charge pump, allows the construction of a high-speed locking circuit. The DZC instruction controls the sub-charge pump. <table border="1"><tr><td>b3</td><td>b2</td><td>Operation</td></tr><tr><td>0</td><td>0</td><td>High impedance</td></tr><tr><td>0</td><td>1</td><td>Only operates in the unlocked state (450 kHz)</td></tr><tr><td>1</td><td>0</td><td>Only operates in the unlocked state (900 kHz)</td></tr><tr><td>1</td><td>1</td><td>Normal operation</td></tr></table> This pin goes to the high-impedance state when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state. This pin goes to the high-impedance state in clock stop mode, during the power-on reset, and in the PLL stop state.	b3	b2	Operation	0	0	High impedance	0	1	Only operates in the unlocked state (450 kHz)	1	0	Only operates in the unlocked state (900 kHz)	1	1	Normal operation
b3	b2	Operation																	
0	0	High impedance																	
0	1	Only operates in the unlocked state (450 kHz)																	
1	0	Only operates in the unlocked state (900 kHz)																	
1	1	Normal operation																	
71	EO3	O	CMOS tristate	Second PLL charge pump output This pin outputs a low level when the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, and a high level when that frequency is lower. This pin goes to the high-impedance state when the frequencies match. (Note that this pin's output logic is the opposite of that of the EO1 and EO2 pins.) This pin goes to the high-impedance state when the HOLD pin is set low in the hold enable state. This pin goes to the high-impedance state in clock stop mode, during the power-on reset, and in the PLL stop state.															

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Pin No.	Symbol	I/O	I/O type	Function
70	HCTR	I	Input	<p>Universal counter/general-purpose input shared-function input port</p> <p>The IOS instruction b3 with PWn = 3 switches the pin function between universal counter input and general-purpose input.</p> <ul style="list-style-type: none"> • Frequency measurement <p>The universal counter function is selected by an IOS instruction with PWn = 3 and b3 = 0. HCTR frequency measurement mode is set up by a UCS instruction with b3 = 0 and b2 = 0, and counting is started with a UCC instruction after the count time is selected. The CNTEND flag is set when the count completes.</p> <p>To operate this circuit as an AC amplifier in this mode, the input must be capacitor coupled.</p> <ul style="list-style-type: none"> • General-purpose input pin use <p>The general-purpose input port function is selected by an IOS instruction with PWn = 3 and b3 = 1.</p> <p>An internal register (address: 0EH) input instruction INR (b0) is used to acquire data from this pin.</p> <p>Input is disabled in clock stop mode. (The input pin will be pulled down.)</p> <p>During the power-on reset, the universal counter function is selected.</p>
69	LCTR	I	Input	<p>Universal counter (frequency and period measurement)/general-purpose input shared-function input port</p> <p>The IOS instruction b2 with PWn = 3 switches the pin function between universal counter input and general-purpose input.</p> <ul style="list-style-type: none"> • Frequency measurement <p>The universal counter function is selected by an IOS instruction with PWn = 3 and b2 = 0. LCTR frequency measurement mode is set up by a UCS instruction with b3 = 0 b2 = 1, and counting is started with a UCC instruction after the count time is selected. The CNTEND flag is set when the count completes.</p> <p>To operate this circuit as an AC amplifier in this mode, the input must be capacitor coupled.</p> <ul style="list-style-type: none"> • Period measurement <p>With the universal counter function selected, set up period measurement mode with a UCS instruction with b3 = 1 and b2 = 0, and start the count with a UCC instruction after selecting the count time. The CNTEND flag will be set when the count completes. In this mode, the signal must be input with DC coupling to turn off the bias feedback resistor.</p> <ul style="list-style-type: none"> • General-purpose input pin use <p>The general-purpose input port function is selected by an IOS instruction with PWn = 3, b2 = 1.</p> <p>An internal register (address: 0EH) input instruction INR (b1) is used to acquire data from this pin.</p> <p>Input is disabled in clock stop mode. (The input pin will be pulled down.)</p> <p>During the power-on reset, the universal counter function (in HCTR frequency measurement mode) is selected.</p>
68	$\overline{\text{SNS}}$	I	Input	<p>Voltage sense/general-purpose input pin shared-function port</p> <p>This circuit is designed for a relatively low input threshold voltage.</p> <ul style="list-style-type: none"> • Voltage sense pin usage <p>This input pin is used to determine whether or not a power failure occurred after recovery from backup (clock stop) mode. An internal sense F/F is used for this determination. The sense F/F is tested with a TUL instruction (b2).</p> <ul style="list-style-type: none"> • General-purpose input port usage <p>When used as a general-purpose input port, the state is sensed by using a TUL instruction (b3).</p> <p>Since, unlike other input ports, input is not disabled in clock stop mode and during the power-on reset, special care is required with respect to through currents.</p>

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Pin No.	Symbol	I/O	I/O type	Function
67	$\overline{\text{HOLD}}$	I	Input	<p>PLL control and clock stop mode control</p> <p>Setting this pin low in the hold enabled state disables input to the FMIN and AMIN pins and sets the EO pin to the high-impedance state.</p> <p>To enter clock stop mode, set the HOLDEN flag, set this pin low, and execute a CKSTP instruction.</p> <p>To clear clock stop mode, set this pin high.</p>
66 65 64 63 62 61	PH0/ADI0 PH1/ADI1 PH2/ADI2 PH3/ADI3 PI0/ADI4 PI1/ADI5	I	Input	<p>General-purpose input port/A/D converter shared-function pins</p> <p>The IOS instruction with PWn = 7 or 8 switches the pin function between general-purpose input ports and A/D converter inputs.</p> <ul style="list-style-type: none"> General-purpose input port usage Specify general-purpose input port usage with the IOS instruction with PWn = 7 or 8 in bit units. A/D converter usage Specify A/D converter usage with the IOS instruction with PWn = 7 or 8 in bit units. Specify the pin to convert with the IOS instruction with PWn = 1. Start a conversion with the UCC instruction (b2). The ADCE flag will be set when the conversion completes. <p>Note: Executing an input instruction for a port specified for ADI usage will always return low since input is disabled. These pins must be set up for general-purpose input port usage before an input instruction is executed.</p> <p>Input is disabled in clock stop mode.</p> <p>During the power-on reset, these pins go to the general-purpose input port function.</p>
60 59 58 57	PJ0 PJ1 PJ2 PJ3	O	N-channel open drain	<p>General-purpose output ports</p> <p>An external pull-up resistor is required since these pins are open-drain circuits.</p> <p>In clock stop mode, these pins go to the transistor off state (high level output).</p> <p>During the power-on reset, these pins are set up as general-purpose output ports and go to the transistor off state (high level output).</p>
56 55 54 53	PK0/INT0 PK1/INT1 PK2 PK3	I/O	CMOS push-pull	<p>General-purpose I/O/external interrupt shared-function ports</p> <p>There is no instruction that switches the function of these ports between general-purpose ports and external interrupt ports. These pins function as external interrupt pins at the point that the external interrupt enable flag is set.</p> <ul style="list-style-type: none"> General-purpose I/O port usage These pins can be set for input or output in bit units (bit I/O). The IOS instruction is used to specify input or output in bit units. External interrupt pin usage This function can be used by setting the external interrupt enable flags (INT0EN and INT1EN) in status register 2. The corresponding pin must be set up for input. To enable interrupt operation, the interrupt enable flag (INTEN) in status register 1 also must be set. The IOS instruction with PWn = 3, b1 = INT1, and b0 = INT0 is used to select rising or falling edge detection. <p>In clock stop mode, input is disabled and these pins go to the high impedance state.</p> <p>During the power-on reset, these pins function as general-purpose input ports.</p>
52 to 45	PL0 to PL3 PM0 to PM3	I/O	CMOS push-pull	<p>General-purpose I/O ports</p> <p>The IOS instruction is used to specify input or output.</p> <p>In clock stop mode input is disabled and these pins go to the high impedance state.</p> <p>During the power-on reset, these pins function as general-purpose input ports.</p>

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Pin No.	Symbol	I/O	I/O type	Function
44 43 42 41	PN0/BEEP PN1 PN2 PN3	O	CMOS push-pull	<p>General-purpose output port/BEEP tone shared-function output pins The BEEP instruction switches between the general-purpose output port and BEEP tone functions.</p> <ul style="list-style-type: none"> General-purpose output port usage The BEEP instruction with b3 = 0 sets up the general-purpose output port function. Pins PN1 to PN3 are general-purpose output-only pins. BEEP output usage The BEEP instruction with b3 = 1 sets up BEEP output. The BEEP instruction bits b0, b1 and b2 sets the frequency. When set up as the BEEP port, executing an output instruction will set the internal latch data but has no influence on the output. These pins go to the output high-impedance state in clock stop mode. These pins go to the output high-impedance state during the power-on reset and hold that state until an output instruction is executed.
40 to 33	PO0 to PO3 PP0 to PP3	O	CMOS push-pull	<p>Output-only ports These pins go to the output high-impedance state in clock stop mode. These pins go to the output high-impedance state during the power-on reset and hold that state until an output instruction is executed.</p>
32	PQ0	I/O	CMOS push-pull	<p>General-purpose I/O ports The IOS instruction is used to specify input or output. The OUTF and INR instructions are used for output and input. The bit set, reset and test instruction cannot be used. In clock stop mode input is disabled and these pins go to the high impedance state. During the power-on reset, these pins function as general-purpose input ports.</p>
79 2	TEST1 TEST2			<p>LSI test pins These pins must be either left open or connected to ground.</p>

LC72358N, LC72362N and LC72366 Instruction Table

Abbreviations:

ADDR: Program memory address

b: Borrow

C: Carry

 D_H : Data memory address high (row address): 2 bits D_L : Data memory address low (column address): 4 bits

I: Immediate data: 4 bits

M: Data memory address

N: Bit position

Pn: Port number: 4 bits

PWn: Port control word number: 4 bits

r: General register (one of banks 00 to 0FH)

Rn: Register number: 4 bits

(): Contents of register or memory

()N: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15 14 13 12				11 10		9 8		7 6 5 4				3 2 1 D0			
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0	1	0	0	0	0	D_H		D_L				r			
	ADS	r	M	Add M to r, then skip if carry	$r \leftarrow (r) + (M)$ skip if carry	0	1	0	0	0	1	D_H		D_L				r			
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0	1	0	0	1	0	D_H		D_L				r			
	ACS	r	M	Add M to r with carry, then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0	1	0	0	1	1	D_H		D_L				r			
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	D_H		D_L				I			
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ skip if carry	0	1	0	1	0	1	D_H		D_L				I			
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	D_H		D_L				I			
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ skip if carry	0	1	0	1	1	1	D_H		D_L				I			
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0	1	1	0	0	0	D_H		D_L				r			
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ skip if borrow	0	1	1	0	0	1	D_H		D_L				r			
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0	1	1	0	1	0	D_H		D_L				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ skip if borrow	0	1	1	0	1	1	D_H		D_L				r			
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	D_H		D_L				I			
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ skip if borrow	0	1	1	1	0	1	D_H		D_L				I			
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	D_H		D_L				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ skip if borrow	0	1	1	1	1	1	D_H		D_L				I			
Comparison instructions	SEQ	r	M	Skip if r equal to M	$(r) - M$ skip if zero	0	0	0	1	0	0	D_H		D_L				r			
	SEQI	M	I	Skip if M equal to I	$(M) - I$ skip if zero	0	0	0	1	0	1	D_H		D_L				I			
	SNEI	M	I	Skip if M not equal to I	$(M) - I$ skip if not zero	0	0	0	0	0	1	D_H		D_L				I			
	SGE	r	M	Skip if r is greater than or equal to M	$(r) - M$ skip if not borrow	0	0	0	0	1	1	D_H		D_L				r			
	SGEI	M	I	Skip if M is greater than or equal to I	$(M) - I$ skip if not borrow	0	0	0	1	1	1	D_H		D_L				I			
	SLEI	M	I	Skip if M is less than I	$(M) - I$ skip if zero	0	0	0	0	1	1	D_H		D_L				I			

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Instruction Group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0												
Logical operation instructions	AND	r	M	AND M with r	$r \leftarrow (r) \text{ AND } (M)$	0 0 1 0	0 0	D _H	D _L	r											
	ANDI	M	I	AND I with M	$M \leftarrow (M) \text{ AND } I$	0 0 1 0	0 1	D _H	D _L	I											
	OR	r	M	OR M with r	$r \leftarrow (r) \text{ OR } (M)$	0 0 1 0	1 0	D _H	D _L	r											
	ORI	M	I	OR I with M	$M \leftarrow (M) \text{ ORI}$	0 0 1 0	1 1	D _H	D _L	I											
	EXL	r	M	Exclusive OR M with r	$r \leftarrow (r) \text{ XOR } (M)$	0 0 1 1	0 0	D _H	D _L	r											
	EXLI	M	I	Exclusive OR I with M	$M \leftarrow (M) \text{ XOR } I$	0 0 1 1	0 1	D _H	D _L	I											
	SHR	r		Shift r right with carry		0 0 0 0	0 0	0 0	1 1 1 0	r											
Transfer instructions	LD	r	M	Load M to r	$r \leftarrow (M)$	1 1 0 1	0 0	D _H	D _L	r											
	ST	M	r	Store r to M	$M \leftarrow (r)$	1 1 0 1	0 1	D _H	D _L	r											
	MVRD	r	M	Move M to destination M referring to r in the same row	$[D_H, r_n] \leftarrow (M)$	1 1 0 1	1 0	D _H	D _L	r											
	MVRS	M	r	Move source M referring to r to M in the same row	$M \leftarrow [D_H, r_n]$	1 1 0 1	1 1	D _H	D _L	r											
	MVSR	M1	M2	Move M to M in the same row	$[D_H, D_L1] \leftarrow [D_H, D_L2]$	1 1 1 0	0 0	D _H	D _{L1}	D _{L2}											
	MVI	M	I	Move I to M	$M \leftarrow I$	1 1 1 0	0 1	D _H	D _L	I											
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1 1 1 1	0 0	D _H	D _L	N											
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1 1 1 1	0 1	D _H	D _L	N											
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	$PC \leftarrow ADDR$	1 0	ADDR (14 bits)														
	CAL	ADDR		Call subroutine	$Stack \leftarrow (PC) + 1$	1 1 0 0	ADDR (12 bits)														
	RT			Return from subroutine	$PC \leftarrow Stack$	0 0 0 0	0 0 0 0	1 0 0 0													
	RTS			Return from subroutine and skip	$PC \leftarrow Stack + 1$	0 0 0 0	0 0 0 0	1 0 1 0													
	RTB			Return from subroutine with bank data	$PC \leftarrow Stack$ $BANK \leftarrow Stack$	1 1 1 1	1 1 1 1	1 1 0 0													
	RTBS			Return from subroutine with bank data and skip	$PC \leftarrow Stack + 1$ $BANK \leftarrow Stack$	1 1 1 1	1 1 1 1	1 1 0 1													
	RTI			Return from interrupt	$PC \leftarrow Stack$ $BANK \leftarrow Stack$ $Carry \leftarrow Stack$	0 0 0 0	0 0 0 0	1 0 0 1													
Status register instructions	SS	I	N	Set status register	(Status reg I) $N \leftarrow 1$	1 1 1 1	1 1 1 1	0 0 0	I	N											
	RS	I	N	Reset status register	(Status reg I) $N \leftarrow 0$	1 1 1 1	1 1 1 1	0 0 1	I	N											
	TST	I	N	Test status register true	if (Status reg I) N = all 1, then skip	1 1 1 1	1 1 1 1	0 1	I	N											
	TSF	I	N	Test status register false	if (Status reg I) N = all 0, then skip	1 1 1 1	1 1 1 1	1 0	I	N											

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Instruction Group	Mnemonic	Operand		Function	Operation	Machine code																	
		1st	2nd			D15 14 13 12				11 10 9 8				7 6 5 4				3 2 1 D0					
F/F test instructions	TUL	N		Test unlock F/F then skip if it has not been set	if unlock FF (N) = 0, then skip	0	0	0	0	0	0	0	0	0	0	1	1	0	1	N			
Internal register transfer instructions	PLL	M	r	Load M to PLL registers	PLL reg ← PLL data	1	1	1	1	1	0		D _H		D _L	r							
	INR	M	Rn	Input register/port data to M	M ← (Rn reg)	0	0	1	1	1	0		D _H		D _L	Rn							
	OUTR	M	Rn	Output contents of M to register/port	Rn reg ← (M)	0	0	1	1	1	1		D _H		D _L	Rn							
Hardware control instructions	SIO	I1	I2	Serial I/o control	SIO reg ← I1, I2	0	0	0	0	0	0	0	1		I1		I2						
	UCS	I		Set I to UCCW1	UCCW1 ← I	0	0	0	0	0	0	0	0	0	0	0	1		I				
	UCC	I		Set I to UCCW2	UCCW2 ← I	0	0	0	0	0	0	0	0	0	0	1	0		I				
	BEEP	I		Beep control	Beep reg ← I	0	0	0	0	0	0	0	0	0	1	1	0		I				
	DZC	I		Data zone control	DZC reg ← I	0	0	0	0	0	0	0	0	1	0	1	1		I				
	TMS	N		Set timer register	Timer reg ← I	0	0	0	0	0	0	0	0	1	1	0	0		N				
	IOS	PWn	N	Set port control word	IOS reg PWn ← N	1	1	1	1	1	1	1	0		PWn		N						
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1	1	1	0	1	0		D _H		D _L	Pn							
	OUT	M	Pn	Output contents of M to port	Pn ← M	1	1	1	0	1	1		D _H		D _L	Pn							
	SPB	Pn	N	Set port bits	(Pn) N ← 1	0	0	0	0	0	0	1	0		Pn	N							
	RPB	Pn	N	Reset port bits	(Pn) N ← 0	0	0	0	0	0	0	1	1		Pn	N							
	TPT	Pn	N	Test port bits, then skip if all bits specified are true	if (Pn) N = all 1, then skip	1	1	1	1	1	1	0	0		Pn	N							
	TPF	Pn	N	Test port bits, then skip if all bits specified are false	if (Pn)) N = all 0, then skip	1	1	1	1	1	1	0	1		Pn	N							
	TPF	Pn	N	Test port bits, then skip if all bits specified are false	if (Pn)) N = all 0, then skip	1	1	1	1	1	1	0	1		Pn	N							
Bank switching instructions	BANK	I		Select bank	BANK ← I	0	0	0	0	0	0	0	0	0	1	1	1		I				
Other instructions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0	0	0	0	0	0	0	0	0	1	0	0		I				
	CKSTP			Clock stop	Stop Xtal OSC if HOLD = 0	0	0	0	0	0	0	0	0	0	1	0	1						
	NOP			No operation	No operation	0	0	0	0	0	0	0	0	0	0	0	0	0					

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