

SANYO

No. 3269

LC7440CMOS-LSI
PIP controller

The LC7440 CMOS LSI chip is a memory controller of the PIP (Picture In Picture) system for the TV and VCR.

The LC7440 has three internal DA converters. So, if the LSI is used together with the AD converter (LC7480) and a memory, a component type PIP system can be configured.

Features

1. Three internal DA converters (Y, R-Y, B-Y)
2. Vertical filter function and high-quality frame display
3. On-chip odd/even field selector
4. On-chip PLL circuit (external VCO)
5. For controlling NTSC/PAL-system TV/VCR applications
6. Sub-screen specifications

(1) Display mode

Single screen mode - Frame display: motion and still pictures

Dual screen mode - Field display: motion and still pictures

(2) Display ON/OFF switch, frame ON/OFF/color switch and wipe functions

(3) Display position select function: Fixed position (4 corners) or a desired position (6-bit vertical and horizontal positioning data)

(4) Size (with respect to main screen): one-third (vertical), one-third (horizontal), and one-ninth (area)

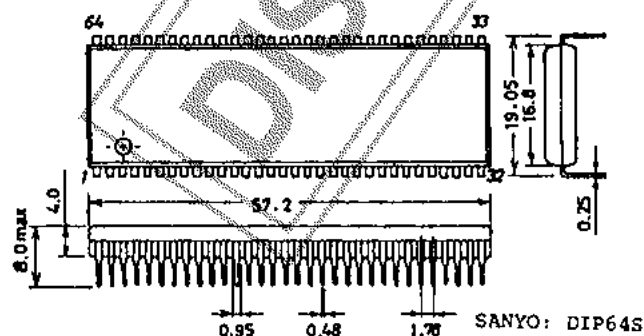
(5) Horizontal resolution (y signal): approximately 120 dots

(6) Tone reproduction: 64 (6 bits)

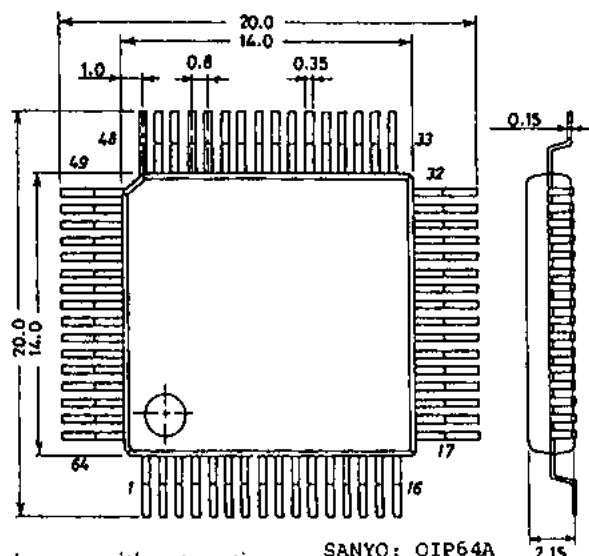
7. Operational supply voltage: $5V \pm 10\%$

8. Packaging: QIP64, DIP64S

Case Outline 3071-D641C
(unit:mm)



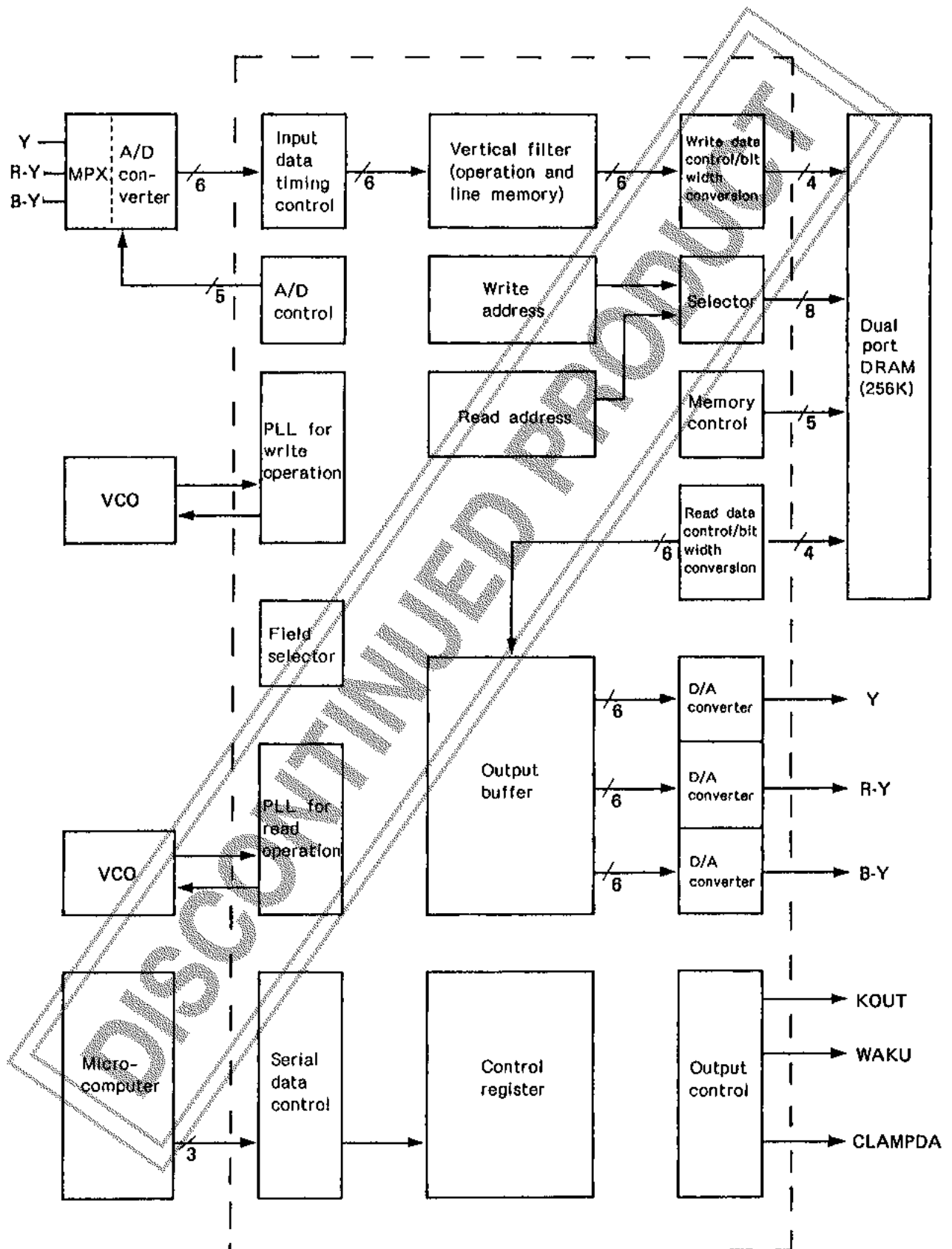
Case Outline 3057-Q64A1C
(unit:mm)



Specifications and information herein are subject to change without notice.

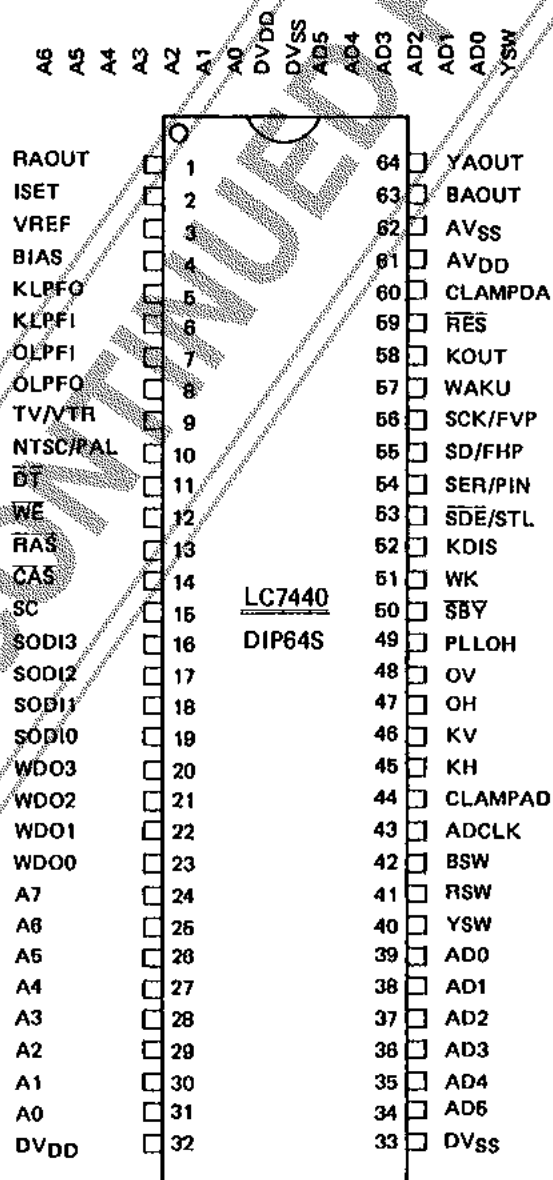
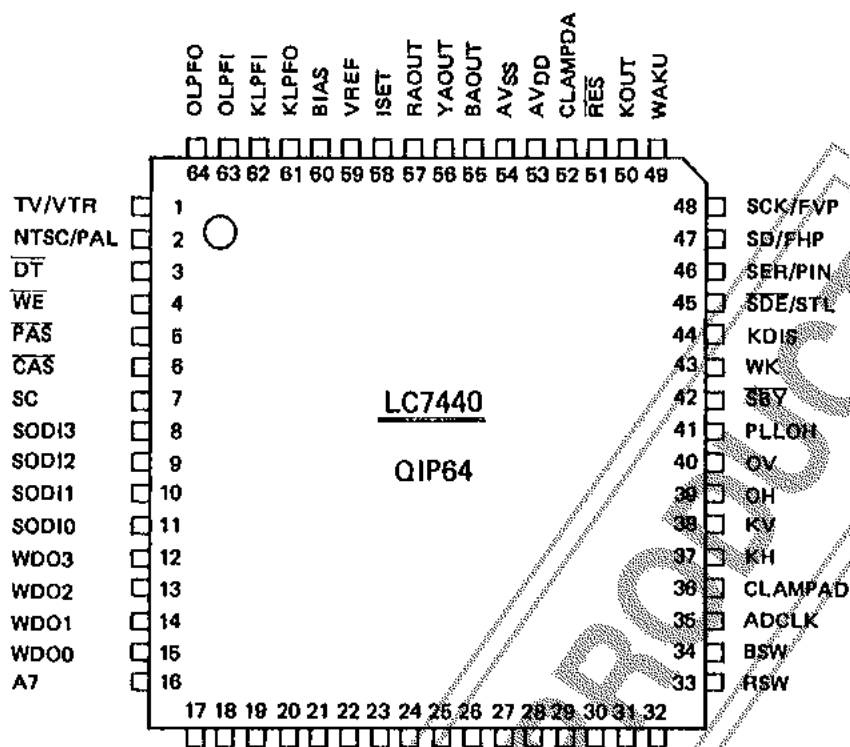
SANYO Electric Co., Ltd. Semiconductor Overseas Marketing Div.
Natsume Bldg., 18-6, 2-chome, Yushima, Bunkyo-ku, TOKYO 113 JAPAN

LC7440 functional block diagram



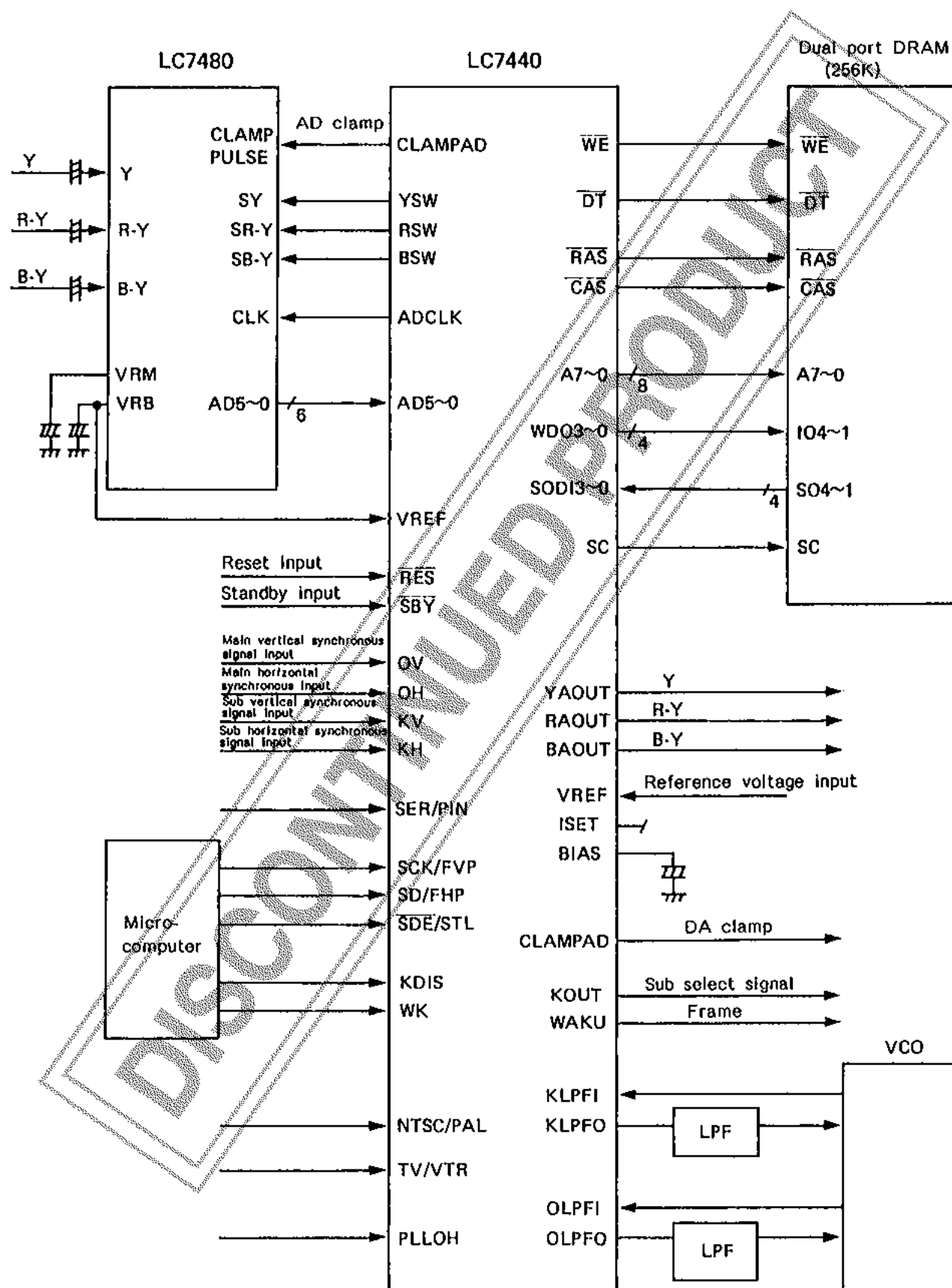
LC7440

Pin assignment

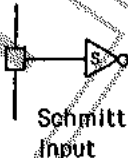
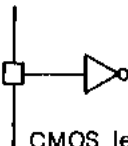
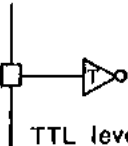
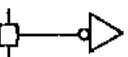
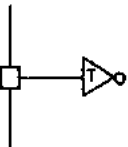
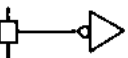
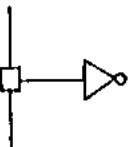


LC7440

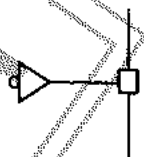

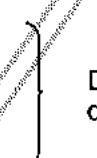
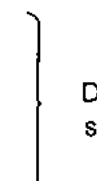
Component type PIP system configuration with the LC7440 and LC7480



Input pins

Pin No.		Pin name	Connected to:	Functional description	Circuit type
QIP	DIP				
40	48	OV	Synchronous separation IC Same as above	Main screen vertical synch. signal	
39	47	OH		Main screen horizontal synch. signal	
38	46	KV	Same as above	Sub screen vertical synch. signal	
37	45	KH	Same as above	Sub screen horizontal synch. signal	
46	54	SER/PIN	V_{DD} or V_{SS}	Serial data or pin function selection	
48	56	SCK/FVP	Microcomputer	Serial data clock/vertical control for four corner positions	
47	55	SD/FHP	Same as above	Serial data/horizontal control for four corner positions	
45	53	\overline{SDE} /STL	Same as above	Serial data enable/still	
2	10	NTSC/PAL	V_{DD} or V_{SS}	NTSC/PAL system select	
1	9	TV/VTR	Same as above	TV/VCR select	
26	34	AD5	LC7480	MSB } Sampled six-bit wide digital data } LSB	
27	35	AD4	LC7480		
28	36	AD3	LC7480		
29	37	AD2	LC7480		
30	38	AD1	LC7480		
31	39	AD0	LC7480		
42	50	\overline{SBY}	—	Standby Input (forces the PLL oscillation circuit to stop)	
8	16	SODI3	Memory	} Serial output data from memory }	
9	17	SODI2	Memory		
10	18	SODI1	Memory		
11	19	SODI0	Memory		
51	59	\overline{RES}	—	Reset input (forces all the functional blocks to stop)	
44	52	KDIS	—	Sub screen display ON/OFF	
43	51	WK	—	D/A converter frame signal output ON/OFF	
41	49	PLLOH	—	Horizontal synch. signal selection for sub screen display positions	

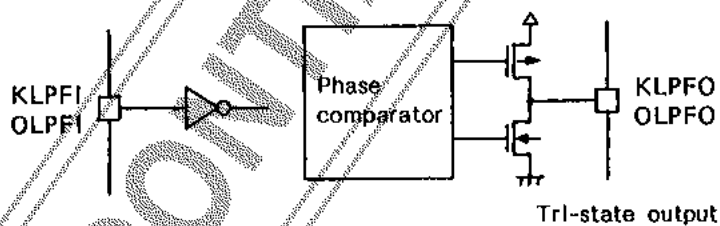
Output pins

Pin No.		Pin name	Connected to:	Functional description	Circuit type
QIP	DIP				
32	40	YSW	LC7480	MPX control	
33	41	RSW	LC7480	Same as above	
34	42	BSW	LC7480	Same as above	
35	43	ADCLK	LC7480	Sampling clock	
56	64	YAOUT	_____	Y signal analog output (D/A)	
57	1	RAOUT	_____	R-Y signal analog output (D/A)	
55	63	BAOUT	_____	B-Y signal analog output (D/A)	
50	58	KOUT		Sub/Main screen selection signal output	
49	57	WAKU		Frame signal output	
16	24	A7	Memory	MSB	
17	25	A6	Same as above		
18	26	A5	Same as above		
19	27	A4	Same as above		
20	28	A3	Same as above		
21	29	A2	Same as above		
22	30	A1	Same as above		
23	31	A0	Same as above	LSB	
12	20	WDO3	Same as above	Dual port memory write data signals	
13	21	WDO2	Same as above		
14	22	WDO1	Same as above		
15	23	WDO0	Same as above		
5	13	$\overline{\text{RAS}}$	Same as above	Dual port memory control signals	
6	14	$\overline{\text{CAS}}$	Same as above		
4	12	$\overline{\text{WE}}$	Same as above		
3	11	$\overline{\text{DT}}$	Same as above		
7	15	SC	Same as above		
36	44	CLAMPAD	LC7480	Clamp pulse signal for A/D conversion	
52	60	CLAMPDA		Clamp pulse signal for D/A converter output	

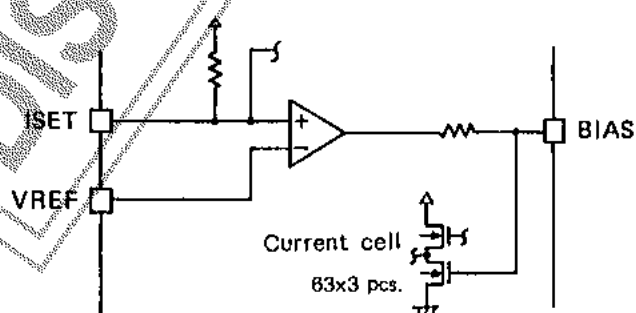
Other pins

Pin No.		Pin name	Connected to:	I/O	Functional description	Circuit type
QIP	DIP					
24	32	DV _{DD}			Power supply for digital functional block	
25	33	DV _{SS}				
53	61	AV _{DD}			Power supply for analog functional block	
54	62	AV _{SS}				
62	8	KLPIFI		I	VCO clock input	Sub screen synch. PLL
61	5	KLPFO		O	Charge pump output	
63	7	OLPIFI		I	VCO clock input	Main screen synch. PLL
64	8	OLPFO		O	Charge pump output	
60	4	BIAS	Capacitor Left open LC7480		D/A converter setting pins	Refer to Note 2.
58	2	ISET				
59	3	VREF				

Note 1



Note 2



Electrical characteristics

Absolute maximum ratings/ $T_a=25 \pm 2^\circ\text{C}$, $V_{SS}=0\text{V}$

			unit
Maximum supply voltage	V_{DD}	-0.3 to +7.0	V
	AV_{DD}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{DD}+0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{DD}+0.3$	V
Maximum power dissipation	P_D	500	mW
Operating temperature	T_{OP}	-10 to +70	$^\circ\text{C}$
Storage temperature	T_{ST}	-55 to +125	$^\circ\text{C}$

Allowable operating conditions/ $T_a=-10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{SS}=0\text{V}$

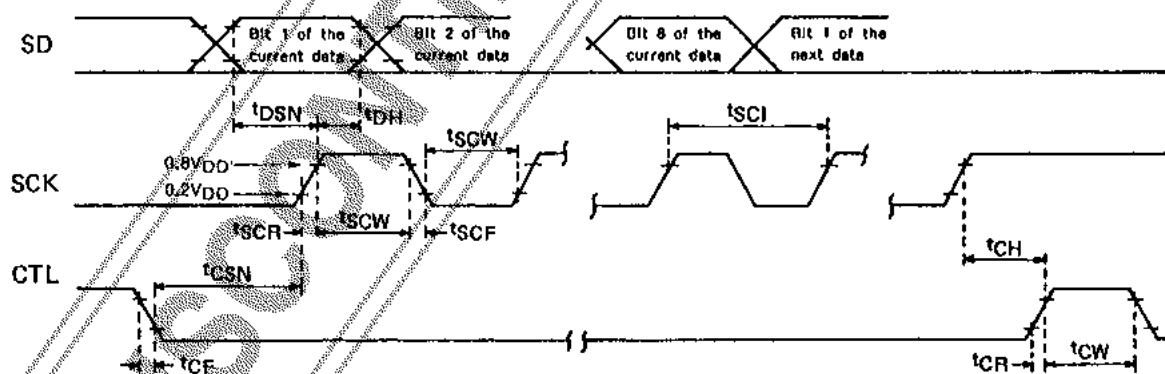
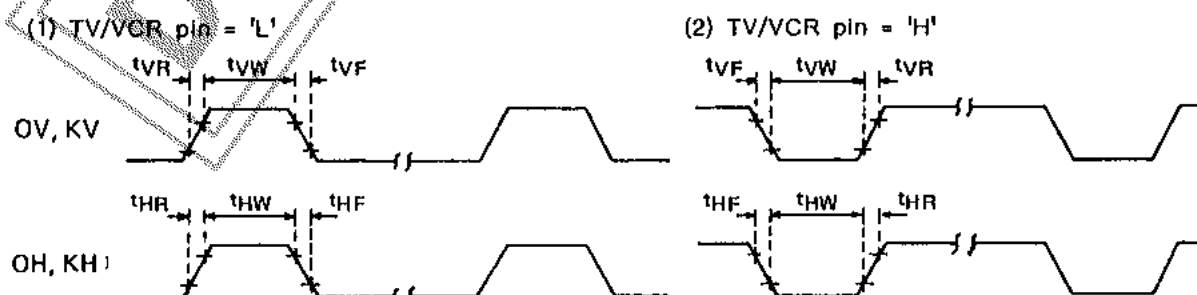
		min	typ	max	unit	Remarks
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
	AV_{DD}	4.5	5.0	5.5	V	
High-level input voltage	V_{IH1}	2.2			V	TTL level
	V_{IH2}	$0.7V_{DD}$			V	CMOS level
Low-level input voltage	V_{IL1}			0.6	V	TTL level
	V_{IL2}			$0.3V_{DD}$	V	CMOS level
Reference voltage	V_{REF}		$AV_{DD}-1$	AV_{DD}	V	
Phase compensation capacitance	C_{BS}		1		μF	

Electrical characteristics/ $T_a=25 \pm 2^\circ\text{C}$, $V_{DD}=5\text{V} \pm 10\%$, $V_{SS}=0\text{V}$

		min	typ	max	unit	Remarks
High-level output voltage	V_{OH1}	$I_{OH}=-0.8\text{mA}$	2.4		V	Except for KLPFO and OLPFO
	V_{OH2}	$I_{OH}=-1.0\text{mA}$	$V_{DD}-1$		V	KLPFO, OLPFO
Low-level output voltage	V_{OL1}	$I_{OL}=4\text{mA}$		0.4	V	Except for KLPFO and OLPFO
	V_{OL2}	$I_{OL}=1.0\text{mA}$		1	V	KLPFO, OLPFO
Operating current dissipation (by digital blocks)	I_{DD}	$\overline{RES}, \overline{SBY}=V_{DD}$ $0\text{V}, K_V=60\text{Hz}$ $0\text{H}, K_H=15\text{kHz}$ $KLPFI, OLPI=20\text{MHz}$	20		mA	No output load
Operating current dissipation (by analog blocks)	I_{DDA}	$\overline{RES}, \overline{SBY}=V_{DD}$ $0\text{V}, K_V=60\text{Hz}$ $0\text{H}, K_H=15\text{kHz}$	20		mA	No output load
Static current dissipation	$I_{DD(S)}$	$\overline{RES}, \overline{SBY}=V_{SS}$		10	μA	
Leakage current at input	I_{IH}, I_{IL}		-1	1	μA	
Leakage current at output	I_{OZ}	$V_I=V_{DD}, V_{SS}$	0.1	0.01	μA	KLPFO, OLPFO
D/A output impedance	DAR			150	Ω	YAOUT RAOUT BAOUT

Switching characteristics/ $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=5V\pm 10\%$, $V_{SS}=0V$

		min	typ	max	unit
Vertical synch. signal					
Pulse width	t_{VW}	1			μs
Rise time	t_{VR}			50	ns
Fall time	t_{VF}			50	ns
Horizontal synch. signal					
Pulse width	t_{HW}	1			μs
Rise time	t_{HR}			50	ns
Fall time	t_{HF}			50	ns
Serial data interface signals					
Serial clock					
Pulse width	t_{SCW}	200			ns
Rise time	t_{SCR}	50			ns
Fall time	t_{SCF}	50			ns
Data setup time	t_{DSU}	100			ns
Data hold time	t_{DH}	30			ns
Interval time	t_{SCI}	2			μs
Control signals					
Pulse width	t_{CW}	200			ns
Rise time	t_{CR}	50			ns
Fall time	t_{CF}	50			ns
Setup time	t_{CSU}	200			ns
Hold time	t_{CH}	200			ns

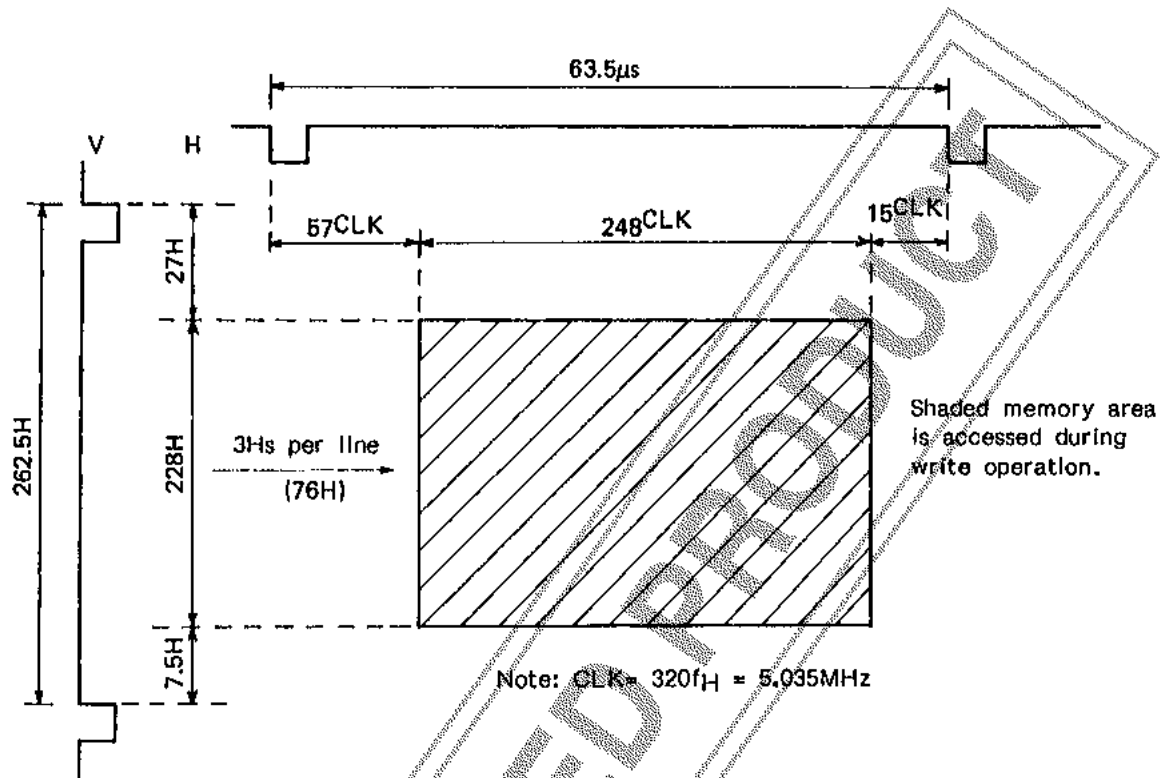
Serial data**Synch. signals**

Digital processing specifications for sub screen

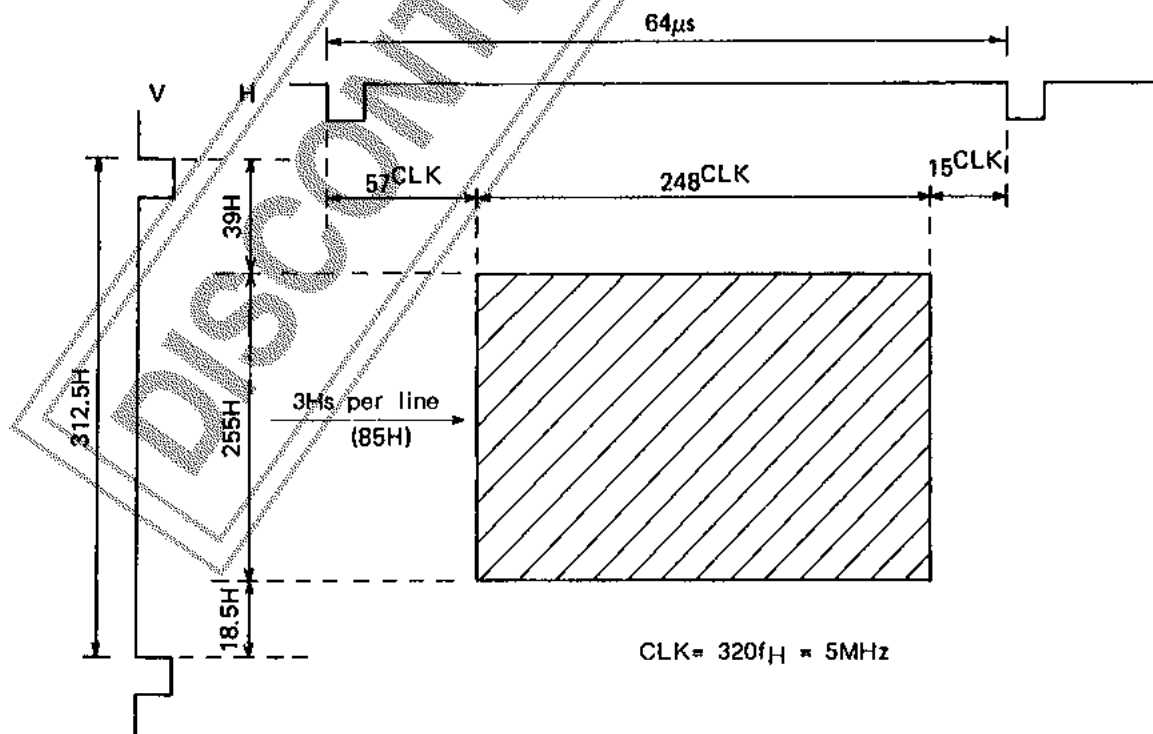
		NTSC ($f_H=15734\text{Hz}$)	PAL ($f_H=15625\text{Hz}$)
Sampling	Sequence	Y, R-Y, Y, B-Y, Y	
	Frequency	$320f_H$	
	$f_T(\text{Hz})$	5.035	5.000
	Y only	$160f_H$	
	f_{TY}	2.517	2.500
	R-Y only	$80f_H$	
	f_{TR}	1.258	1.250
	B-Y only	$80f_H$	
	f_{TB}	1.258	1.250
Quantization bit count		6 bits	
DA converter clock (MHz)	Y signal only	$480f_H$	
	f_{CY}	7.552	7.500
	R-Y signal only	$240f_H$	
	f_{CR}	3.776	3.750
Write	B-Y signal only	$240f_H$	
	f_{CB}	3.776	3.750
	Horizontal dot count	252	
	Y only	126	
	R-Y only	63	
Read and Display	B-Y only	63	
	Vertical H count	80	85
	Horizontal dot count	244	
	Y only	122	
	R-Y only	61	
	B-Y only	61	
	Horizontal H count	77	83

Memory write range

<NTSC>

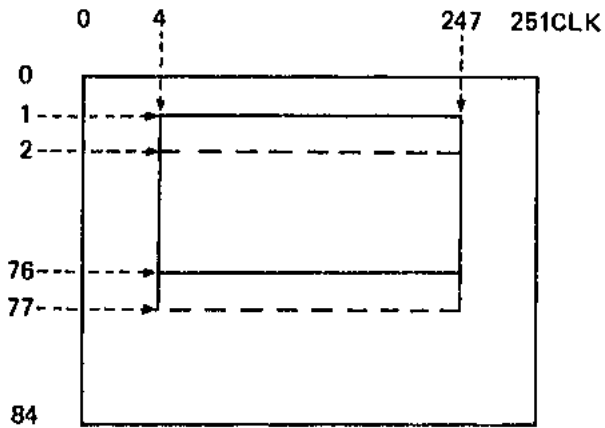


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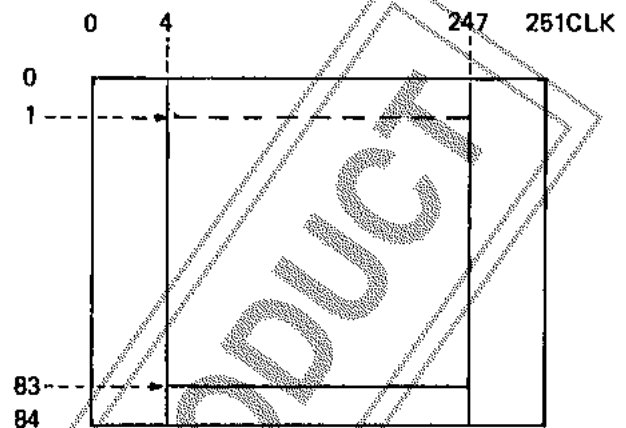


Memory read range

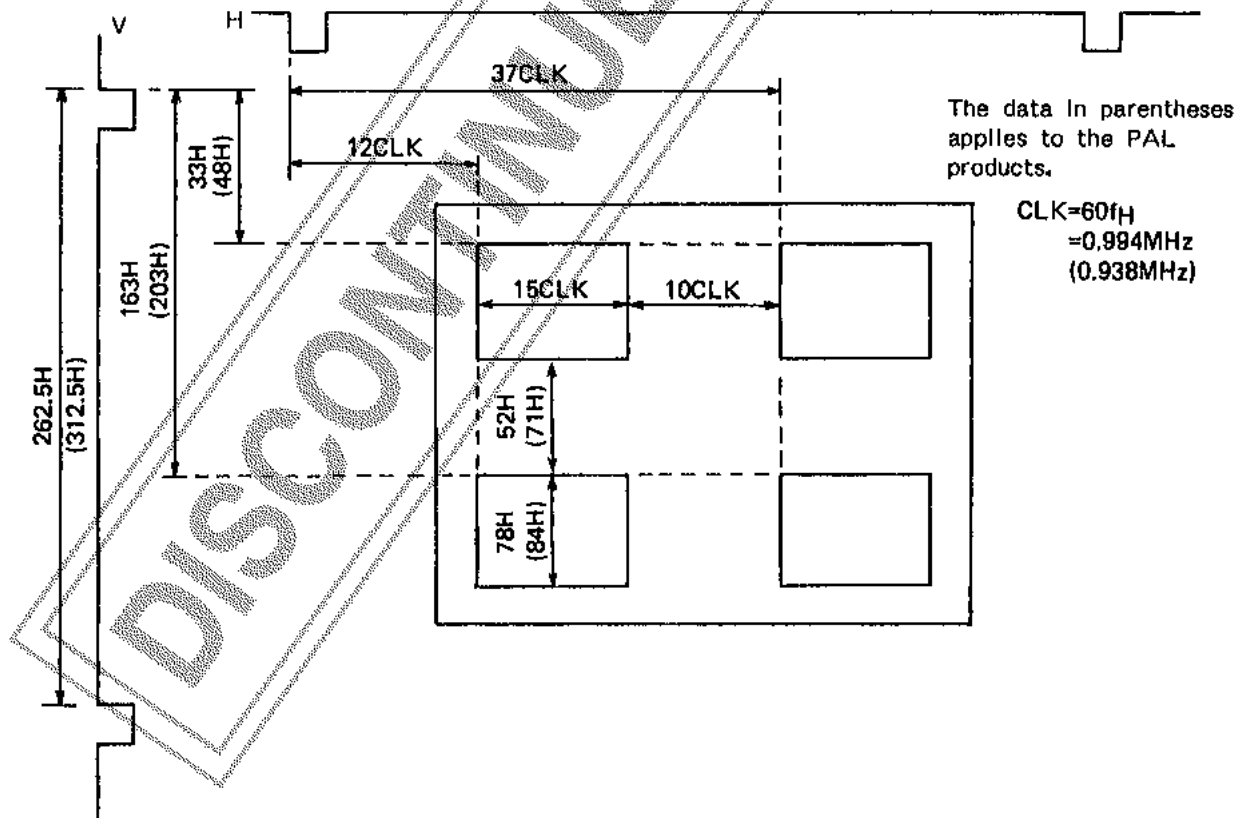
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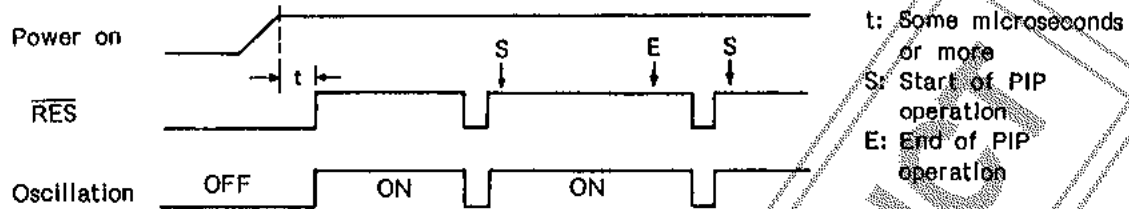
Sub screen display positioning (multiple four-corner screens)



On Initialization

(1) $\overline{\text{RES}}$ pin - Reset input

The $\overline{\text{RES}}$ pin should be set to the 'L' level at power-on and before the PIP operation is started. The internal control registers are set as shown in the table below.

(2) $\overline{\text{SBY}}$ pin - Standby input

The $\overline{\text{SBY}}$ pin has the same functions as those of the $\overline{\text{RES}}$ pin except for the initial data of the internal control registers. Note that the SBY register can be used to force the system into the standby mode.

Initial data

Internal register	Reset	Standby
SBY	L	H
WKVAR WKVAR1,2	L	-
FILD	L	-
KOUT KOUT1,2	KDIS	KDIS
POSVAR	L	-
STL STL1,2	SDE/STL	SDE/STL
FVPR	SCK/FVP	SCK/FVP
FHPR	SD/FHP	SD/FHP
PRI	H	-
VWIPE	L	-
HWIPE	L	-
VP5 to 0	-	-
HP5 to 0	-	-
WK1,2	WK	-
VDFS1	L	-
VDFS0	H	-
Ywk5 to 0	-	-
Rwk5 to 0	-	-
Bwk5 to 0	-	-

Note: H: VDD level
L: VSS level
-: Previous data

KDIS and other pins: Level of corresponding input pins.

Example: If the level of the KDIS pin is 'L' with the $\overline{\text{RES}}$ pin already set to 'L', the Kout, and Kout 1 and 2 registers will have an 'L' level logic.

Sub screen display setting

(1) Pin setting (one screen mode only, SER/PIN = 'L')

Pin name	Functional Description
SCK/FVP SD/FHP	<div>Screen</div> <div> <div>{0, 0}</div> <div>{0, 1}</div> <div>{1, 0}</div> <div>{1, 1}</div> </div> <div>Fixed positions (four corners) selection (SCK/FVP, SD/FHP)</div>
KDIS	<div>[H: Sub screen display ON</div> <div>[L: Sub screen display OFF</div>
SDE/STL	<div>[H: Still picture</div> <div>[L: Motion picture</div>
WK	<div>[H: DAC frame output ON</div> <div>[L: DAC frame output OFF</div> <div>The output color is fixed (note 1).</div>

Note: DAC frame output - Frame color data is output from the DAC converter.
The pulse output from the WAKU pin is always active during sub screen display.
All these pin settings become invalid when serial data transmission is started.

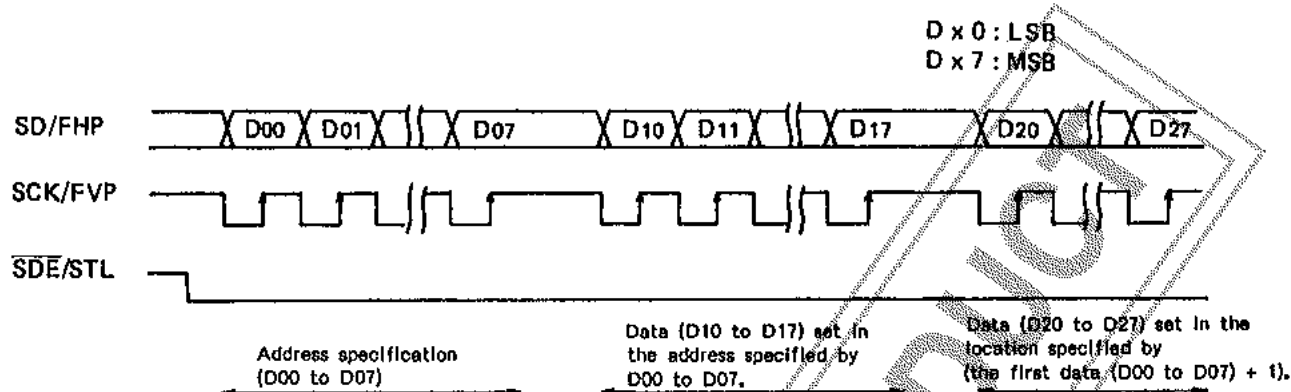
(2) Serial data control and Pin control (SER/PIN pin)

Use of the SER/PIN pin enables the following pin functions to be selected.

Pin name	SER/PIN	
	H	L
SCK/FVP	Serial data clock	Vertical control for four-corner positioning
SD/FHP	Serial data (LSB first)	Horizontal control for four-corner positioning
SDE/STL	Serial data enable	Still picture
KDIS	Sub screen display ON/OFF Initialization at reset	Sub screen display ON/OFF
WK	DAC frame output ON/OFF Initialization at reset	DAC frame output ON/OFF

Serial data interface

(1) Serial input format (SER/PIN = 'H')



When the $\overline{\text{SDE/STL}}$ pin level is 'L', the first 8-bit data is used as address data. The second 8-bit data is set in a specified internal register. The third data is transferred to the location specified by (the first data + 1). Note that address data can be changed after the $\overline{\text{SDE/STL}}$ pin level changes from L to H, then to L.

(2) Internal control registers

X: Invalid

Serial data	MSB							LSB	
Address data	7	6	5	4	3	2	1	0	
Hexadecimal data									
X 0	SBY	WKVAR	FILD	KOUT	POSVAR	STL	FVPR	FHPR	One-screen mode
X 1	SBY	PRI	KOUT2	KOUT1	STL2	STL1	FVPR	FHPR	Two-screen mode
X 8	VWIPE	HWIPE	Vp5	Vp4	Vp3	Vp2	Vp1	Vp0	
X 9	X	X	Hp5	Hp4	Hp3	Hp2	Hp1	Hp0	
X A	WK2	WK1	Ywk5	Ywk4	Ywk3	Ywk2	Ywk1	Ywk0	
X B	WKVAR2	WKVAR1	Rwk5	Rwk4	Rwk3	Rwk2	Rwk1	Rwk0	
X C	VDFS1	VDFS0	Bwk5	Bwk4	Bwk3	Bwk2	Bwk1	Bwk0	

(3) Register data functions

Note: Screen A - Sub display screens at fixed four corner positions
Screen B - Sub display screen at the position specified by register data.

Fixed frame color - Pre-defined white frame color. See note 1.

Desired frame color - Frame color specified by register data

a. One-screen mode

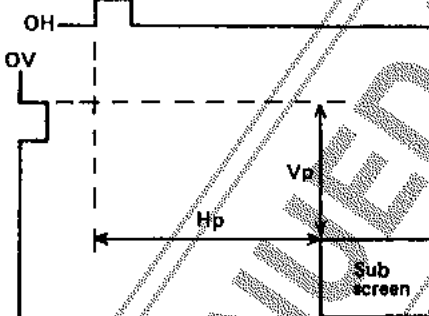
Data bit name	Data bit level		Function
	H	L	
WKVAR	Desired frame color	Fixed frame color	
FILD	Field display	Frame display	
KOUT	ON	OFF	Sub screen display control
POSVAR	Screen B	Screen A	
STL	Still picture	Motion picture	

b. Two-screen mode

Data bit name	Data bit level		Function
	H	L	
PRI	Top screen	Bottom screen	Priority control of two sub screens. See note 2.
KOUT1	ON	OFF	Screen A display control
KOUT2	ON	OFF	Screen B display control
STL1	Still picture	Motion picture	Screen A control
STL2	Still picture	Motion picture	Screen B control
WKVAR1	Desired frame color	Fixed frame color	Screen A control
WKVAR2	Desired frame color	Fixed frame color	Screen B control

c. Register data common to the one- and two-screen modes

Data bit name	Data bit level		Function
	H	L	
WK1	ON	OFF	DAC frame output for screen A
WK2	ON	OFF	DAC frame output for screen B
VWIPE	ON	OFF	Vertical wipe control. See note 3.
HWIPE	ON	OFF	Horizontal wipe control. See note 3.
SBY	ON	OFF	Standby - PLL circuit stop. See note 4.

Data bit name	Function				
Vp5 to 0 Hp5 to 0	<p>Screen B position control</p>  $Vp = [(Vp5 \text{ to } 0) + 1] \times 5H + 3H$ $Hp = [(Hp5 \text{ to } 0) + 6] \times \frac{1}{60f_H}$ <p>*The sub screen position beyond the main screen range is ignored.</p>				
RVPR FHPR	<p>Positioning of fixed four corner sub screens</p> <table border="1"> <tr> <td>(0 , 0) (000101,000110)</td> <td>(0 , 1) (000101,011111)</td> </tr> <tr> <td>(1 , 0) (011111,000110)</td> <td>(1 , 1) (011111,011111)</td> </tr> </table> <p>(FVPR,FHPR) (Vp5 to 0,Hp5 to 0)</p>	(0 , 0) (000101,000110)	(0 , 1) (000101,011111)	(1 , 0) (011111,000110)	(1 , 1) (011111,011111)
(0 , 0) (000101,000110)	(0 , 1) (000101,011111)				
(1 , 0) (011111,000110)	(1 , 1) (011111,011111)				
Ywk5 to 0 Rwk5 to 0 Bwk5 to 0	<p>Y signal R-Y signal B-Y signal</p> <p>DAC frame color data</p>				

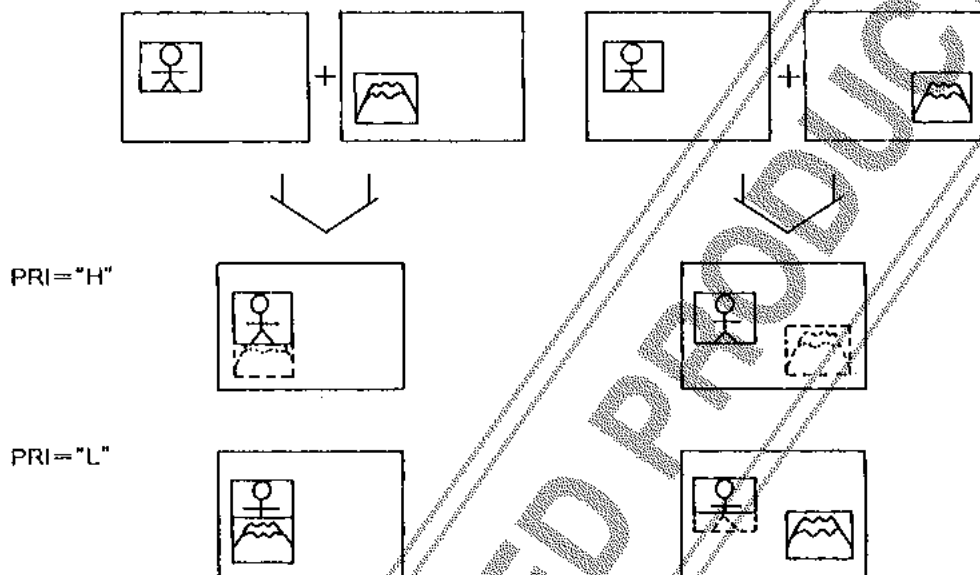
Data bit name		Vertical filter factor			Function
VDFS1	VDFS0	First line	Second line	Third line	
L	L	0.50	0.50	0.00	
L	H	0.25	0.50	0.25	
H	L	0.31	0.38	0.31	
H	H	X	X	X	No use

Note 1:

	MSB	LSB
Ywk5 to 0 =	1	1 0 0 0 0
Rwk5 to 0 =	1	0 0 0 0 0
Bwk5 to 0 =	1	0 0 0 0 0

Note 2:

This data bit controls sub-screen display priority when two sub screens are created on the same display area.



*: The sub screens indicated in dotted lines do not appear on the screen.

*: The example on the right side shows that the two sub screens are not superimposed on each other.

However, this display specification is not allowed. That is, two sub screens cannot be created horizontally.

Note 3:

Wipe function - A sub screen is made to gradually appear or disappear from the display screen. This function applies only to the one-screen display mode.

VWIPE	HWIPE	Operation description	Time
L	L	wipe off	—
H	L	About one second	About one second
L	H	About one second	About one second
H	H	About one second	About one second

*: The above example shows the 4-step wipe operation. However, the actual wipe operation is based on 64 steps.

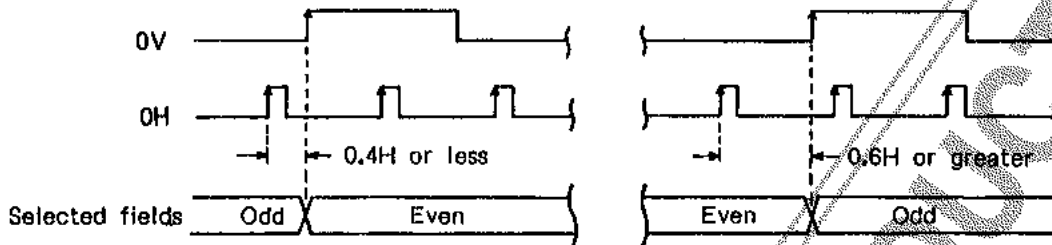
*: The sub screen is made to disappear from the display screen area in the reverse order.

Note 4: If the standby mode is activated, the PLL circuit stops. As a result, the contents of the memory are not kept.

The data transfer to internal registers can be continued because the VCO oscillation clock is not used.

Odd/even field selection circuit

The fields selection is carried out by using the phase difference between the two rising edges of OV and OH if the TV/VCR is 'L'. For this purpose, the two timing signals (OV and OH) should be input as follows.



Note: The above requirements can apply to the KV and KH signals. If the TV/VCR pin is 'H', the falling edges are used for the field selection. Note that the exact horizontal synch. signals should be generated and equalizing pulse signals should be eliminated.

Synch. signals

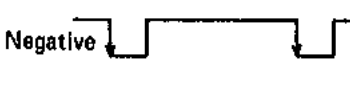
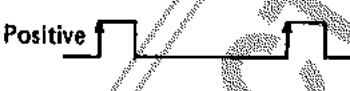
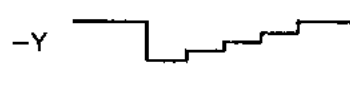

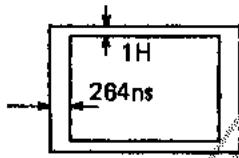
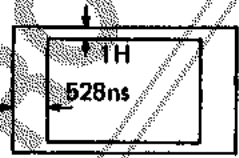
- a. The LC7440 is set on the assumption that the OH and KH pin input signals are delayed one microsecond from the horizontal synch. signal of the video signal as shown below.



- b. Noise input to the synch. signal input pins (KV, KH, OV and OH) will cause screen display distortion. To prevent this, all pins should be wired with much care.
- c. Unstable synch. signal will cause sub screen display distortion. In this case, it is recommended that the display be switched off.

On TV/VCR pin

The following values can be set according to the TV/VCR pin levels.

Value item	TV/VTR	H	L
Synch. signal polarity (V and H)		Negative 	Positive 
YDA output signal polarity (AD Input:Y)		-Y 	Y 
Vertical frame of the WAKU pin			
Timings of KOUT, WAKU and DAC outputs		Simultaneous outputs For details, refer to the section dealing with the sub screen output timings.	KOUT, WAKU: Delayed 528 nano seconds.

On PLLOH pin

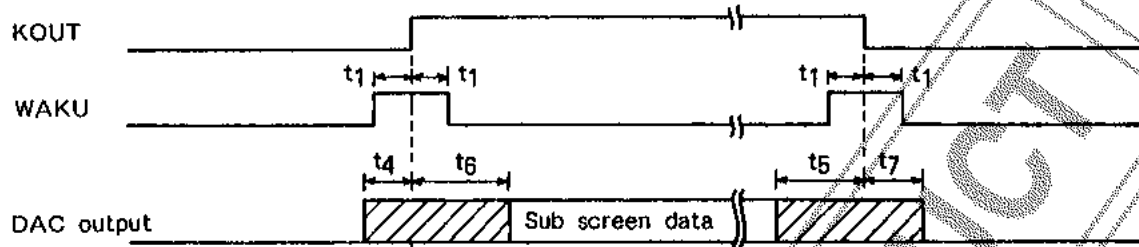
In case of PLLOH = 'H'

Sub screen display positions are controlled by the horizontal synch. signals generated by the PLL circuit. This means that no digital error is generated. As a result, high-quality sub screen display can be obtained.

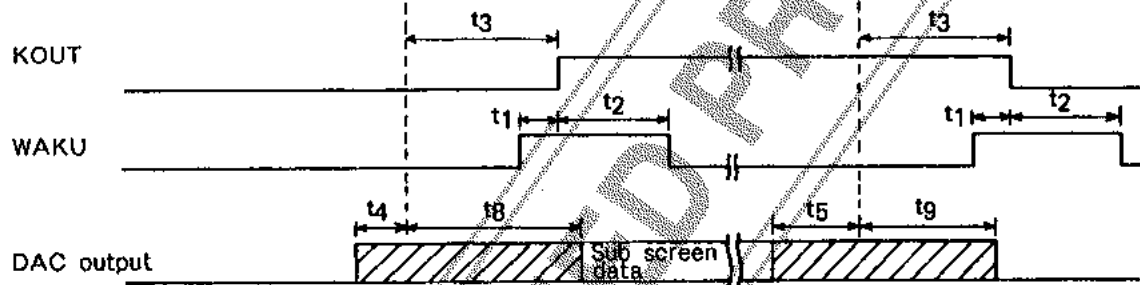
If the main horizontal synch. signal (Input signal to the OH pin) is unstable, the PLL lock operation may be adversely affected. As a result, the sub screen display will flicker. In this case, set the PLLOH pin to 'L'.

Sub screen output timings

(1) TV/VCR = 'H'



(2) TV/VCR = 'L'



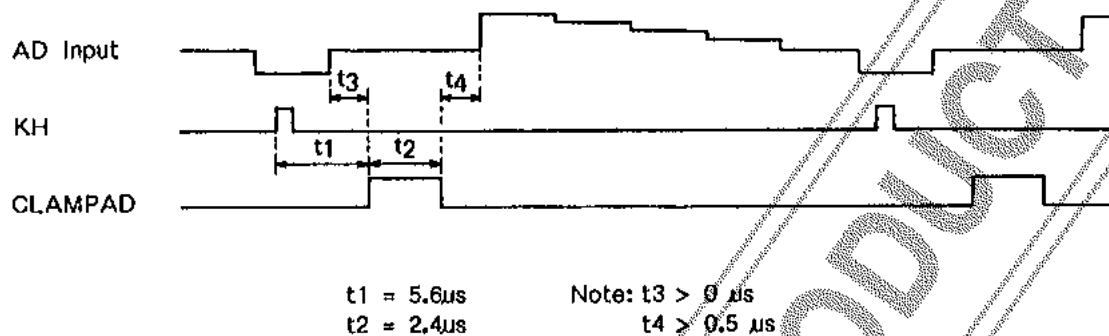
$t_1 = 132\text{ns}$	$t_4 = 176\text{ns}$	$t_7 = 220\text{ns}$
$t_2 = 396\text{ns}$	$t_5 = 308\text{ns}$	$t_8 = 616\text{ns}$
$t_3 = 528\text{ns}$	$t_6 = 352\text{ns}$	$t_9 = 484\text{ns}$

Note: The shaded DAC outputs indicate frame data.

Clamp pulse

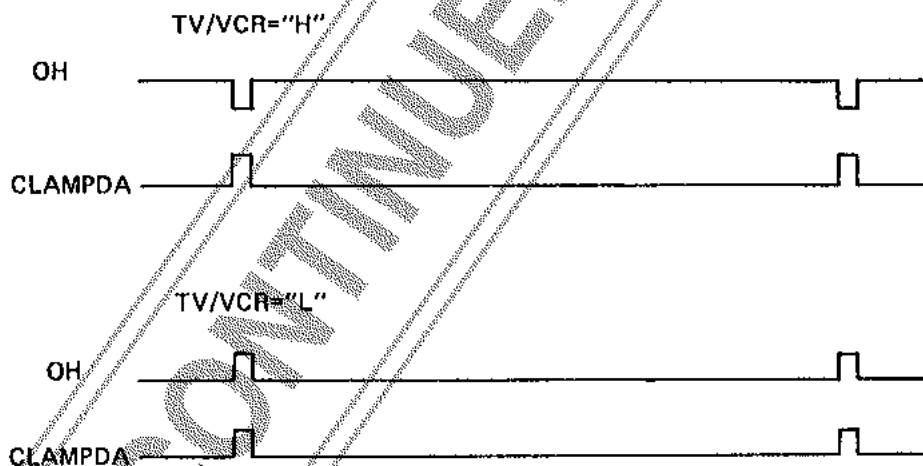
(1) A/D converter clamp

The clamp pulses are output at the timings as shown below. In this case, the pedestal level should be carefully considered.



(2) DA converter clamp

The DA converter clamp pulse (CLAMPDA) is exactly the same as the main horizontal synch. signal (OH). However, its polarity is always positive.



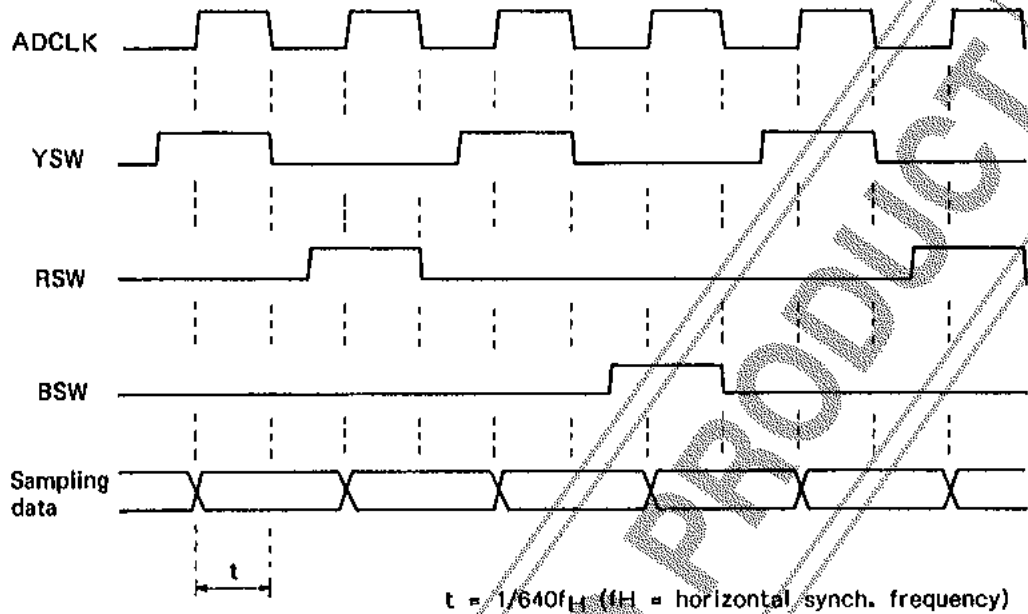
The DA converter output values except for sub screen output data are shown in the table below.

	TV/VTR									
	H					L				
YAOUT	1	1	1	1	1	0	0	0	0	0
	MSB					LSB				
RAOUT	1	0	0	0	0	1	0	0	0	0
BAOUT	1	0	0	0	0	1	0	0	0	0

If TV mode has been selected,
the output Y signal is -Y.
If VCR mode has been selected,
the output Y signal is Y.

Control signal output timings

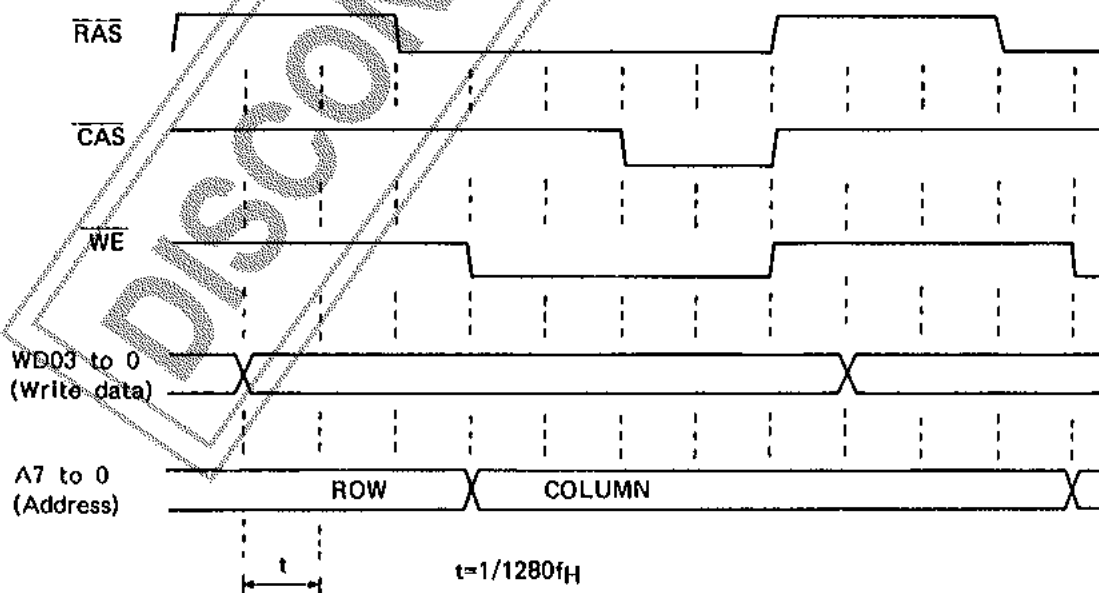
(1) AD converter (LC7480) control signal output timings



Note: The above timings show the high-speed operation. To prevent any operational errors due to noises, pins should be wired with much care. The wires should be as short as possible.

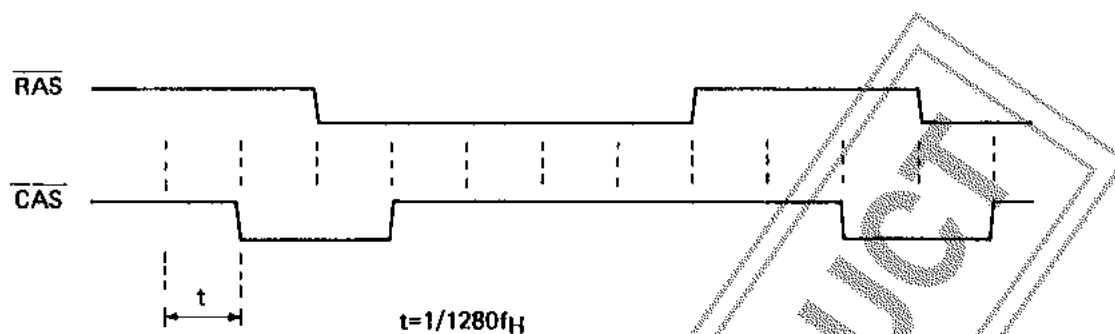
(2) Memory (256K dual port) control signal timings

a. Data write timings

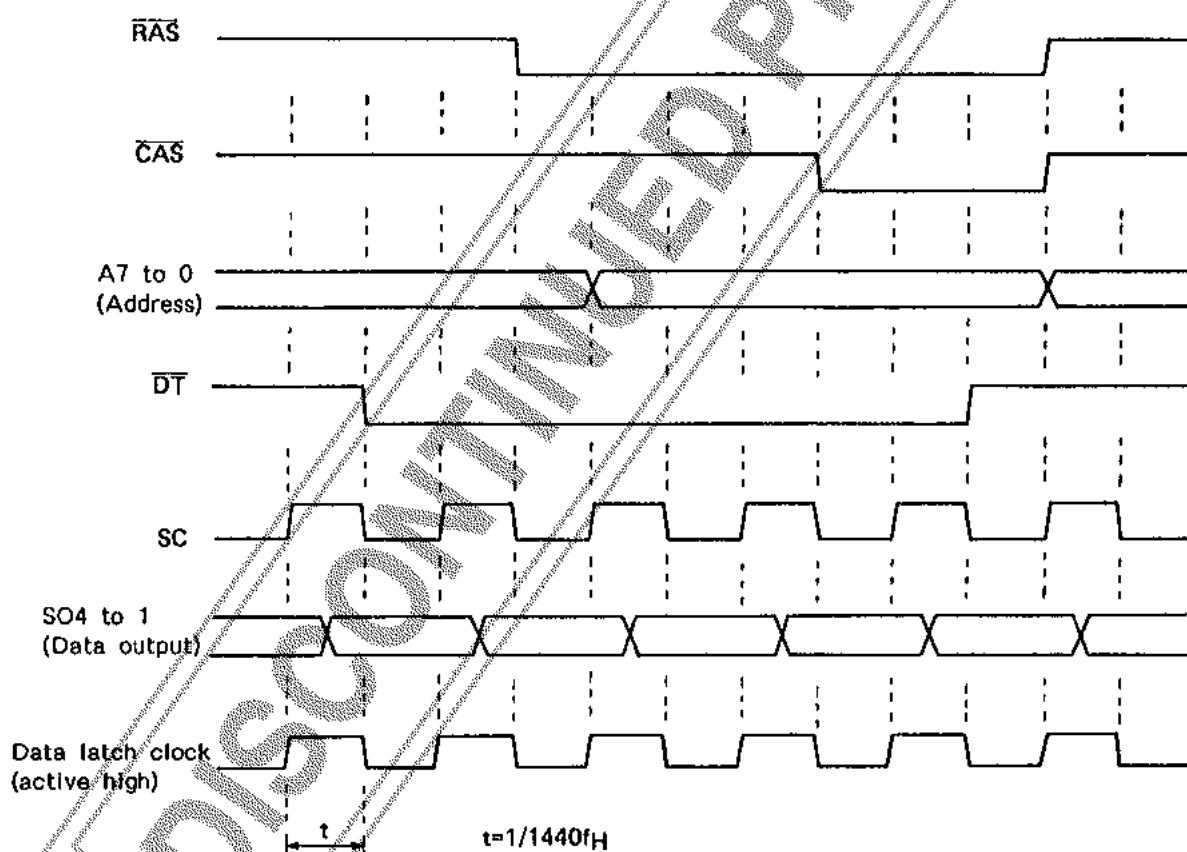


b. Refresh timings

The refresh operations are carried out by using the CAS-before RAS refresh timings as shown below.



c. Data transfer → Serial read



Note: The above timings show the high-speed operation. To prevent any operational errors due to noises, pins should be wired with much care. The wires should be as short as possible.

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass produced.
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