

SANYO

No. 3725

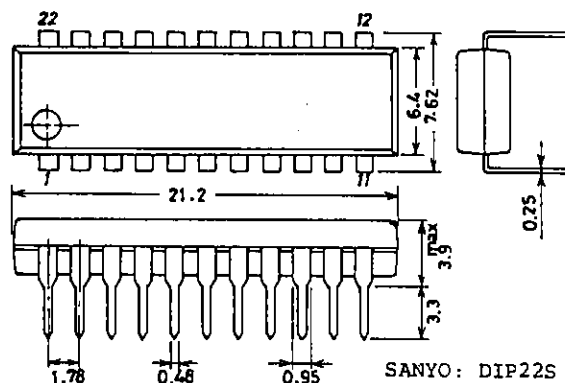
LC7470**Character and Pattern Display Control IC****Overview**

Character and pattern display control IC for TV screen

A character dot configuration is 12 x 18. The IC has 64 internal character ROMs and displays up to 288 characters (24 characters x 12 lines) on a TV screen. It can be controlled by a microcomputer.

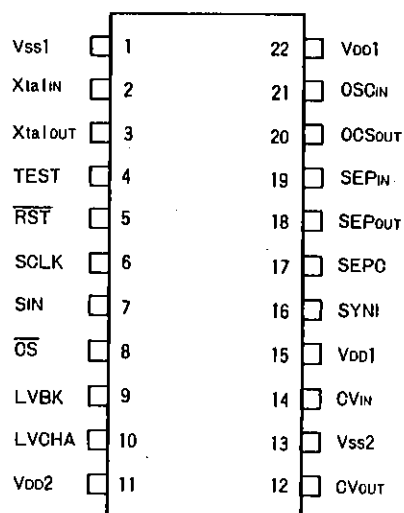
Functions and Applications

- | | |
|--|---|
| (1) Screen Display Mode | 24 characters x 12 lines |
| (2) Number of display characters | 288 characters (MAX.) |
| (3) Display control ROM (line ROM) | 64 lines (line control: 24-character line) |
| (4) Display RAM | 176 characters (used for specifying variable characters) |
| (5) Character configuration | 12 (horizontal) x 18(vertical) dots |
| (6) Number of character types | 64 types |
| (7) Character size | Horizontal direction: 4, Vertical direction: 4 |
| (8) Display start position | Horizontal direction: 64, Vertical direction: 64 |
| (9) Blinking mode | Character blinking |
| (10) Display ON/OFF mode | ON/OFF cycle: 1.0 second and 0.5 second. Duty cycle: 25%, 50% and 75% |
| (11) Blanking mode | Entire font area (12 x 18 dots) |
| (12) Background colors | 4 (at internal SYNC. operation mode) |
| (13) External control input | Serial data input |
| (14) Synchronous signal | Selectable: Internal and External |
| (15) Internal SYNC. separation circuit available | |
| (16) Video output | NTSC-format composite output |
| (17) Superimpose function | Superimposes character output on composite video output |

Package Dimensions DIP-22S
(unit: mm)

LC7470

Pin Assignment



Absolute Maximum Ratings

Characteristics	Symbol	Condition	Ratings		unit
			min	max	
Supply Voltage	VDD	VDD1, VDD2	Vss-0.3	Vss+7.0	V
Input Voltage	VIN	All input pins	Vss-0.3	VDD1+0.3	V
Output Voltage	VOUT		Vss-0.3	VDD1+0.3	V
Maximum Current Dissipation	Pd max	Ta=25°C		300	mW
Operating Temperature	Topg		-30	+70	°C
Storage Temperature	Tstg		-40	+125	°C

Recommended Operating Conditions at Ta=-30 to +70 °C

Characteristics	Symbol	Condition	Ratings			unit
			min	typ	max	
Supply Voltage	VDD1	Pin VDD1	4.5	5.0	5.5	V
	VDD2	Pin VDD2	4.5	5.0	1.27VDD1	V
'H' Level Input Voltage	VIH2	Pins CS, SIN, RST, SCLK	0.8VDD1		VDD1+0.3	V
'L' Level Input Voltage	VIL2	Pins CS, SIN, RST, SCLK	Vss-0.3		0.2VDD1	V
Composite Video Input Voltage	VIN1	CVIN		2VP-P		V
	VIN2	Pin SYN1		2VP-P	2.5VP-P	
Oscillation Frequency	FOSC1	Xtal oscillation pin (at 4fosc)		14.31		MHz
	FOSC2	Xtal oscillation pin (at 2fosc)		7.16		MHz
	FOSC3	LC oscillation pin		7		MHz

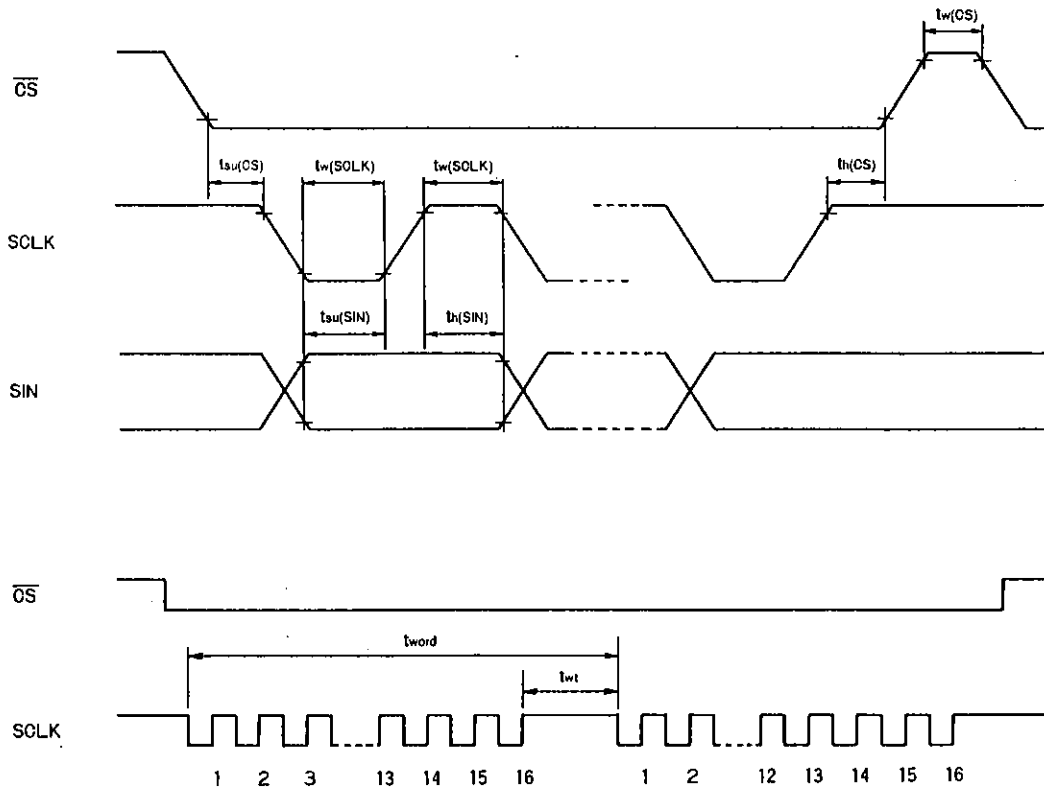
Electrical characteristics (Ta=-30 °C to +70 °C, and VDD = 5V unless other noted)

Characteristics	Symbol	Pin	Condition	Ratings			unit
				min	typ	max	
Output-off Leakage Current	Ileak	CVOUT				10	μA
'H' Level Output Voltage	VIH1	SEPOUT	VDD=4.5V IOH=1.0mA	3.5			V
'L' Level Output Voltage	VIL1	SEPOUT	VDD=4.5V IOL=1.0mA			1.0	V
Input Current	IiH	CS, SIN, RST, SCLK, SEPIN	VIN=VDD			1	μA
	IiL	OSCIN	VIN=Vss	-1			μA
Operating Current Dissipation	IDD					15	mA

Timing Characteristics at Ta=-30 to +70 °C, V_{DD}=5±0.5V

Characteristics	Symbol	Condition	Ratings			unit
			min	typ	max	
Minimum Input Pulse Width	t _w (SCLK)	SCLK	200			ns
	t _w (CS)	$\overline{\text{CS}}$ (CS="H" level period)	1			μs
Data Setup Time	t _{su} (CS)	$\overline{\text{CS}}$	200			ns
	t _{su} (SIN)	SIN	200			ns
Data Hold Time	t _h (CS)	$\overline{\text{CS}}$	2			μs
	t _h (SIN)	SIN	200			ns
1-Word Write Period	t _{word}	16-bit data write period	10			μs
	t _{wt}	RAM data write period	1			μs

Serial Data Input Timings

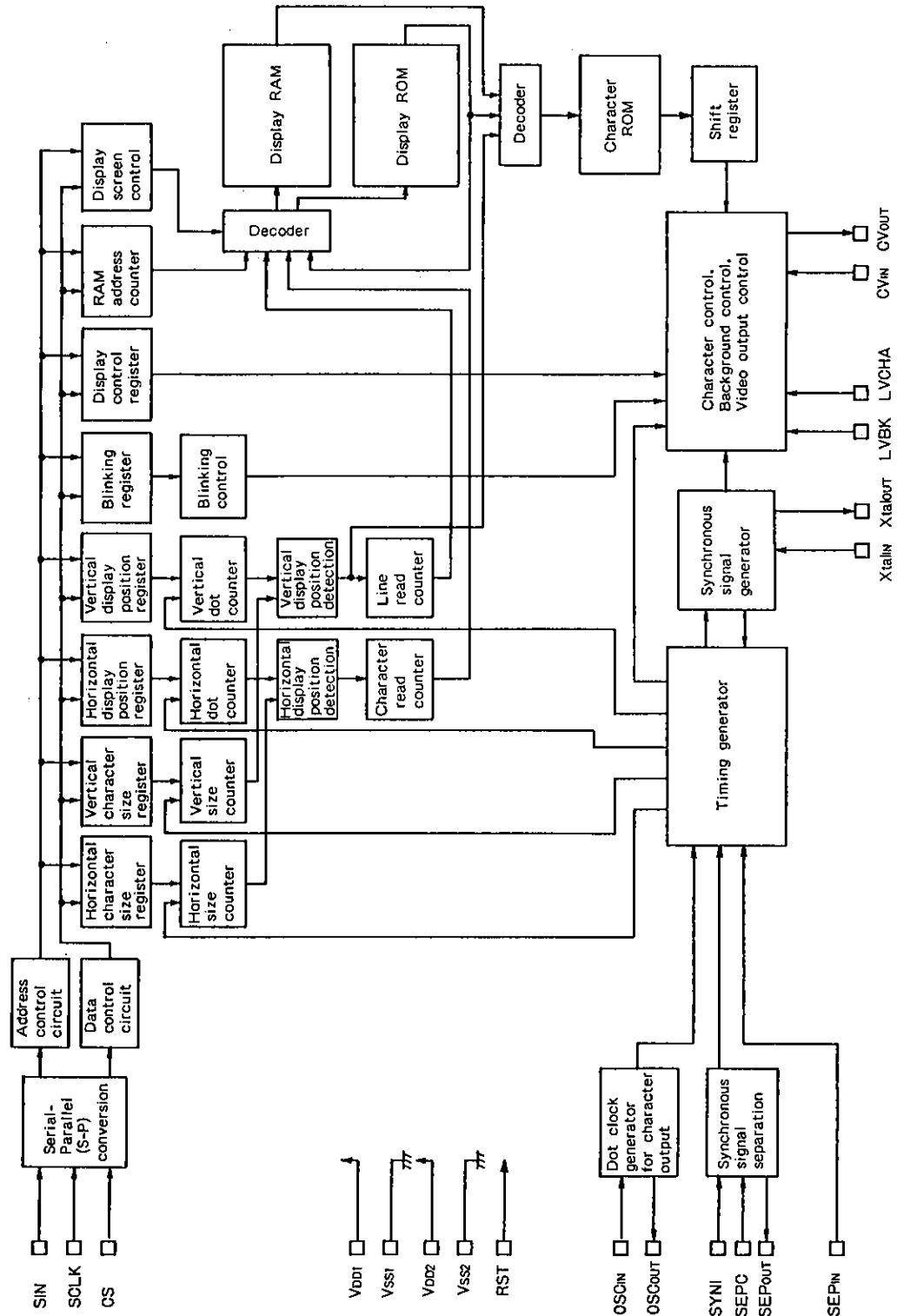


Pin Description

Pin No.	Pin Symbol	Pin Name	Functions
1	VSS1	Ground pin	GND pin (digital grounding)
2	XtalIN	Xtal oscillation pin	Oscillation pins for connecting a crystal oscillator and capacitor to generate internal synchronous signals.
3	XtalOUT		
4	TEST	Test pin	Test output pin
5	RST	Reset input pin	System reset input pin
6	SCLK	Clock input pin	Clock input pin for serial data input
7	SIN	Data input pin	Serial data input pin. Serial 16-bit data input is supported.
8	CS	Enable input pin	Enable input pin for serial data input. If this pin becomes active (active low), the serial data input is enabled.
9	LVBK	Input pin for blank level adjustment	Level input pin for adjusting blank levels.
10	LVCHA	Input pin for character level adjustment	Level input pin for adjusting character levels.
11	VDD2	Power supply pin	Power supply pin for adjusting composite video signal levels (analog power supply)
12	CVOUT	Video signal output pin	Output pin for composite video signal
13	VSS2	Ground pin	GND pin (analog grounding)
14	CVIN	Video signal input pin	Input pin for composite video signal
15	VDD1	Supply voltage pin	Supply voltage pin (+5V)
16	SYNI	Synchronous signal separation circuit input pin	Input pin for synchronous signal separation circuit
17	SEPC	Synchronous signal separation circuit adjustment pin	Adjustment pin for synchronous signal separation circuit (A capacitor is connected to this pin.)
18	SEPOUT	Composite synchronous signal output pin	Composite synchronous signal output pin for synchronous signal separation circuit
19	SEPIN	Vertical synchronous signal input pin	Vertical synchronous signal input pin. The input signal to this pin is generated by integrating the output signal from the SEPOUT pin. Add an integral circuit between the SEPOUT pin and the SEPIN pin.
20	OScout	LC oscillation pin	Oscillation pins for connecting a coil and capacitor to generate character output dot clocks.
21	OSCIN		
22	VDD1	Supply voltage pin (+5V)	Supply voltage (+5V)

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System Block Diagram



Display Screen

The maximum display screen consists of horizontal 24 characters and vertical 12 lines.

The number of display characters is 288 (MAX.). The display characters can consist of display line ROM (12 lines) data and display RAM (176 characters).

- Fixed characters can be specified by making an access to the display line ROM.
- Variable characters can be generated by programming the display RAM.

24 characters																							
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

Memory Configuration (display RAM and control RAM)

Memory address and data signals consist of 16 bits.

Address range from 0D (000h) to 175D (0AFh) used as the display RAM.

Address range from 176D (0B0h) to 191D (0BFh) is used as the display control register data area.

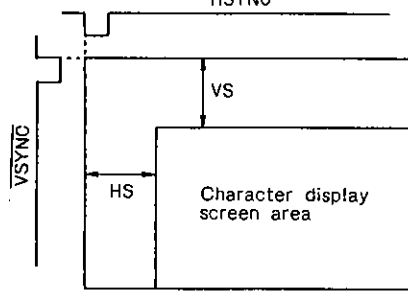
Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	Display RAM area
	<div><div>Blink- ing</div><div>Character code</div></div>																
175 (0AFh)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the first line
177 (0B1h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the second line
178 (0B2h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the third line
179 (0B3h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fourth line
180 (0B4h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fifth line
181 (0B5h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the sixth line
182 (0B6h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the seventh line
183 (0B7h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eighth line
184 (0B8h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the ninth line
185 (0B9h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the tenth line
186 (0BAh)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eleventh line
187 (0BBh)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position. Horizontal character size.
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position. Vertical character size.
190 (0BEh)	0	0	0	0	INT NON	—	—	OSC STP	DSP ON	—	SYS RST	—	—	—	PHASE 1	PHASE 0	Video signal and etc.
191 (0BFh)	0	0	0	0	TST MOD	—	—	BLK 1	BLK 0	—	BLINK 2	BLINK 1	BLINK 0	EX	—	BCOL	Control register

(1) Address 188D (0BCH)

DA 0~C	Register Name	Contents		Remarks									
		Status	Function										
0	HP0 (LSB)	0	If a horizontal display start position is defined as the HS, the HS can be calculated as follows: $HS=Tc \times (4 \sum_{n=0}^5 2^n HP_n)$ Tc: Oscillation cycle of the OSCIN-OSCOUT oscillation circuit during operation.	The horizontal display start position is speci- fied by using six bits HP5 to HP0. The LSB (HP0) has a bit weight of 4Tc.									
		1											
1	HP1	0											
		1											
2	HP2	0											
		1											
3	HP3	0											
		1											
4	HP4	0											
		1											
5	HP5 (MSB)	0											
		1											
6	HSZ10	0	<table><tr><td>HSZ11 \ HSZ10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	HSZ11 \ HSZ10	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Horizontal character size for the first line
HSZ11 \ HSZ10	0	1											
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
		1											
7	HSZ11	0	<table><tr><td>HSZ21 \ HSZ20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	HSZ21 \ HSZ20	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Horizontal character size for the second line
HSZ21 \ HSZ20	0	1											
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
		1											
8	HSZ20	0	<table><tr><td>HSZ31 \ HSZ30</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	HSZ31 \ HSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Horizontal character size for lines third to twelfth
HSZ31 \ HSZ30	0	1											
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
		1											
9	HSZ21	0	<table><tr><td>HSZ31 \ HSZ30</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	HSZ31 \ HSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	
HSZ31 \ HSZ30	0	1											
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
		1											
A	HSZ30	0	<table><tr><td>HSZ31 \ HSZ30</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	HSZ31 \ HSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	
HSZ31 \ HSZ30	0	1											
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
		1											
B	HSZ31	0	<table><tr><td>HSZ31 \ HSZ30</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	HSZ31 \ HSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	
HSZ31 \ HSZ30	0	1											
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
		1											
C	—	0											
		1											

*: If the \overline{RST} pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

(2) Address 189D (0BDH)

DA 0~C	Register Name	Contents		Remarks									
		Status	Function										
0	VP0 (LSB)	0	<p>If a vertical display start position is defined as the VS, the VS can be calculated as follows: $VS=H\times(4\sum_{n=0}^52^nVP_n)$ H: Horizontal synchronization pulse cycle</p> 	The vertical display start position is specified by using six bits VP5 to VP0. The LSB (VP0) has a bit weight of 4H.									
		1											
1	VP1	0											
		1											
2	VP2	0											
		1											
3	VP3	0											
		1											
4	VP4	0											
		1											
5	VP5 (MSB)	0											
		1											
6	VSZ10	0	<table><tr><td>VSZ11 \ VSZ10</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	VSZ11 \ VSZ10	0	0	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Vertical character size for the first line
		VSZ11 \ VSZ10	0	0									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
7	VSZ11	0											
		1											
8	VSZ20	0	<table><tr><td>VSZ21 \ VSZ20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	VSZ21 \ VSZ20	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Vertical character size for the second line
		VSZ21 \ VSZ20	0	1									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
9	VSZ21	0											
		1											
A	VSZ30	0	<table><tr><td>VSZ31 \ VSZ30</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/1 dot</td><td>2Tc/1 dot</td></tr><tr><td>1</td><td>3Tc/1 dot</td><td>4Tc/1 dot</td></tr></table>	VSZ31 \ VSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Vertical character size for lines third to twelfth
		VSZ31 \ VSZ30	0	1									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
B	VSZ31	0											
		1											
C	—	0											
		1											

*: If the $\overline{\text{RST}}$ pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

(3) Address 190D (0BEH)

DA 0~C	Register Name	Contents				Remarks
		Status	Function			
0	PHASE0	0	PHASE1	PHASE0	Background color	Background color
		1	0	0	$\pi/2$	
1	PHASE1	0	0	1	π	
		1	1	0	$3\pi/2$	
		0	1	1	In-phase	
		1	1	1		
2	—	0				
		1				
3	—	0				
		1				
4	—	0				
		1				
5	SYSRST	0				With CS pin level = 'L', the LSI is reset. If the pin level changes to 'H', the LSI reset will be released.
		1	All the registers are reset and the display mode is inactivated.			
6	—	0				
		1				
7	DSPON	0	Character OFF			
		1	Character ON			
8	OSCSTP	0	The oscillation circuit does not enter a stop state if the display mode is inactivated.			To stop the crystal oscillation circuit and LC oscillation circuit.
		1	The oscillation circuit enters the stop state if the display mode is inactivated.			
9	—	0				
		1				
A	—	0				
		1				
B	INT/ NON	0	Interlace (262.5H/1 field)			Display operation mode selection: interlace and non-interlace
		1	Non-interlace (263H/1 field)			
C	—	0				
		1				

*: If the $\overline{\text{RST}}$ pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

(4) Address 191D (0BFH)

DA 0~C	Register Name	Contents			Remarks												
		Status	Function														
0	BCOL	0	Active background coloring (available only in internal synchronization mode)														
		1	Inactive background coloring (background level adjustable only)														
1	—	0															
		1															
2	EX	0	External synchronization		HSYNC and VSYNC signals selection: internal and external.												
		1	Internal synchronization														
3	BLINK0	0	<table><tr><td colspan="2">BLINK0 \ BLINK1</td><td>0</td><td>1</td></tr><tr><td>0</td><td></td><td>Blinking OFF mode</td><td>Duty: 25%</td></tr><tr><td>1</td><td></td><td>Duty: 50%</td><td>Duty: 75%</td></tr></table>			BLINK0 \ BLINK1		0	1	0		Blinking OFF mode	Duty: 25%	1		Duty: 50%	Duty: 75%
BLINK0 \ BLINK1		0				1											
0		Blinking OFF mode	Duty: 25%														
1		Duty: 50%	Duty: 75%														
		1															
4	BLINK1	0															
		1															
5	BLINK2	0	Blinking cycle: 1 second		Blinking cycle control												
		1	Blinking cycle: 0.5 seconds														
6	—	0															
		1															
7	BLK0	0	<table><tr><td colspan="2">BLK0 \ BLK1</td><td>0</td><td>1</td></tr><tr><td>0</td><td></td><td>Blanking OFF mode</td><td>Character size</td></tr><tr><td>1</td><td></td><td>Partial screen size</td><td>Entire screen size</td></tr></table>			BLK0 \ BLK1		0	1	0		Blanking OFF mode	Character size	1		Partial screen size	Entire screen size
BLK0 \ BLK1		0				1											
0		Blanking OFF mode	Character size														
1		Partial screen size	Entire screen size														
		1															
8	BLK1	0															
		1															
9	—	0															
		1															
A	—	0															
		1															
B	TSTMOD	0	Normal operation		Should be fixed to "0".												
		1	Test mode														
C	—	0															
		1															

*: If the $\overline{\text{RST}}$ pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

Memory Configuration (display line ROM)

The display line ROM address range is from 0D (000H) to 1535D (5FFH).

Data consists of 7 bits.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
0000 (000h)	0	0	0	0	0	0	0	0	ROM RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the first line
0023 (017h)	0	0	0	0	0	0	0	0	ROM RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty- fourth character of the first line
0024 (018h)	0	0	0	0	0	0	0	0	ROM RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the second line
									ROM RAM								Character code
1535 (5FFh)	0	0	0	0	0	0	0	0	ROM RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty- fourth character of the sixty- fourth line

DA 0~8	Register Name	Contents		Remarks		
		Status	Function			
0	ADR0	0	Used to specify the desired character ROM address.			
		1	To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'. To access the character ROM, addresses 0D (000) to 63D (3FH) can be used. Set bit 6 (ADR6) to '0'.			
1	ADR1	0				
		1				
2	ADR2	0				
		1				
3	ADR3	0				
		1				
4	ADR4	0				
		1				
5	ADR5	0				
		1				
6	ADR6	0				
		1				
7	ROM/ RAM	0			Direct read access to the character ROM	
		1			Read access to the character ROM through the display RAM.	

Display Line ROM: Line Address Table



Line No.	Address No.	Line No.	Address No.
1st line	00HEX (0000)	33rd line	300HEX (0768)
2nd line	18HEX (0024)	34th line	318HEX (0792)
3rd line	30HEX (0048)	35th line	330HEX (0816)
4th line	48HEX (0072)	36th line	348HEX (0840)
5th line	60HEX (0096)	37th line	360HEX (0864)
6th line	78HEX (0120)	38th line	378HEX (0888)
7th line	90HEX (0144)	39th line	390HEX (0912)
8th line	A8HEX (0168)	40th line	3A8HEX (0936)
9th line	C0HEX (0192)	41st line	3C0HEX (0960)
10th line	D8HEX (0216)	42nd line	3D8HEX (0984)
11th line	F0HEX (0240)	43rd line	3F0HEX (1008)
12th line	108HEX (0264)	44th line	408HEX (1032)
13th line	120HEX (0288)	45th line	420HEX (1056)
14th line	138HEX (0312)	46th line	438HEX (1080)
15th line	150HEX (0336)	47th line	450HEX (1104)
16th line	168HEX (0360)	48th line	468HEX (1128)
17th line	180HEX (0384)	49th line	480HEX (1152)
18th line	198HEX (0408)	50th line	498HEX (1176)
19th line	1B0HEX (0432)	51st line	4B0HEX (1200)
20th line	1C8HEX (0456)	52nd line	4C8HEX (1224)
21st line	1E0HEX (0480)	53rd line	4E0HEX (1248)
22nd line	1F8HEX (0504)	54th line	4F8HEX (1272)
23rd line	210HEX (0528)	55th line	510HEX (1296)
24th line	228HEX (0552)	56th line	528HEX (1320)
25th line	240HEX (0576)	57th line	540HEX (1344)
26th line	258HEX (0600)	58th line	558HEX (1368)
27th line	270HEX (0624)	59th line	570HEX (1392)
28th line	288HEX (0648)	60th line	588HEX (1416)
29th line	2A0HEX (0672)	61st line	5A0HEX (1440)
30th line	2B8HEX (0696)	62nd line	5B8HEX (1464)
31st line	2D0HEX (0720)	63rd line	5D0HEX (1488)
32nd line	2E8HEX (0744)	64th line	5E8HEX (1512)

Sample Display Screen

Twelve display lines of the display 64-line ROM are specified.

Variable characters are prepared in the display control RAM.

The display RAM address area is automatically allocated to addresses from 0D (000H) to 175D (AFH) in the display order.

-  The display characters indicated by bold lines are specified through the display RAM access.
-  The display characters indicated by slender lines are specified directly through the display ROM access.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	ROM 000h	ROM 001h	ROM 002h	ROM 003h	ROM 004h	ROM 005h	ROM 006h	ROM 007h	ROM 008h	ROM 009h	ROM 00Ah	ROM 00Bh	ROM 00Ch	ROM 00Dh	ROM 00Eh	ROM 00Fh	ROM 010h	ROM 011h	ROM 012h	ROM 013h	ROM 014h	ROM 015h	ROM 016h	ROM 017h
2	ROM 018h	ROM 019h	ROM 01Ah	ROM 01Bh	ROM 01Ch	ROM 01Dh	ROM 01Eh	ROM 01Fh	ROM 020h	ROM 021h	ROM 022h	ROM 023h	ROM 024h	ROM 025h	ROM 026h	ROM 027h	ROM 028h	ROM 029h	ROM 02Ah	ROM 02Bh	ROM 02Ch	ROM 02Dh	ROM 02Eh	ROM 02Fh
3	ROM 030h	ROM 031h	ROM 032h	ROM 033h	ROM 034h	ROM 035h	ROM 036h	ROM 037h	ROM 038h	ROM 039h	ROM 03Ah	ROM 03Bh	ROM 03Ch	ROM 03Dh	ROM 03Eh	ROM 03Fh	ROM 040h	ROM 041h	ROM 042h	ROM 043h	ROM 044h	ROM 045h	ROM 046h	ROM 047h
4	ROM 048h	ROM 049h	ROM 04Ah	ROM 04Bh	ROM 04Ch	ROM 04Dh	ROM 04Eh	ROM 04Fh	ROM 050h	ROM 051h	ROM 052h	ROM 053h	ROM 054h	ROM 055h	ROM 056h	ROM 057h	ROM 058h	ROM 059h	ROM 05Ah	ROM 05Bh	ROM 05Ch	ROM 05Dh	ROM 05Eh	ROM 05Fh
5	ROM 060h	ROM 061h	ROM 062h	ROM 063h	ROM 064h	ROM 065h	ROM 066h	ROM 067h	ROM 068h	ROM 069h	ROM 06Ah	ROM 06Bh	ROM 06Ch	ROM 06Dh	ROM 06Eh	ROM 06Fh	ROM 070h	ROM 071h	ROM 072h	ROM 073h	ROM 074h	ROM 075h	ROM 076h	ROM 077h
6	ROM 078h	ROM 079h	ROM 07Ah	ROM 07Bh	ROM 07Ch	ROM 07Dh	ROM 07Eh	ROM 07Fh	ROM 080h	ROM 081h	ROM 082h	ROM 083h	ROM 084h	ROM 085h	ROM 086h	ROM 087h	ROM 088h	ROM 089h	ROM 08Ah	ROM 08Bh	ROM 08Ch	ROM 08Dh	ROM 08Eh	ROM 08Fh
7	ROM 090h	ROM 091h	ROM 092h	ROM 093h	ROM 094h	ROM 095h	ROM 096h	ROM 097h	ROM 098h	ROM 099h	ROM 09Ah	ROM 09Bh	ROM 09Ch	ROM 09Dh	ROM 09Eh	ROM 09Fh	ROM 0A0h	ROM 0A1h	ROM 0A2h	ROM 0A3h	ROM 0A4h	ROM 0A5h	ROM 0A6h	ROM 0A7h
8	ROM 0A8h	ROM 0A9h	ROM 0AAh	ROM 0ABh	ROM 0ACh	ROM 0ADh	ROM 0AEh	ROM 0AFh	ROM 0B0h	ROM 0B1h	ROM 0B2h	ROM 0B3h	ROM 0B4h	ROM 0B5h	ROM 0B6h	ROM 0B7h	ROM 0B8h	ROM 0B9h	ROM 0BAh	ROM 0BCh	ROM 0BDh	ROM 0BEh	ROM 0BFh	ROM 0C0h
9	ROM 0C1h	ROM 0C2h	ROM 0C3h	ROM 0C4h	ROM 0C5h	ROM 0C6h	ROM 0C7h	ROM 0C8h	ROM 0C9h	ROM 0CAh	ROM 0CBh	ROM 0CCh	ROM 0CDh	ROM 0CEh	ROM 0CFh	ROM 0D0h	ROM 0D1h	ROM 0D2h	ROM 0D3h	ROM 0D4h	ROM 0D5h	ROM 0D6h	ROM 0D7h	ROM 0D8h
10	ROM 0D9h	ROM 0DAh	ROM 0DBh	ROM 0DCh	ROM 0DDh	ROM 0DEh	ROM 0DFh	ROM 0E0h	ROM 0E1h	ROM 0E2h	ROM 0E3h	ROM 0E4h	ROM 0E5h	ROM 0E6h	ROM 0E7h	ROM 0E8h	ROM 0E9h	ROM 0EAh	ROM 0EBh	ROM 0EC	ROM 0ED	ROM 0EE	ROM 0EF	ROM 0F0h
11	ROM 0F1h	ROM 0F2h	ROM 0F3h	ROM 0F4h	ROM 0F5h	ROM 0F6h	ROM 0F7h	ROM 0F8h	ROM 0F9h	ROM 0FAh	ROM 0FBh	ROM 0FCh	ROM 0FDh	ROM 0FEh	ROM 0FFh	ROM 100h	ROM 101h	ROM 102h	ROM 103h	ROM 104h	ROM 105h	ROM 106h	ROM 107h	ROM 108h
12	ROM 109h	ROM 10Ah	ROM 10Bh	ROM 10Ch	ROM 10Dh	ROM 10Eh	ROM 10Fh	ROM 110h	ROM 111h	ROM 112h	ROM 113h	ROM 114h	ROM 115h	ROM 116h	ROM 117h	ROM 118h	ROM 119h	ROM 11Ah	ROM 11Bh	ROM 11Ch	ROM 11Dh	ROM 11Eh	ROM 11Fh	ROM 120h

Input Timings of External Control Data

Address and data information is input serially to this chip from an external device.

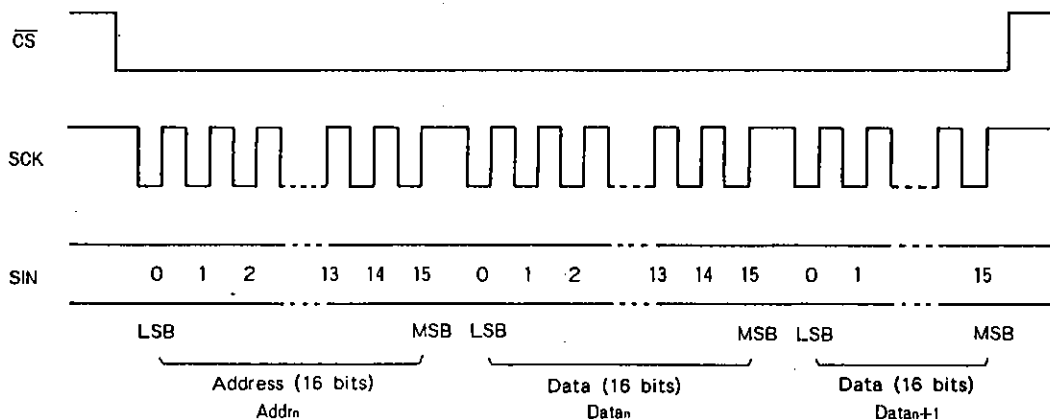
- (1) Address data consists of 16 bits.

The 8 low-order bits have significance. Always set 8 high-order bits to '0'.

- (2) Data consists of 16 bits.

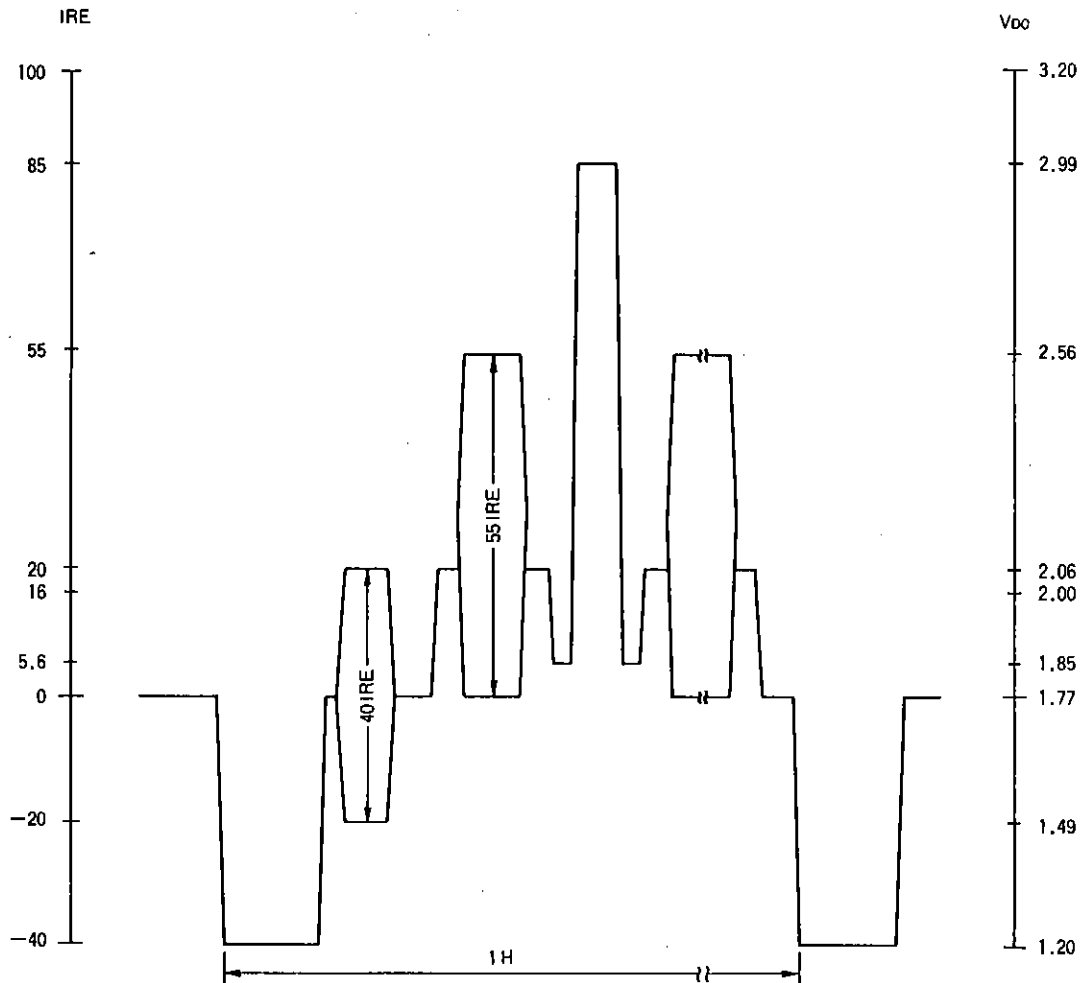
- Only 8 low-order bits of input data to addresses from 000H to 0AFH have significance. Always set 8 high-order bits to '0'.
- Only 11 low-order bits of input data to addresses from 0B0H to 0BBH have significance. Always set 5 high-order bits to '0'.
- Only 12 low-order bits of input data to addresses from 0BCH to 0BFH have significance. Always set 4 high-order bits to '0'.

- (3) The data input format is shown below. The first 16 bits after the \overline{CS} pin (active low) becomes active are processes as an address data. The subsequent groups of 16 bits are handled as the data.



LC7470

Composite Video Signal Output Level (internal generation)



Output level (IRE)	Output voltage (VDC)
100	3.200
85	2.986
46.1	2.430
20	2.057
5.8	1.854
0	1.771
-20	1.486
-40	1.200

V_{DD}=5.000VDC