

SANYO

No. 4991A

LC74784, 74784M**On-Screen Display Controller LSI
for VCR Products**

Overview

The LC74784 and LC74784M are on-screen display CMOS LSIs that display characters and patterns on a TV screen under microprocessor control. The LC74784 and LC74784M display up to 12 lines of 24 characters, each in a 12 × 18 dot matrix.

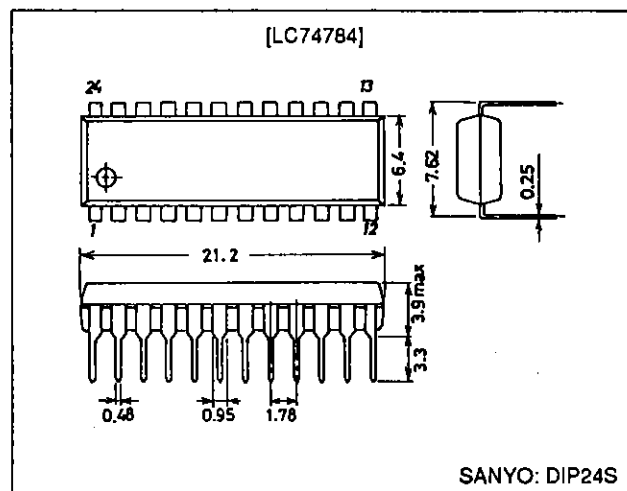
Features

- Display structure: 12 lines × 24 characters (up to 288 characters)
- Character structure: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three size settings each in the vertical and horizontal directions
- Character set: 256 characters
- Display start position: 64 position settings each in the vertical and horizontal directions
- Blinking: In individual character units
- Blinking types: Two types with periods of about 0.5 and 1.0 second
- Blanking: Whole font area blanking (12 × 18 dots)
- Background colors: 8 colors (in internal synchronization mode): 4fSC (NTSC/PAL/PAL-M/PAL-N)
Background colors: 4 colors (in internal synchronization mode): 2fSC (NTSC)
Background colors: 1 color (blue) (in internal synchronization mode): 2fSC (PAL/PAL-M/PAL-N)
- External control input: 8-bit serial input format
- Built-in sync separator circuit
- Character blanked data output
- Video output: Compound NTSC, PAL, PAL-N and PAL-M output

Package Dimensions

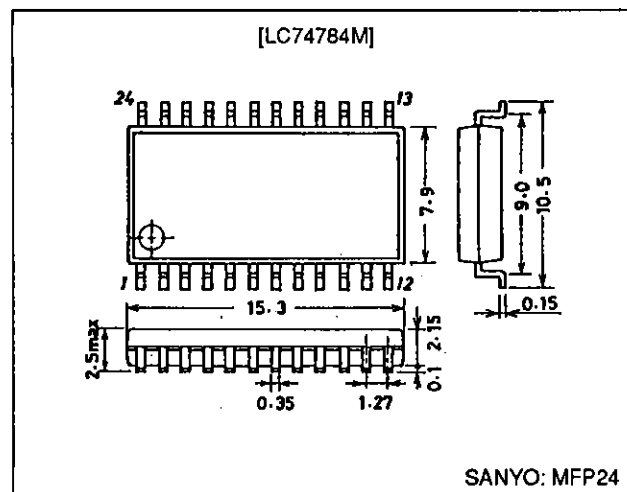
unit: mm

3067-DIP24S



unit: mm

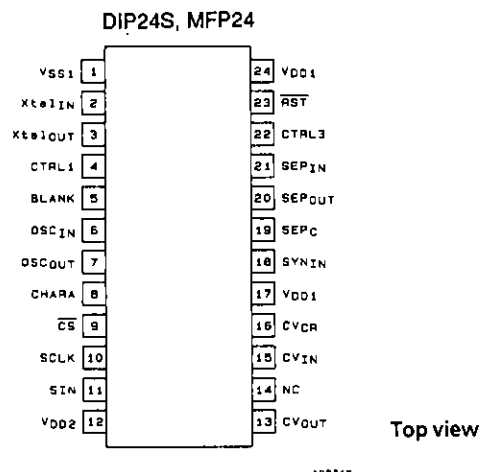
3045B-MFP24



Pin Functions

Pin No.	Symbol	Function	Description
1	V _{SS1}	Ground	Ground connection (digital system ground)
2	Xtal _{IN}	Crystal oscillator connection	Used to connect the crystal oscillator and capacitor used to generate the internal synchronization signal, or to input an external clock (2fsc or 4fsc).
3	Xtal _{OUT}		
4	CTRL1	Crystal oscillator input switching	Switches between external clock input mode and crystal oscillator mode. Low = crystal oscillator mode, high = external clock mode
5	BLANK	Blanking output	Outputs the blank signal (the OR of the character and border signals). (Outputs a composite sync signal when MOD0 is high.) Outputs the crystal oscillator clock during reset (when the RST pin is low), but can be set up to not output this signal by microprocessor command.
6	OSC _{IN}	LC oscillator connection	Connections for the coil and capacitor that form the oscillator that generates the character output dot clock.
7	OSC _{OUT}		
8	CHARA	Character output	Outputs the character signal. (Functions as the external synchronization signal discrimination signal output pin when MOD0 is high, and outputs the state of the judgment as to whether the external synchronization signal is present or not. Outputs a high level when the synchronization signal is present.) Outputs the dot clock (LC oscillator) during reset, but can be set up to not output this signal by microprocessor command.
9	$\overline{\text{CS}}$	Enable input	Serial data input enable input. Serial data input is enabled when low. A pull-up resistor is built in (hysteresis input).
10	SCLK	Clock input	Serial data input clock input. A pull-up resistor is built in (hysteresis input).
11	SIN	Data input	Serial data input. A pull-up resistor is built in (hysteresis input).
12	V _{DD2}	Power supply	Composite video signal level adjustment power supply pin (analog system power supply).
13	CV _{OUT}	Video signal output	Composite video signal output
14	NC		Must be either connected to ground or left open.
15	CV _{IN}	Video signal input	Composite video signal input
16	CV _{CR}	Video signal input	SECAM chrominance signal input
17	V _{DD1}	Power supply	Power supply (+5 V: digital system power supply)
18	SYN _{IN}	Sync separator circuit input	Video signal input for the built-in sync separator circuit (Used for either horizontal synchronization signal or composite sync signal input when the built-in sync separator circuit is not used.)
19	SEP _C	Sync separator circuit bias voltage	Built-in sync separator circuit bias voltage monitor pin
20	SEP _{OUT}	Composite sync signal output	Built-in sync separator circuit composite sync signal output. (When MOD1 is high, outputs a high level during internal synchronization and a low level during external synchronization.) (Outputs the SYN _{IN} input signal when the internal sync separator circuit is not used.)
21	SEP _{IN}	Vertical synchronization signal input	Inputs a vertical synchronization signal created by integrating the SEP _{OUT} pin output signal. An integrator must be attached at the SEP _{OUT} pin. This pin must be tied to V _{DD1} if unused.
22	CTRL3	SEP _{IN} input control	Controls whether or not the VSYNC signal is input to the SEP _{IN} input. Low = VSYNC input, high = VSYNC not input.
23	$\overline{\text{RST}}$	Reset input	System reset input. A pull-up resistor is built in (hysteresis input).
24	V _{DD1}	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Pin Assignment



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD1} and V_{DD2} pins	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Maximum input voltage	$V_{IN\text{ max}}$	All pins	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Maximum output voltage	$V_{OUT\text{ max}}$	BLANK, CHARA and SEP_{OUT} pins	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a = 25^\circ\text{C}$	350	mW
Operating temperature	T_{opr}		-30 to $+70$	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to $+125$	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -30$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD1}	V_{DD1} pin	4.5	5.0	5.5	V
	V_{DD2}	V_{DD2} pin	4.5	5.0	$1.27 V_{DD1}$	V
Input high level voltage	V_{IH1}	\overline{RST} , \overline{CS} , SIN and SCLK pins	$0.8 V_{DD1}$		$V_{DD1} + 0.3$	V
	V_{IH2}	CTRL1, CTRL3 and SEP_{IN} pins	$0.7 V_{DD1}$		$V_{DD1} + 0.3$	V
Input low level voltage	V_{IL1}	\overline{RST} , \overline{CS} , SIN and SCLK pins	$V_{SS} - 0.3$		$0.2 V_{DD1}$	V
	V_{IL2}	CTRL1, CTRL3 and SEP_{IN} pins	$V_{SS} - 0.3$		$0.3 V_{DD1}$	V
Pull-up resistance	R_{PU}	\overline{RST} , \overline{CS} , SIN and SCLK pins, applies to pins set by options.	25	50	90	k Ω
Composite video input voltage	V_{IN1}	CVIN pin: $V_{DD1} = 5\text{ V}$		2.0		Vp-p
	V_{IN2}	SYNIN pin: $V_{DD1} = 5\text{ V}$		2.0	2.5	Vp-p
	V_{IN3}	CVCR pin: $V_{DD1} = 5\text{ V}$		2.0		Vp-p
Input voltage	V_{IN4}	XtalIN pin (in external clock input mode), $f_{in} = 2f_{sc}$ or $4f_{sc}$; $V_{DD1} = 5\text{ V}$	0.10		5.0	Vp-p
Oscillator frequency	F_{OSC1}	XtalIN and XtalOUT oscillator pins (2fsc: NTSC)		7.159		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (4fsc: NTSC)		14.318		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (2fsc: PAL)		8.867		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (4fsc: PAL)		17.734		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (2fsc: PAL-M)		7.151		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (4fsc: PAL-M)		14.302		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (2fsc: PAL-N)		7.164		MHz
	F_{OSC1}	XtalIN and XtalOUT oscillator pins (4fsc: PAL-N)		14.328		MHz
	F_{OSC2}	OSCIN and OSCOUT oscillator pins (LC oscillator)	5		10	MHz

Note: If the XtalIN pin is used in clock input mode, be sure to prevent input noise from becoming a problem.

Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD1} = 5\text{ V}$ unless otherwise specified

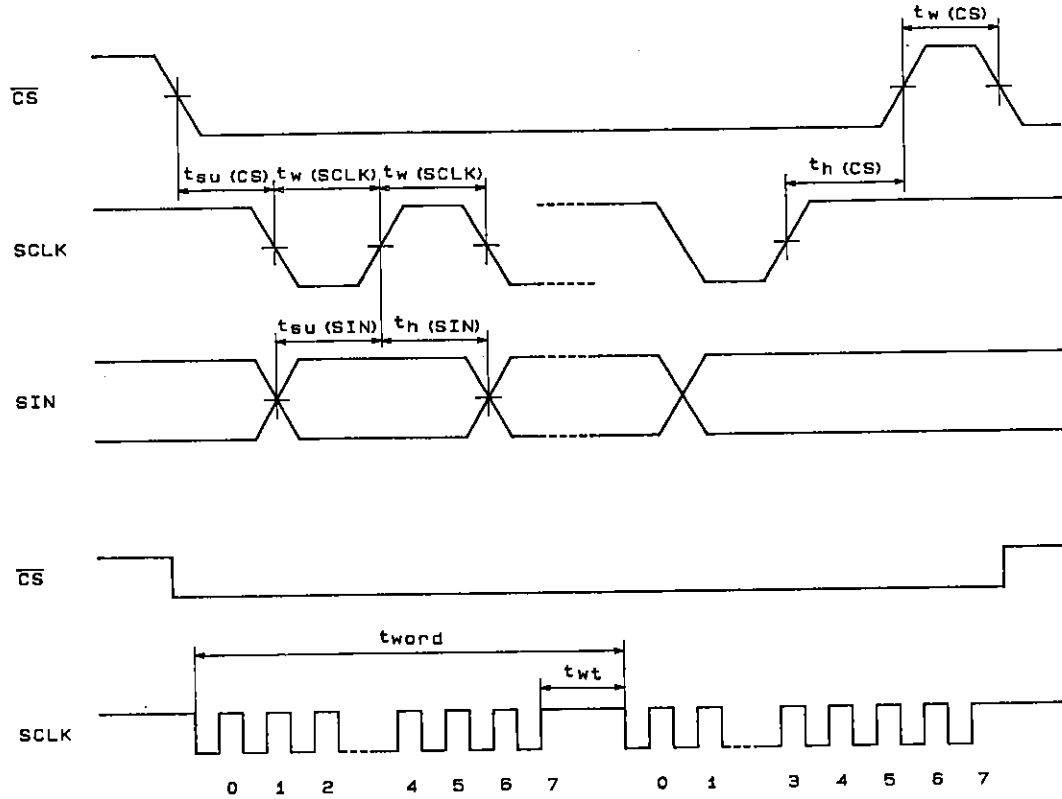
Parameter	Symbol	Conditions		min	typ	max	Unit	
Input off leakage current	I_{leak1}	CV_{IN} pin, CV_{CH} pin				1	μA	
Output off leakage current	I_{leak2}	CV_{OUT} pin				1	μA	
Output high level voltage	V_{OH1}	BLANK, CHA and SEP_{OUT} pins: $V_{\text{DD1}} = 4.5\text{ V}$, $I_{\text{OH}} = -1.0\text{ mA}$		3.5			V	
Output low level voltage	V_{OL1}	BLANK, CHA and SEP_{OUT} pins: $V_{\text{DD1}} = 4.5\text{ V}$, $I_{\text{OH}} = 1.0\text{ mA}$				1.0	V	
Input current	I_{IH}	RST , $\overline{\text{CS}}$, SIN , SCLK , CTRL1 , CTRL3 and SEP_{IN} pins: $V_{\text{IN}} = V_{\text{DD1}}$				1	μA	
	I_{IL}	CTRL1 , CTRL3 and OSC_{IN} pins: $V_{\text{IN}} = V_{\text{SS1}}$		-1			μA	
Operating current drain	I_{DD1}	V_{DD1} pin; all outputs: open, Xtal: 7.159 MHz, LC: 8 MHz				15	mA	
	I_{DD2}	V_{DD2} pin: $V_{\text{DD2}} = 5\text{ V}$				20	mA	
Sync level	V_{SN}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	0.70	0.82	0.94	V
				*2	0.91	1.03	1.15	V
Pedestal level	V_{PD}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.31	1.43	1.55	V
				*2	1.53	1.65	1.77	V
Color burst low level	V_{CBL}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.00	1.12	1.24	V
				*2	1.21	1.33	1.45	V
Color burst high level	V_{CBH}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.63	1.75	1.87	V
				*2	1.84	1.96	2.08	V
Background color low level	V_{RSL}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.47	1.59	1.71	V
				*2	1.68	1.80	1.92	V
Background color high level	V_{RSH}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.99	2.11	2.23	V
				*2	2.19	2.31	2.43	V
Border level 0	V_{BK0}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.42	1.54	1.66	V
				*2	1.63	1.75	1.87	V
Border level 1	V_{BK1}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	1.99	2.11	2.23	V
				*2	2.19	2.31	2.43	V
Character level	V_{CHA}	CV_{OUT} pin	$V_{\text{DD1}} = 5.0\text{ V}$, $V_{\text{DD2}} = 5.0\text{ V}$	*1	2.58	2.70	2.82	V
				*2	2.78	2.90	3.02	V

Note: 1. When the sync level is 0.8 V.
2. When the sync level is 1.0 V.

Timing Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{\text{DD1}} = 5 \pm 0.5\text{ V}$

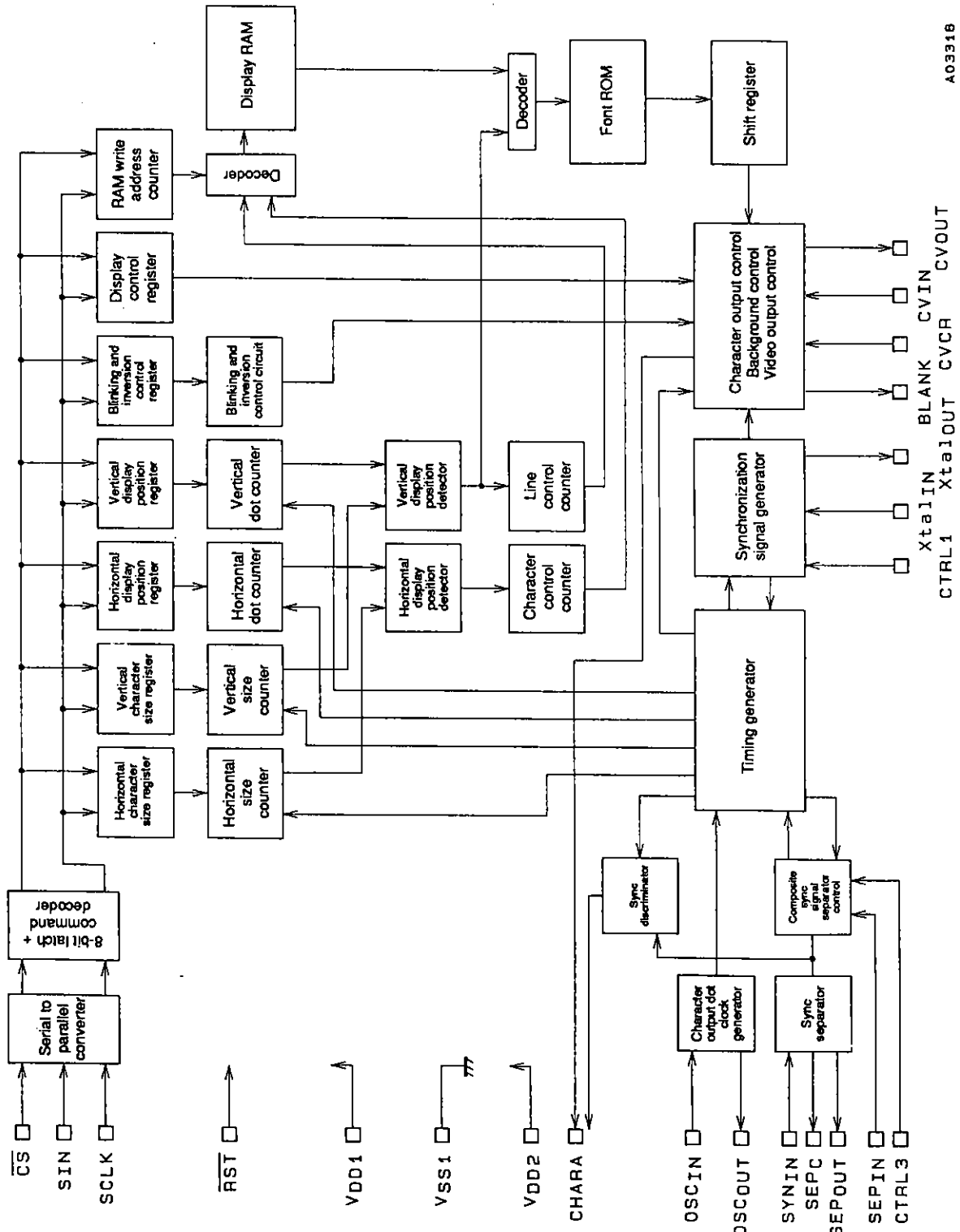
Parameter	Symbol	Conditions	min	typ	max	Unit
Minimum input pulse width	$t_{\text{W}}(\text{SCLK})$	SCLK pin	200			ns
	$t_{\text{W}}(\text{CS})$	CS pin (the period when CS is high)	1			μs
Data setup time	$t_{\text{SU}}(\text{CS})$	CS pin	200			ns
	$t_{\text{SU}}(\text{SIN})$	SIN pin	200			ns
Data hold time	$t_{\text{H}}(\text{CS})$	CS pin	2			μs
	$t_{\text{H}}(\text{SIN})$	SIN pin	200			ns
One word write time	t_{word}	8-bit data write time	4.2			μs
	t_{wt}	RAM data write time	1			μs

Serial Data Input Timing



A03317

System Block Diagram



Display Control Commands

The display control commands have a serial input format with 8-bit units. A command consists of a command identifier code in the first byte and data in the second and subsequent bytes. There are eight commands as listed below.

- ① COMMAND0: Display memory (VRAM) write address setup command
- ② COMMAND1: Display character data write command
- ③ COMMAND2: Vertical display start position and vertical character size setup command
- ④ COMMAND3: Horizontal display start position and horizontal character size setup command
- ⑤ COMMAND4: Display control setup command
- ⑥ COMMAND5: Display control setup command
- ⑦ COMMAND6: Synchronization signal detection setup command
- ⑧ COMMAND7: Display control setup command

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 (Set write address)	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 (Write character)	1	0	0	1	0	0	0	at	c7	c6	c5	c4	c3	c2	c1	c0
COMMAND2 (Set vertical display start position and vertical character size)	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 (Set horizontal display start position and horizontal character size)	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 (Display control)	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND5 (Display control)	1	1	0	1	NP 1	NP 0	NON	INT	0	0	HLF INT	BCL	CB	PH 2	PH 1	PH 0
COMMAND6 (Synchronization signal detection)	1	1	1	0	MOD 1	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND7 (Display control)	1	1	1	1	EX 1	PD 1	EX 0	PD 0	0	CIN SEL	CIN CTL	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL

Once written, the command identifier code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74784/M locks into the display character data write mode, and another first byte cannot be written.

When a high level is input to the \overline{CS} pin, the LC74784/M is set to COMMAND0 (display memory write address setup mode).

① COMMAND0 (Display memory write address setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 0 identification code Set the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory address (0 to 8 hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	H4	0	Display memory address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: The register states are all set to zero when the LC74784/M is reset with the $\overline{\text{RST}}$ pin.

② COMMAND1 (Display character data write setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 1 identification code Set up display character data write.	When this command is input, the LC74784/M locks into the display character data write mode until the $\overline{\text{CS}}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	at	0	Character attribute off	
		1	Character attribute on	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	c7	1	Character code (00 to FF hexadecimal)	
		0		
6	c6	0		
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

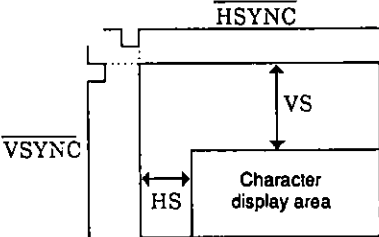
Note: The register states are all set to zero when the LC74784/M is reset with the RST pin.

③ COMMAND2 (Vertical display start position and vertical character size setup command)

First byte

DA0 to DA7	Register name	Register content		Note									
		State	Function										
7	—	1	Command 2 identification code Set the vertical display start position and vertical character size.										
6	—	0											
5	—	1											
4	—	0											
3	VS21	0	<table><tr><td>VS21 \ VS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H per dot</td><td>2H per dot</td></tr><tr><td>1</td><td>3H per dot</td><td>1H per dot</td></tr></table>	VS21 \ VS20	0	1	0	1H per dot	2H per dot	1	3H per dot	1H per dot	Second line vertical character size
		VS21 \ VS20		0	1								
0	1H per dot	2H per dot											
1	3H per dot	1H per dot											
1													
2	VS20	0											
		1											
1	VS11	0	<table><tr><td>VS11 \ VS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H per dot</td><td>2H per dot</td></tr><tr><td>1</td><td>3H per dot</td><td>1H per dot</td></tr></table>	VS11 \ VS10	0	1	0	1H per dot	2H per dot	1	3H per dot	1H per dot	First line vertical character size
		VS11 \ VS10		0	1								
0	1H per dot	2H per dot											
1	3H per dot	1H per dot											
1													
0	VS10	0											
		1											

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	FS	0	Crystal oscillator frequency: 2fsc	
		1	Crystal oscillator frequency: 4fsc	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times (2^5 \sum_{n=0}^5 2^n VP_n)$ H: the horizontal synchronization pulse period 	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: The register states are all set to zero when the LC74784/M is reset with the \overline{RST} pin.

④ COMMAND3 (Horizontal display start position and horizontal character size setup command)

First byte

DA0 to DA7	Register name	Register content		Note									
		State	Function										
7	—	1	Command 3 identification code Set the horizontal display start position and horizontal character size.										
6	—	0											
5	—	1											
4	—	1											
3	HS21	0	<table><tr><td>HS21 \ HS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1 Tc per dot</td><td>2 Tc per dot</td></tr><tr><td>1</td><td>3 Tc per dot</td><td>1 Tc per dot</td></tr></table>	HS21 \ HS20	0	1	0	1 Tc per dot	2 Tc per dot	1	3 Tc per dot	1 Tc per dot	Second line horizontal character size
		HS21 \ HS20		0	1								
0	1 Tc per dot	2 Tc per dot											
1	3 Tc per dot	1 Tc per dot											
1													
2	HS20	0											
		1											
1	HS11	0	<table><tr><td>HS11 \ HS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1 Tc per dot</td><td>2 Tc per dot</td></tr><tr><td>1</td><td>3 Tc per dot</td><td>1 Tc per dot</td></tr></table>	HS11 \ HS10	0	1	0	1 Tc per dot	2 Tc per dot	1	3 Tc per dot	1 Tc per dot	First line horizontal character size
		HS11 \ HS10		0	1								
0	1 Tc per dot	2 Tc per dot											
1	3 Tc per dot	1 Tc per dot											
1													
0	HS10	0											
		1											

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	LC	0	An LC oscillator is used for the dot clock.	Selects the dot clock used in horizontal character display.
		1	A crystal oscillator is used for the dot clock.	
5	HP5 (MSB)	0	If HS is the horizontal start position then: $HS = Tc \times (2^5 \sum_{n=0}^5 2^n HP_n)$ Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.	The horizontal display start position is set by the six bits HP5 to HP0. The weight of bit 1 is 2Tc.
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: The register states are all set to zero when the LC74784/M is reset with the \overline{RST} pin.

⑤ COMMAND4 (Display control setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 4 identification code Display control	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be zero.
		1	Test mode	
2	RAMERS	0		The RAM erase operation requires about 500 μ s (It is executed in the DSPOFF state.)
		1	Erase display RAM (set to FF hexadecimal)	
1	OSCSTP	0	Do not stop the crystal oscillator and LC oscillator circuits.	Valid when character display is off in external synchronization mode.
		1	Stop the crystal oscillator and LC oscillator circuits.	
0	SYSRST	0		Reset occurs when the \overline{CS} pin is low, and the reset is cleared when CS goes high.
		1	Reset all registers and turn the display off.	

Second byte

DA0 to DA7	Register name	Register content			Note									
		State	Function											
7	—	0	Second byte identification bit											
6	BLK2	0	Character display block		Full character size specification									
		1	Video display block											
5	BLK1	0	<table border="1"><tr><td>BLK1 \ BLK0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blanking off</td><td>Character size</td></tr><tr><td>1</td><td>Border size</td><td>Full character size</td></tr></table>		BLK1 \ BLK0	0	1	0	Blanking off	Character size	1	Border size	Full character size	Changes the blanking size.
		BLK1 \ BLK0			0	1								
0	Blanking off	Character size												
1	Border size	Full character size												
1														
4	BLK0	0												
		1												
3	BK1	0	Blinking period: about 0.5 s		Switches the blinking period.									
		1	Blinking period: about 1.0 s											
2	BK0	0	Blinking off		When blinking is specified for reversed characters, the blinking will be between normal character and reversed character display.									
		1	Blinking on											
1	RV	0	Reverse (character reversing) off											
		1	Reverse (character reversing) on											
0	DSPON	0	Character display off											
		1	Character display on											

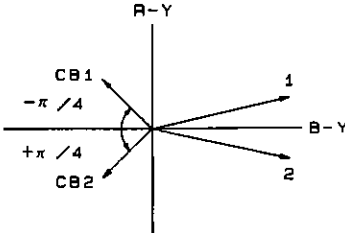
Note: The register states are all set to zero when the LC74784/M is reset with the \overline{RST} pin.

⑥ COMMAND5 (Display control setup command)

First byte

DA0 to DA7	Register name	Register content			Note									
		State	Function											
7	—	1	Command 5 identification code Display control											
6	—	1												
5	—	0												
4	—	1												
3	NP1	0	<table><tr><td>NP1 \ NP0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>NTSC</td><td>PAL-M</td></tr><tr><td>1</td><td>PAL</td><td>PAL-N</td></tr></table>		NP1 \ NP0	0	1	0	NTSC	PAL-M	1	PAL	PAL-N	Switches between NTSC, PAL, PAL-M and PAL-N
		NP1 \ NP0			0	1								
0	NTSC	PAL-M												
1	PAL	PAL-N												
1														
2	NP0	0												
		1												
1	NON	0	Interlaced		Switches between interlaced and non-interlaced displays									
		1	Non-interlaced											
0	INT	0	External synchronization		Switches between external and internal synchronization									
		1	Internal synchronization											

Second byte

DA0 to DA7	Register name	Register content						Note
		State	Function					
7	—	0	Second byte identification bit					
6	—	0						
5	HLFINT	0	Normal mode					
		1	Half internal synchronization mode					
4	BCL	0	Background color present					Only valid with internal synchronization.
		1	No background color (only the background level is set)					
3	CB	0	Outputs a color burst signal.					Only valid when BCL is high.
		1	Stops color burst signal output.					
2	PH2	0	Phase 2	Phase 1	Phase 0	Background color (phase)		Sample background color phase diagram for PAL mode color burst 
		NTSC				PAL		
1	0	0	0	$\pi/2^*$	$\pm\pi/2$			
1	PH1	0	0	0	1	In phase*	In phase	
		0	1	0	$3\pi/2^*$	$\mp\pi/2$		
		0	1	1	π^*	$\pm\pi$		
		1	0	0	$3\pi/4$	$\pm 3\pi/4$		
0	PH0	0	1	0	1	$\pi/4$	$\pm\pi/4$	
		1	1	0	$7\pi/4$	$\mp\pi/4$		
		1	1	1	$5\pi/4$	$\mp 3\pi/4$		

*: When 2fsc NTSC is used

A03319

Note: The register states are all set to zero when the LC74784/M is reset with the RST pin.

⑦ COMMAND6 (Synchronization signal detection setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 6 identification code Synchronization signal control settings	
6	—	1		
5	—	1		
4	—	0		
3	MOD1	0	Sync separator circuit signal	Switches the SEP _{OUT} (pin 19) output
		1	High level output during internal synchronization	
2	MOD0	0	Pin 5: Blank signal Pin 8: Character signal	Switches the BLANK (pin 5) and CHARA (pin 8) outputs
		1	Pin 5: Composite synchronization signal Pin 8: External synchronization signal discrimination output signal	
1	DISLIN	0	12 lines	Switches the number of display lines.
		1	10 lines	
0	MUT	0	Normal output	Switches CV _{OUT}
		1	CV _{IN} is cut and CV _{OUT} is fixed at the pedestal level.	

Second byte

DA0 to DA7	Register name	Register content				Note																													
		State	Function																																
7	—	0	Second byte identification bit																																
6	RN2	0	<table><tr><th>RN2</th><th>RN1</th><th>RN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>4 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>8 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>16 times</td></tr></table>	RN2	RN1	RN0	Number of times HSYNC detected	0	0	0	0 times	0	0	1	4 times	0	1	0	8 times	1	0	0	16 times	External synchronization signal detection control Signal absent to present transition recognition Setting for the sampling period when SYNC can be detected consecutively in the horizontal synchronization signal period (1H).											
		RN2		RN1	RN0	Number of times HSYNC detected																													
0	0	0		0 times																															
0	0	1		4 times																															
0	1	0		8 times																															
1	0	0		16 times																															
1																																			
5	RN1	0																																	
		1																																	
4	RN0	0																																	
		1																																	
3	SN3	0	<table><tr><th>SN3</th><th>SN2</th><th>SN1</th><th>SN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Not detected</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>32 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>64 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>128 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>256 times</td></tr></table>	SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronization signal detection control Signal present to absent transition recognition Setting for the sampling period when SYNC can not be detected consecutively in the horizontal synchronization signal period (1H).	
		SN3		SN2	SN1	SN0	Number of times HSYNC detected																												
0	0	0		0	Not detected																														
0	0	0		1	32 times																														
0	0	1		0	64 times																														
0	1	0		0	128 times																														
1	0	0		0	256 times																														
1																																			
2	SN2	0																																	
		1																																	
1	SN1	0																																	
		1																																	
0	SN0	0																																	
		1																																	

Note: The register states are all set to zero when the LC74784/M is reset with the $\overline{\text{RST}}$ pin.

⑧ COMMAND7 (Display control setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	EX1	0	MODE1 setting output	Switches the SEP _{OUT} (pin 19) output
		1	PORT DATA1 setting output	
2	PD1	0	The output is set low.	
		1	The output is set high.	
1	EX0	0	MODE0 setting output	Switches the BLANK (pin 5) output
		1	PORT DATA0 setting output	
0	PD0	0	The output is set low.	
		1	The output is set high.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	CINSEL	0	Blank (the OR of the character and the border) signal area	Switches the CV _{CR} on signal
		1	Video signal display area	
5	CINCTL	0	CV _{CR} : Off	CV _{CR} on/off setting
		1	CV _{CR} : On	
4	VNPSEL	0	V falling edge detection	Switches V acquisition polarity when internal V separation is used in external mode.
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 μ s (for NTSC)	Switches the internal V separation time.
		1	VSEP: about 17.8 μ s (for NTSC)	
2	MSKERS	0	Mask valid	HSYNC and VSYNC mask release
		1	Mask invalid	
1	MSKSEL	0	3H (for NTSC)	Switches the VSYNC mask.
		1	20H (for NTSC)	
0	EGL	0	Border level 0 only (VBK0)	Switches the border level (Only valid for BLK0 = 0 and BLK1 = 1)
		1	Border level has two stages (VBK0, VBK1)	

Note: The register states are all set to zero when the LC74784/M is reset with the $\overline{\text{RST}}$ pin.

Display Screen Structure

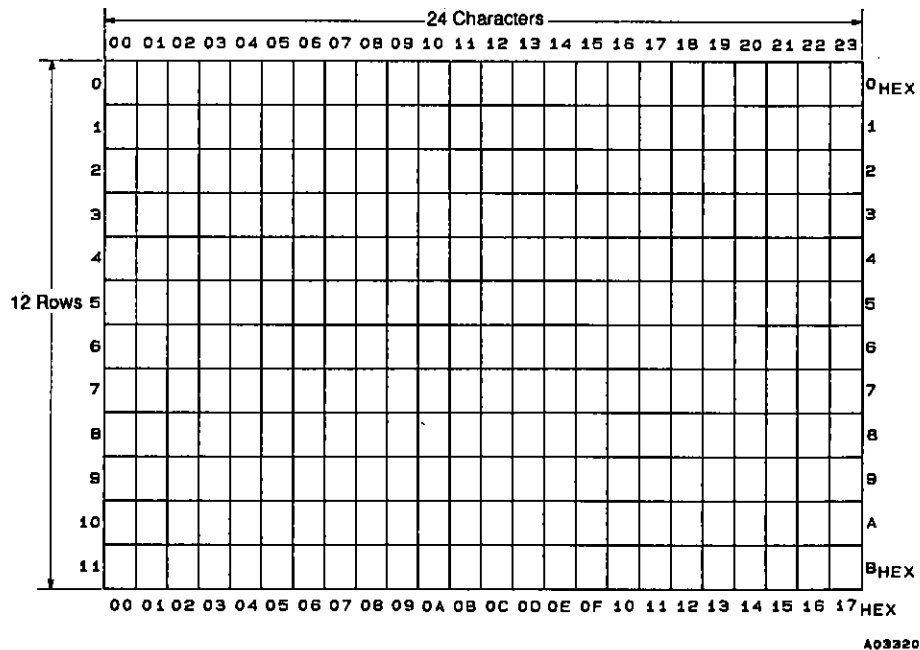
The display consists of 24 characters \times 12 rows.

The maximum number of displayed character is 288.

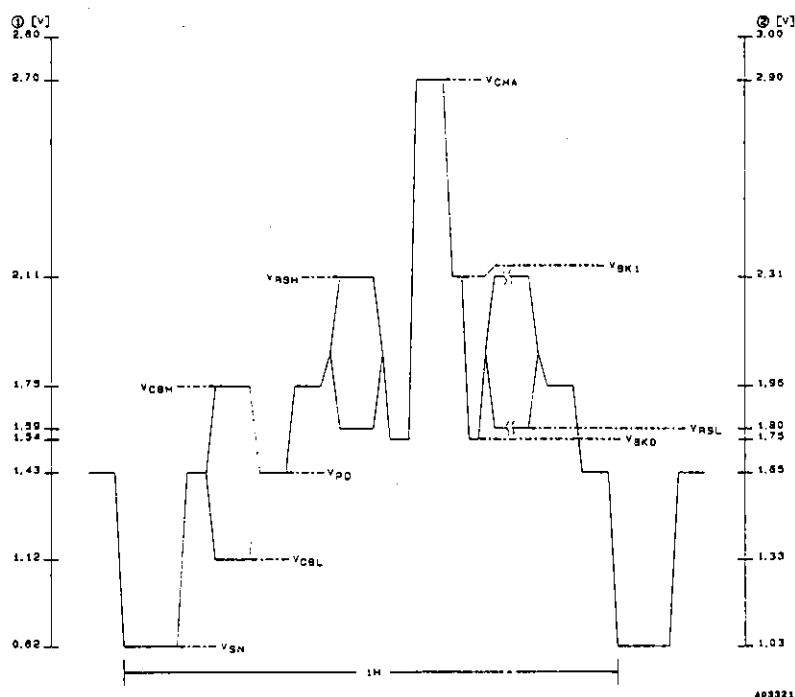
The maximum number of characters is reduced to less than 288 when the character size is enlarged.

Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Level (Internally generated level)

CV_{OUT} output level waveform (V_{DD2} = 5.00 V)

Output level	Output voltage ① [V]	Output voltage ② [V]
V _{CHA} : Character	2.70	2.90
V _{BK1} : Border	2.11	2.31
V _{RSH} : Background color high	2.11	2.31
V _{CBH} : Color burst high	1.75	1.96
V _{RSL} : Background color low	1.59	1.80
V _{BK0} : Border	1.54	1.75
V _{PD} : Pedestal	1.43	1.65
V _{CBL} : Color burst low	1.12	1.33
V _{SN} : Sync	0.82	1.03

V_{DD2} = 5.00 V

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of September, 1995. Specifications and information herein are subject to change without notice.