



LC74798, 74798M

On-Screen Display Controller IC

Overview

The LC74798 and LC74798M are on-screen display controller CMOS ICs that display characters and patterns on the TV screen under microprocessor control. These ICs include a built-in PDC/VPS/UDT interface circuit.

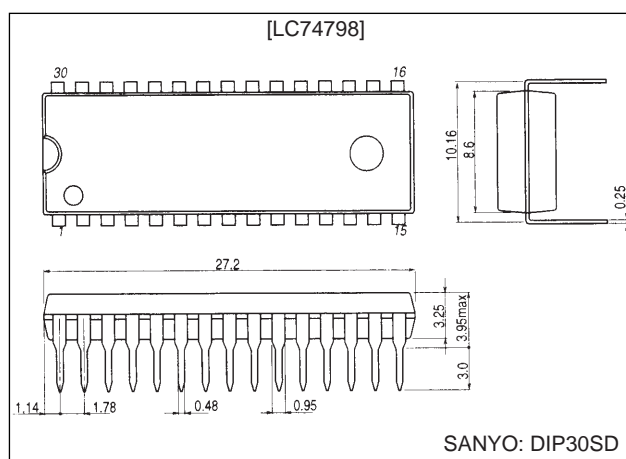
Features

- Display format: 24 characters by 12 rows (Up to 288 characters)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three sizes each in the horizontal and vertical directions
- Characters in font: 128
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types: Two periods supported: 1.0 second and 0.5 second
- Blanking: Over the whole font (12 × 18 dots)
- Background color
 - 8 colors (internal synchronization mode): 4fSC
 - 6 colors (internal synchronization mode): 2fSC
 - Blue background only: NTSC
- Line background color
 - Three lines can be set up.
 - 8 line background colors (in internal synchronization mode): 4fSC
 - 6 line background colors (in internal synchronization mode): 2fSC
- External control input: 8-bit serial input format
- On-chip sync separator and AFC circuits
- On-chip PDC/VPS/UDT interface circuit
- Video outputs: PAL and NTSC format composite video outputs
- Package: DIP30SD (400 mil)
MFP30S (375 mil)

Package Dimensions

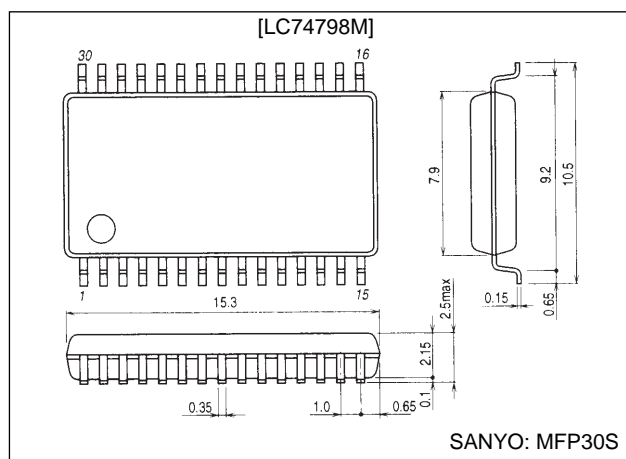
unit: mm

3193-DIP30SD

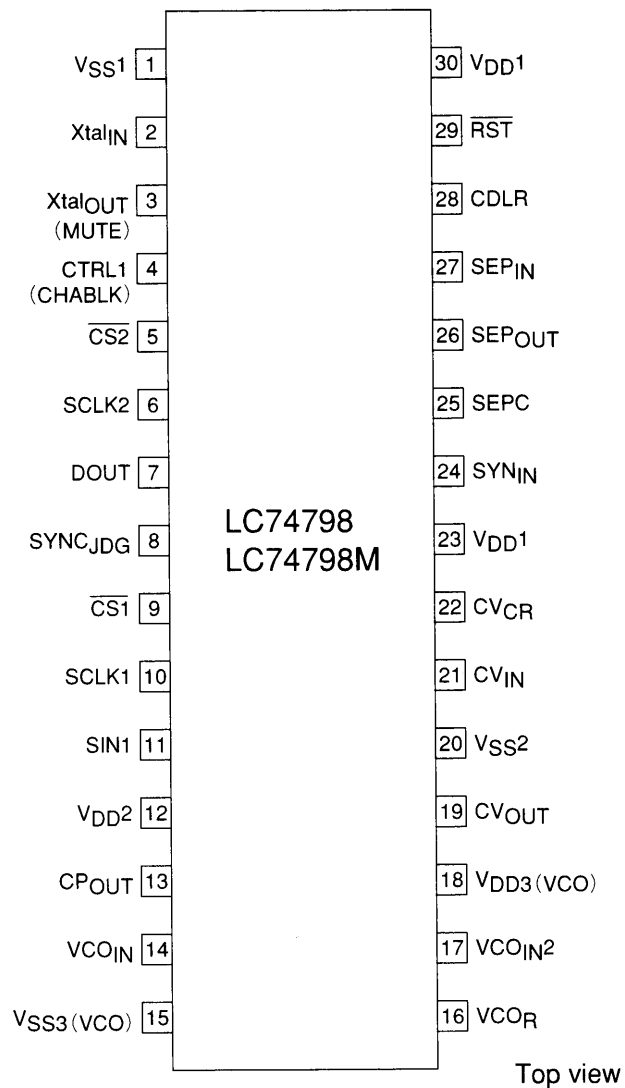


unit: mm

3216-MFP30S



Pin Assignment



Top view

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Pin Descriptions

Pin No.	Pin name	Function	Notes
1	V _{SS1}	Ground	Ground connection (digital system ground)
2	Xtal _{IN}	Crystal oscillator (MUTE input)	These pins are used either to connect the crystal and capacitors used to form an external crystal oscillator circuit to generate the internal synchronizing signals, or to input an external clock signal (2fsc or 4fsc). As a mask option, the Xtal _{OUT} pin can be set to function as the MUTE input pin. When this pin is set low, the video output is held at the pedestal level. (A pull-up resistor is built in and the input has hysteresis characteristics.)
3	Xtal _{OUT} (MUTE)		
4	CTRL1 (CHABLK)	Crystal oscillator input switching (CHABLK output)	Switches the mode between external clock input and crystal oscillator operation. A low level selects crystal oscillator operation and a high level selects external clock input. As a mask option, the CTRL1 input pin can be set to function as the CHABLK (character - frame) output. This is a 3-value output.
5	$\overline{\text{CS2}}$	Enable input 2	Enable input for the PDC/VPS data output. Data output is enabled when this input is low. A pull-up resistor is built in and the input has hysteresis characteristics.
6	SCLK2	Clock input 2	Clock input for the PDC/VPS data output. A pull-up resistor is built in and the input has hysteresis characteristics.
7	DOUT	Data output	PDC/VPS data output. (This can be either an n-channel open-drain output or a CMOS output.)
8	SYNC _{JDG}	External synchronizing signal judgment output	Outputs the state of the external synchronizing signal presence/absence judgment. Outputs a high level when synchronizing signals are present. Outputs the crystal oscillator clock when CS1 and RST are low. (This signal is not output on command resets.)
9	$\overline{\text{CS1}}$	Enable input 1	Enable input for the OSD serial data input. Serial data input is enabled when this pin is low. A pull-up resistor is built in and the input has hysteresis characteristics.
10	SCLK1	Clock input 1	Serial data input enable pin. A pull-up resistor is built in and the input has hysteresis characteristics.
11	SIN1	Data input 1	Serial data input. A pull-up resistor is built in and the input has hysteresis characteristics.
12	V _{DD2}	Power supply	Composite video signal level adjustment power supply (analog system power supply)
13	CP _{OUT}	Charge pump output	Charge pump output. Connect a low-pass filter to this pin.
14	VCO _{IN}	Oscillator control voltage input	VCO oscillator control voltage input. (For data slicing)
15	V _{SS3}	Ground	Ground (VCO ground)
16	VCO _R	Oscillator range adjustment	VCO oscillator range adjustment resistor connection
17	VCO _{IN2}	Oscillator control voltage input 2	VCO oscillator control voltage input. For character display.
18	V _{DD3}	Power supply (+5 V)	Power supply (+5 V: VCO power supply)
19	CV _{OUT}	Video signal output	Composite video signal output
20	V _{SS2}	Ground	Ground (analog system ground)
21	CV _{IN}	Video signal input	Composite video signal input
22	CV _{CR}	Video signal input	SECAM chrominance signal input
23	V _{DD1}	Power supply (+5 V)	Power supply (+5 V: digital system power supply)
24	SYN _{IN}	Sync separator circuit input	Video signal input to the internal sync separator circuit
25	SEPC	Sync separator circuit adjustment	Internal sync separator circuit adjustment
26	SEP _{OUT}	Composite synchronizing signal output	Internal sync separator circuit composite synchronizing signal output. Can be switched to function as a signal (high, low, or ST. pulse) output by the MOD0 setting when SEL0 is high.
27	SEP _{IN}	Vertical synchronizing signal input	Inputs the vertical synchronizing signal created by integrating the SEP _{OUT} pin output signal. An integration circuit must be connected between this pin and the SEP _{OUT} pin. This pin must be tied to V _{DD1} if unused. This pin is valid when CTL3 is set high.
28	CDLR	Background color phase adjustment	Background color phase adjustment resistor connection
29	$\overline{\text{RST}}$	Reset input	System reset input. A pull-up resistor is built in and the input has hysteresis characteristics.
30	V _{DD1}	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note *: A capacitor of at least 2000 pF must be connected between the V_{DD1} power supply and V_{SS1}.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$	V_{DD1} and V_{DD2}	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Maximum input voltage	V_{IN}	All input pins	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Maximum output voltage	V_{OUT}	D_{OUT} , SEP_{OUT} , $SYNC_{JDG}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\ max$	$T_a = 25^\circ\text{C}$	350	mW
Operating temperature	T_{opr}		-30 to $+70$	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to $+125$	$^\circ\text{C}$

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	V_{DD1} and V_{DD2}	4.5	5.0	5.5	V
	V_{DD2}	V_{DD2}	4.5	5.0	$1.27 V_{DD1}$	V
Input high-level voltage	V_{IH1}	\overline{RST} , $\overline{CS1}$, $\overline{CS2}$, $SIN1$, $SCLK1$, $SCLK2$, $MUTE$	$0.8 V_{DD1}$		$V_{DD1} + 0.3$	V
	V_{IH2}	$CTRL1$	$0.7 V_{DD1}$		$V_{DD1} + 0.3$	V
Input low-level voltage	V_{IL1}	\overline{RST} , $\overline{CS1}$, $\overline{CS2}$, $SIN1$, $SCLK1$, $SCLK2$, $MUTE$	$V_{SS} - 0.3$		$0.2 V_{DD1}$	V
	V_{IL2}	$CTRL1$	$V_{SS} - 0.3$		$0.3 V_{DD1}$	V
Pull-up resistance	R_{PU}	\overline{RST} , $\overline{CS1}$, $\overline{CS2}$, $SIN1$, $SCLK1$, $SCLK2$, $MUTE$ Applies to pins set up by options.	25	50	90	$k\Omega$
Composite video signal input voltage	V_{IN1}	CV_{IN} and CV_{CR} : $V_{DD1} = 5\text{ V}$		2.0		Vp-p
	V_{IN2}	SYN_{IN} : $V_{DD1} = 5\text{ V}$	1.5	2.0	2.5	Vp-p
Input voltage	V_{IN3}	$Xtal_{IN}$ (when used for external clock input) $f_{IN} = 2f_{sc}$ or $4f_{sc}$: $V_{DD1} = 5\text{ V}$	0.10		5.0	Vp-p
Oscillator frequencies	F_{OSC1}	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($2f_{sc}$: PAL)		8.867		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($4f_{sc}$: PAL)		17.734		MHz

Note: Applications must be especially cautious about noise when using the $Xtal_{IN}$ input pin in clock input mode.

Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD1} = 5\text{ V}$ unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input off leakage current	I_{leak1}	CV_{IN} and CV_{CR}			1	μA
Output off leakage current	I_{leak2}	CV_{OUT}			1	μA
Output high-level voltage	V_{OH1}	D_{OUT} , SEP_{OUT} , CP_{OUT} , and $SYNC_{JDG}$ $V_{DD1} = 4.5\text{ V}$, $I_{OH} = -1.0\text{ mA}$	3.5			V
Output low-level voltage	V_{OL1}	D_{OUT} , SEP_{OUT} , CP_{OUT} , and $SYNC_{JDG}$ $V_{DD1} = 4.5\text{ V}$, $I_{OL} = -1.0\text{ mA}$			1.0	V
Three-value output voltage	V_O	$CHABLK$: $V_{DD1} = 5.0\text{ V}$	H	3.3	5.0	V
			M	1.8	2.3	V
			L	0	0.8	V
Input current	I_{IH}	\overline{RST} , $\overline{CS1}$, $\overline{CS2}$, SIN , $SCLK1$, $SCLK2$, $CTRL1$, $MUTE$, SEP_{IN} , $VCOIN$, and $VCOIN2$, $V_{IN} = V_{DD1}$			1	μA
	I_{IL}	$CTRL1$, SEP_{IN} , $VCOIN$, and $VCOIN2$, $V_{IN} = V_{SS1}$	-1			μA
Operating mode current drain	I_{DD1}	V_{DD1} : With all outputs open $Xtal$: 17.734 MHz, VCO : 27 MHz			40	mA
	I_{DD2}	V_{DD2} : $V_{DD2} = 5\text{ V}$			20	mA
SYNC level	V_{SN}	CV_{OUT} : $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$	(1)	0.80		V
			(2)	1.00		V
			(3)	1.40		V
Pedestal level	V_{PD}	CV_{OUT} : $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$	(1)	1.37		V
			(2)	1.57		V
			(3)	1.97		V
Color burst low level	V_{CBL}	CV_{OUT} : $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$	(1)	1.07		V
			(2)	1.27		V
			(3)	1.67		V
Color burst high level	V_{CBH}	CV_{OUT} : $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$	(1)	1.67		V
			(2)	1.87		V
			(3)	2.27		V

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Background color low level	V_{RSL}	$CV_{OUT} : V_{DD1} = 5.0 \text{ V}, V_{DD2} = 5.0 \text{ V}$	(1)	1.23 (1.16)		V
			(2)	1.43 (1.36)		V
			(3)	1.83 (1.76)		V
Background color high level	V_{RSH}	$CV_{OUT} : V_{DD1} = 5.0 \text{ V}, V_{DD2} = 5.0 \text{ V}$	(1)	2.37 (2.01)		V
			(2)	2.57 (2.21)		V
			(3)	2.97 (2.61)		V
Frame level 0	V_{BK0}	$CV_{OUT} : V_{DD1} = 5.0 \text{ V}, V_{DD2} = 5.0 \text{ V}$	(1)	1.50		V
			(2)	1.70		V
			(3)	2.10		V
Frame level 1	V_{BK1}	$CV_{OUT} : V_{DD1} = 5.0 \text{ V}, V_{DD2} = 5.0 \text{ V}$	(1)	2.08		V
			(2)	2.28		V
			(3)	2.68		V
Character level	V_{CHA}	$CV_{OUT} : V_{DD1} = 5.0 \text{ V}, V_{DD2} = 5.0 \text{ V}$	(1)	2.65		V
			(2)	2.85		V
			(3)	3.25		V

Notes: (1): When the sync level = 0.8 V

(2): When the sync level = 1.0 V

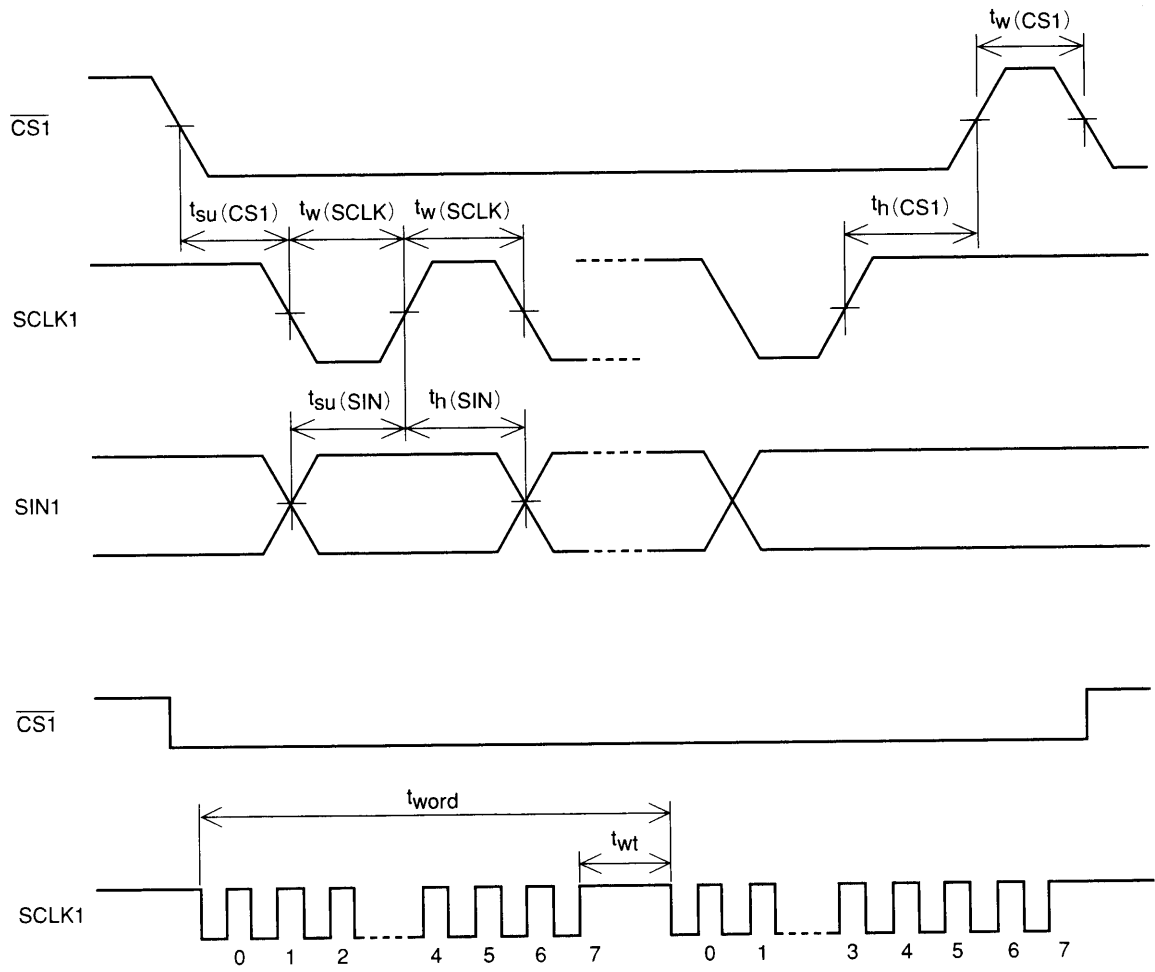
(3): When the sync level = 1.4 V

The values in parentheses for the background high and low levels are for blue background mode.

Timing Characteristics at $T_a = -30 \text{ to } +70^\circ\text{C}$, $V_{DD1} = 5 \pm 0.5 \text{ V}$

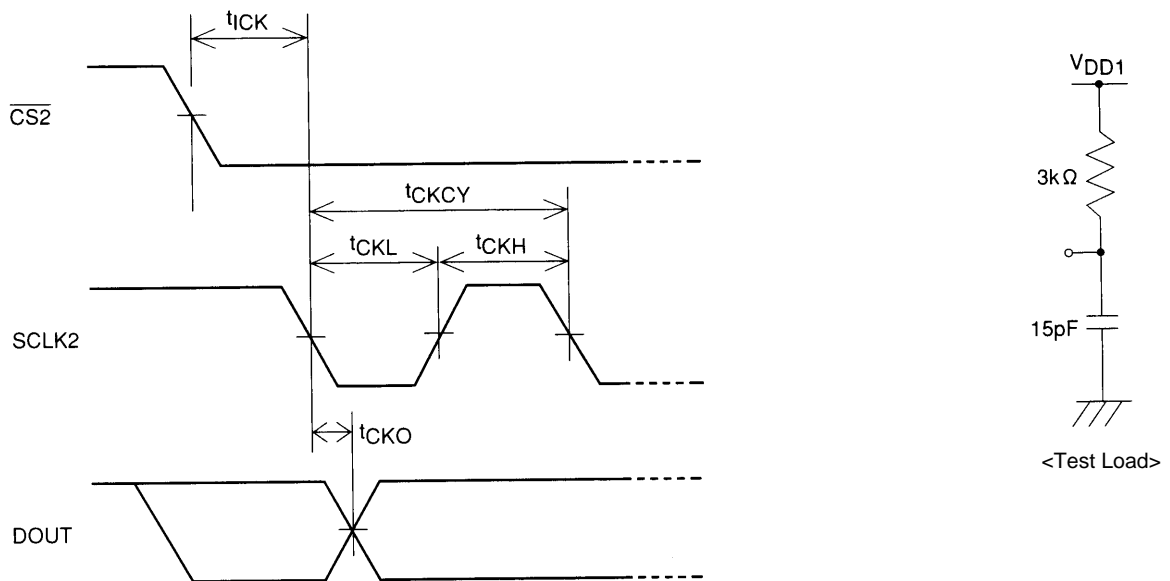
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
OSD write (See figure 1.)						
Minimum input pulse width	t _W (SCLK)	SCLK1	200			ns
	t _W (CS1)	CS1 (The period when CS1 is high)	1			μs
Data setup time	t _{SU} (CS1)	CS1	200			ns
	t _{SU} (SIN)	SIN1	200			ns
Data hold time	t _h (CS1)	CS1	2			μs
	t _h (SIN)	SIN1	200			ns
One word write time	t _{word}	The 8-bit data write time	4.2			μs
	t _{wt}	The RAM data write time	1			μs
PDC/VPS write (For the n-channel open-drain output circuit type. See figure 2)						
Minimum input pulse width	t _{CKCY}	SCLK2	2			μs
	t _{CKL}	SCLK2	1			μs
	t _{CKH}	SCLK2	1			μs
Setup time	t _{ICK}	SCLK2	10			μs
Output delay time	t _{CKO}	DOUT			0.5	μs

Note: The OSD timing applies when the CMOS output circuit type is used.



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Figure 1 OSD Serial Data Input Timing

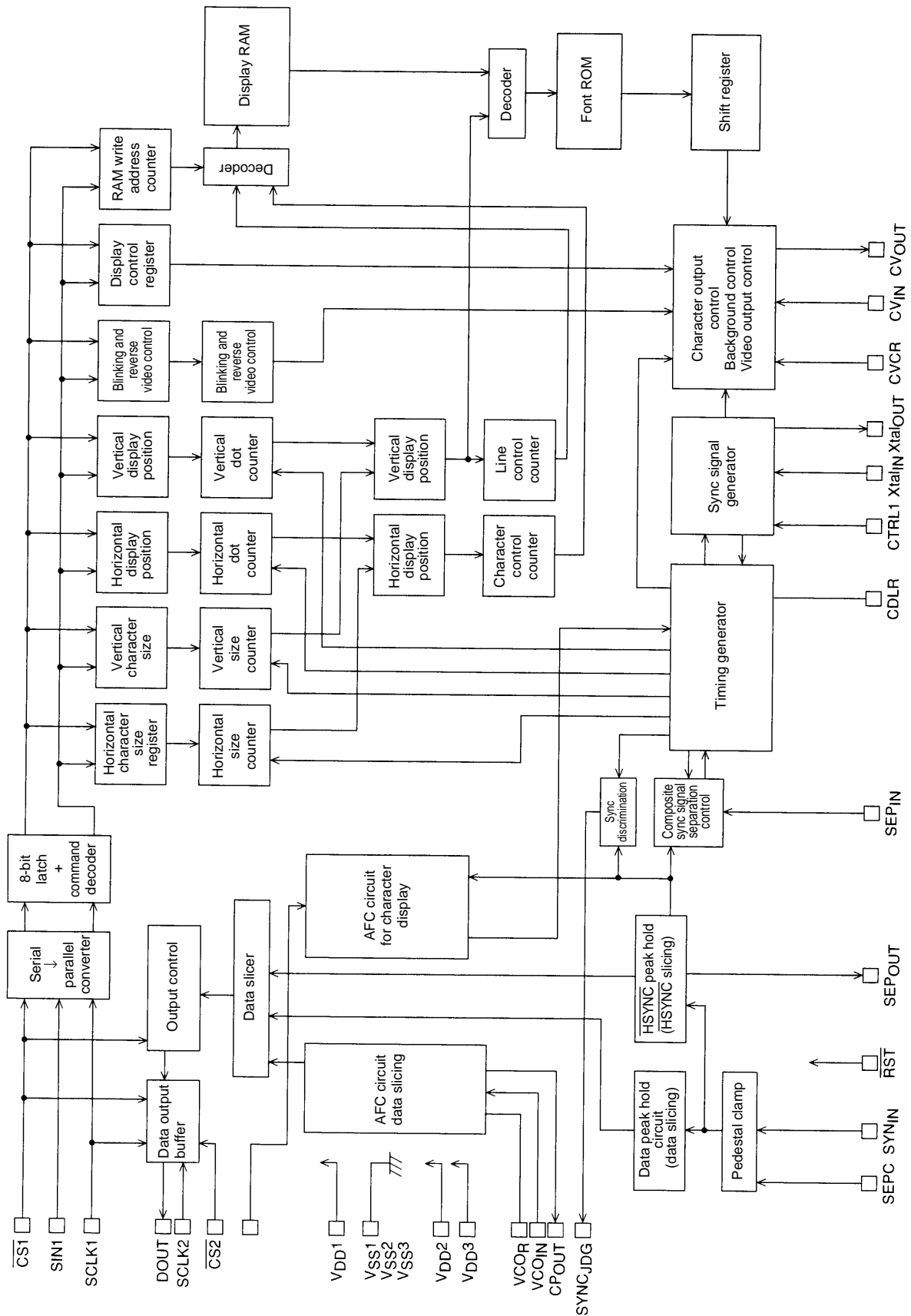


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Note: DOUT goes to the high-impedance state while $\overline{CS2}$ is high.

Figure 2 PDC/VPS Serial Output Test Conditions (For the n-channel open-drain output circuit type.)

System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

- 1 COMMAND0: Display memory (VRAM) write address setup command
- 2 COMMAND1: Display character data write command
- 3 COMMAND2: Vertical display start position and vertical character size setup command
- 4 COMMAND3: Horizontal display start position and horizontal character size setup command
- 5 COMMAND4: Display control setup command
- 6 COMMAND5: Display control setup command
- 7 COMMAND6: Synchronizing signal detection setup command
- 8 COMMAND7 to COMMAND12: Display control setup commands
- 9 COMMAND13 to COMMAND17: VPS/PDC control commands

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 (Write address setup)	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 (Character write)	1	0	0	1	0	0	0	0	at	c6	c5	c4	c3	c2	c1	c0
COMMAND2 (Vertical character size and vertical display start position)	1	0	1	0	VS	VS	VS	VS	0	FS	VP	VP	VP	VP	VP	VP
					21	20	11	10			5	4	3	2	1	0
COMMAND3 (Horizontal character size and horizontal display start position)	1	0	1	1	HS	HS	HS	HS	0	0	HP	HP	HP	HP	HP	HP
					21	20	11	10			5	4	3	2	1	0
COMMAND4 (Display control)	1	1	0	0	TST	RAM	OSC	SYS	0	BLK	BLK	BLK	BK	BK	RV	DSP
					MOD	ERS	STP	RST		2	1	0	1	0		ON
COMMAND5 (Display control)	1	1	0	1	NP1	NP0	NON	INT	0	RSH	HLF	BCL	CB	PH	PH	PH
										LV2	INT			2	1	0
COMMAND6 (Synchronizing signal detection)	1	1	1	0	SEL	MOD	DIS	MUT	0	RN	RN	RN	SN	SN	SN	SN
					0	0	LIN			2	1	0	3	2	1	0
COMMAND7 (Display control)	1	1	1	1	0	0	0	0	0	CIN	CIN	VNP	VSP	MSK	MSK	EGL
										SEL	CTL	SEL	SEL	ERS	SEL	
COMMAND8 (Display control)	1	1	1	1	0	0	0	1	0	LNA	LNA	LNA	LNA	LPA	LPA	LPA
										3	2	1	0	2	1	0
COMMAND9 (Display control)	1	1	1	1	0	0	1	0	0	LNB	LNB	LNB	LNB	LPB	LPB	LPB
										3	2	1	0	2	1	0
COMMAND10 (Display control)	1	1	1	1	0	0	1	1	0	LNC	LNC	LNC	LNC	LPC	LPC	LPC
										3	2	1	0	2	1	0
COMMAND11 (Display control)	1	1	1	1	0	1	0	0	0	0	VSP	VSP	LNC	MOD	LNB	MOD
											DCK	SLC	SEL	3	SEL	2
COMMAND12 (Display control)	1	1	1	1	0	1	0	1	0	VIN	VIN	SEL	HLF	SEL	SEL	CTL
										NP	2	22	TON	2	1	3
COMMAND13 (VPS/PDC control)	1	1	1	1	0	1	1	0	0	CPA	CPA	0	VPM	VPM	VPM	VPM
										1	0		3	2	1	0
COMMAND14 (VPS/PDC control)	1	1	1	1	0	1	1	1	0	VMW	VMW	HBS	HBS	BMS	EMS	DCE
										SE2	SEL	2	1			
COMMAND15 (VPS/PDC control)	1	1	1	1	1	0	0	0	0	0	ECV	ECV	ECV	ECV	ECV	ECV
											15	14	13	12	11	5
COMMAND16 (VPS/PDC control)	1	1	1	1	1	0	0	1	0	ECP	ECP	ECP	ECP	ECP	ECP	ECP
										19	18	17	16	15	14	13
COMMAND17 (VPS/PDC control)	1	1	1	1	1	0	1	0	0	0	ECP	ECP	ECP	ECP	ECP	ECP
											25	24	23	22	21	20

Once written, a first byte command identification code is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74798/M locks into the display character data write mode, and another first byte cannot be written. When the CS pin is set high, the LC74798/M is set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 0 identification code. Sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to B hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND1 (Display character data write setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 1 identification code. Sets up display character data write mode.	When this command is input, the LC74798/M locks in the display character data write mode until the $\overline{\text{CS}}$ pin goes high
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	at	0	Character attribute off	
		1	Character attribute on	
6	c6	0	Character code (00 to 7F hexadecimal)	
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

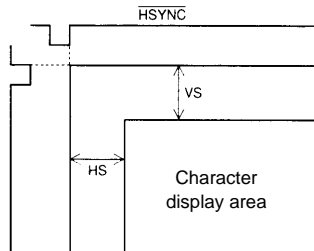
COMMAND2 (Vertical display start position and vertical character size setup command)

• First byte

DA 0 to 7	Register	Contents		Notes									
		State	Function										
7	—	1	Command 2 identification code. Sets the vertical display start position and the vertical character size.										
6	—	0											
5	—	1											
4	—	0											
3	VS21	0	<table><tr><td>VS21 \ VS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/dot</td><td>2H/dot</td></tr><tr><td>1</td><td>3H/dot</td><td>1H/dot</td></tr></table>	VS21 \ VS20	0	1	0	1H/dot	2H/dot	1	3H/dot	1H/dot	Second line vertical character size
VS21 \ VS20	0	1											
0	1H/dot	2H/dot											
1	3H/dot	1H/dot											
		1											
2	VS20	0											
		1											
1	VS11	0	<table><tr><td>VS11 \ VS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/dot</td><td>2H/dot</td></tr><tr><td>1</td><td>3H/dot</td><td>1H/dot</td></tr></table>	VS11 \ VS10	0	1	0	1H/dot	2H/dot	1	3H/dot	1H/dot	First line vertical character size
VS11 \ VS10	0	1											
0	1H/dot	2H/dot											
1	3H/dot	1H/dot											
		1											
0	VS10	0											
		1											

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	FS	0	Crystal oscillator frequency: 2fsc	
		1	Crystal oscillator frequency: 4fsc	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times \left(2 \sum_{n=0}^5 2^n VP_n \right)$ H: the horizontal synchronization pulse period	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		



Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND3 (Horizontal display start position and horizontal size setup command)

• First byte

DA 0 to 7	Register	Contents			Notes									
		State	Function											
7	—	1	Command 3 identification code. Sets the horizontal display start position and the horizontal character size.											
6	—	0												
5	—	1												
4	—	0												
3	HS21	0	<table><tr><td>HS21 \ HS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/dot</td><td>2Tc/dot</td></tr><tr><td>1</td><td>3Tc/dot</td><td>1Tc/dot</td></tr></table>		HS21 \ HS20	0	1	0	1Tc/dot	2Tc/dot	1	3Tc/dot	1Tc/dot	Second line horizontal character size
		HS21 \ HS20			0	1								
0	1Tc/dot	2Tc/dot												
1	3Tc/dot	1Tc/dot												
1														
2	HS20	0												
		1												
1	HS11	0	<table><tr><td>HS11 \ HS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/dot</td><td>2Tc/dot</td></tr><tr><td>1</td><td>3Tc/dot</td><td>1Tc/dot</td></tr></table>		HS11 \ HS10	0	1	0	1Tc/dot	2Tc/dot	1	3Tc/dot	1Tc/dot	First line horizontal character size
		HS11 \ HS10			0	1								
0	1Tc/dot	2Tc/dot												
1	3Tc/dot	1Tc/dot												
1														
0	HS10	0												
		1												

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	HP5 (MSB)	0	<p>If HS is the horizontal start position then:</p> $HS = T_c \times \left(2 \sum_{n=0}^5 2^n VP_n \right)$ <p>Tc: Period of the oscillator in operating mode.</p>	<p>The horizontal display start position is set by the 6 bits HP0 to HP5. The weight of bit 1 is 2Tc.</p>
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74798/M is reset by the \overline{RST} pin.

COMMAND4 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 4 identification code. Display character data write setup.	
6	—	1		
5	—	1		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be set to 0
		1	Test mode	
2	RAMERS	0		Erasing RAM takes about 500 μ s. (This operation must be executed in the DSPOFF state.)
		1	Erase display RAM. (The RAM data is set to 7F hexadecimal.)	
1	OSCSTP	0	Do not stop the crystal and VCO oscillators	Valid in external synchronization mode when character display is off. It will no longer be possible to detect VPS/PDC data
		1	Stop the crystal and VCO oscillators	
0	SYSRST	0		The registers are reset when the \overline{CS} pin is low, and the reset state is cleared when \overline{CS} is set high
		1	Reset all registers and turn display off	

• Second byte

DA 0 to 7	Register	Contents			Notes										
		State	Function												
7	—	0	Second byte identification bit												
6	BLK2	0	Character display area		Specifies the size for complete fill in										
		1	Video display area												
5	BLK1	0	<table><tr><td>BLK1 \ BLK0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blanking off</td><td>Character size</td></tr><tr><td>1</td><td>Frame size</td><td>Complete fill in size</td></tr></table>		BLK1 \ BLK0	0	1	0	Blanking off	Character size	1	Frame size	Complete fill in size	Changes the blanking size	
		BLK1 \ BLK0			0	1									
0	Blanking off	Character size													
1	Frame size	Complete fill in size													
1															
4	BLK0	0													
		1													
3	BK1	0	Blinking period: About 0.5 s		Switches the blinking period										
		1	Blinking period: About 1.0 s												
2	BK0	0	Blinking off		Blinking in reverse video mode switches the display between normal character display and reverse video display										
		1	Blinking on												
1	RV	0	Reverse video off												
		1	Reverse video on												
0	DSPON	0	Character display off												
		1	Character display on												

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND5 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 5 identification code. Display control setup.	
6	—	1		
5	—	0		
4	—	1		
3	NP1	0	NTSC	Switches between NTSC and PAL
		1	PAL	
2	NP0	0	525 lines	Modified by the external input signal V
		1	625 lines	
1	NON	0	Interlaced	Switches between interlaced and noninterlaced video
		1	Noninterlaced	
0	INT	0	External synchronization	Switches between external and internal synchronization
		1	Internal synchronization	

• Second byte

DA 0 to 7	Register	Contents		Notes																																						
		State	Function																																							
7	—	0	Second byte identification bit																																							
6	RSHLV2	0	Background color level 1 (level that is different from blue)	Switches the background color signal level																																						
		1	Background color level 2 (level that is identical to the blue level)																																							
5	HLFINT	0	Normal mode																																							
		1	Partial internal synchronization mode																																							
4	BCL	0	Background color on	Only valid in internal synchronization mode																																						
		1	No background color (Only the background level is set)																																							
3	CB	0	Color burst signal output	Only valid when BCL is high																																						
		1	Color burst signal output stopped																																							
2	PH2	0	<table><tr><th>PH2</th><th>PH1</th><th>PH0</th><th>Background color (phase)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Cyan*</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Yellow*</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Red*</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Blue*</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Cyan blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Green*</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Orange</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Magenta*</td></tr></table> *: When 2fsc is used.				PH2	PH1	PH0	Background color (phase)	0	0	0	Cyan*	0	0	1	Yellow*	0	1	0	Red*	0	1	1	Blue*	1	0	0	Cyan blue	1	0	1	Green*	1	1	0	Orange	1	1	1	Magenta*
		PH2					PH1	PH0	Background color (phase)																																	
0	0	0					Cyan*																																			
0	0	1					Yellow*																																			
0	1	0					Red*																																			
0	1	1					Blue*																																			
1	0	0					Cyan blue																																			
1	0	1					Green*																																			
1	1	0					Orange																																			
1	1	1					Magenta*																																			
1	1																																									
1	PH1	0																																								
		1																																								
0	PH0	0																																								
		1																																								

*: When 2fsc is used.

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND6 (Synchronizing signal detection setup command)

• First byte

DA 0 to 7	Register	Contents			Notes										
		State	Function												
7	—	1	Command 6 identification code. Sets up synchronizing signal control.												
6	—	1													
5	—	1													
4	—	0													
3	SEL0	0	<table><tr><td>SEL0 \ MOD0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>DAV</td><td>Sliced data width</td></tr><tr><td>1</td><td>CSYNC</td><td>ST.PULSE</td></tr></table>			SEL0 \ MOD0	0	1	0	DAV	Sliced data width	1	CSYNC	ST.PULSE	Switches the SEP _{OUT} (pin 26) output
		SEL0 \ MOD0				0	1								
0	DAV	Sliced data width													
1	CSYNC	ST.PULSE													
1															
2	MOD0	0													
		1													
1	DISLIN	0	12 lines		Switches the number of lines displayed										
		1	10 lines												
0	MUT	0	Normal output			CV _{OUT} switching									
		1	CV _{IN} is cut and CV _{OUT} is held at the pedestal level												

• Second byte

DA 0 to 7	Register	Contents				Notes																															
		State	Function																																		
7	—	0	Second byte identification bit																																		
6	RN2	0	<table><tr><th>RN2</th><th>RN1</th><th>RN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>32 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>4 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>8 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>16 times</td></tr></table>				RN2	RN1	RN0	Number of times HSYNC detected	0	0	0	32 times	0	0	1	4 times	0	1	0	8 times	1	0	0	16 times	<p>External synchronizing signal detection control. Signal absent → signal present transition detection. Sets the sampling period in which SYNC can be detected continuously in the horizontal synchronizing signal period (1H).</p>										
		RN2					RN1	RN0	Number of times HSYNC detected																												
0	0	0	32 times																																		
0	0	1	4 times																																		
0	1	0	8 times																																		
1	0	0	16 times																																		
1																																					
5	RN1	0																																			
		1																																			
4	RN0	0																																			
		1																																			
3	SN3	0	<table><tr><th>SN3</th><th>SN2</th><th>SN1</th><th>SN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Not detected</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>32 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>64 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>128 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>256 times</td></tr></table>				SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	<p>External synchronizing signal detection control. Signal present → signal absent transition detection. Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).</p>
		SN3					SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0	0	Not detected																																	
0	0	0	1	32 times																																	
0	0	1	0	64 times																																	
0	1	0	0	128 times																																	
1	0	0	0	256 times																																	
1																																					
2	SN2	0																																			
		1																																			
1	SN1	0																																			
		1																																			
0	SN0	0																																			
		1																																			

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND7 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	CINSEL	0	Blank area (the logical OR of the character and frame signals)	CV _{CR} on signal switching
		1	Video signal display area	
5	CINCTL	0	CV _{CR} : off	CV _{CR} on/off switching
		1	CV _{CR} : on	
4	VNPSEL	0	V falling edge detection	Switches the V acquisition polarity in external mode when internal V separation is used
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 μ s (for NTSC)	Switches the internal V separation period
		1	VSEP: about 17.8 μ s (for NTSC)	
2	MSKERS	0	Mask valid	Clears the HSYNC and VSYNC masks
		1	Mask invalid	
1	MSKSEL	0	3H (NTSC)	Switches the VSYNC mask
		1	20H (NTSC)	
0	EGL	0	Frame level 0 only (V _{BK0})	Switches the frame level. (Only valid when BLK0 is 0 and BLK1 is 1.)
		1	Two-stage frame level (V _{BK0} and V _{BK1})	

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND8 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	0		
1	—	0		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents					Notes	
		State	Function					
7	—	0	Second byte identification bit					
6	LNA3	0	LNA3	LNA2	LNA1	LNA0	Specified line	Specifies the line whose background is to be changed. (This specification is illegal for the same line as LNA*, LNB*, and LNC*)
		1	0	0	0	0	Do not change the line background	
5	LNA2	0	0	0	0	1	Line 1	
			0	0	1	0	Line 2	
		1	0	0	1	1	Line 3	
			0	1	0	0	Line 4	
4	LNA1	0	0	1	0	1	Line 5	
			0	1	1	0	Line 6	
		1	0	1	1	1	Line 7	
			1	0	0	0	Line 8	
3	LNA0	0	1	0	0	1	Line 9	
			1	0	1	0	Line 10	
		1	1	0	1	1	Line 11	
			1	1	—	—	Line 12	
2	LPA2	0	LPA2	LPA1	LPA0	Background color (phase)	Specifies the background color	
		1	0	0	0	Cyan*		
1	LPA1	0	0	0	1	Yellow*		
			0	1	0	Red*		
		1	0	1	1	Blue*		
			1	0	0	Cyan blue		
0	LNA0	0	1	0	1	Green*		
			1	1	0	Orange		
		1	1	1	1	Magenta*		
			*: When 2fsc is used.					

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND9 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 2 identification code	
2	—	0		
1	—	1		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents				Notes		
		State	Function					
7	—	0	Second byte identification bit					
6	LNB3	0	LNB3	LNB2	LNB1	LNB0	Specified line	Specifies the line whose background is to be changed. (This specification is illegal for the same line as LNA*, LNB*, and LNC*)
		1	0	0	0	0	Do not change the line background	
5	LNB2	0	0	0	0	1	Line 1	
			0	0	1	0	Line 2	
		1	0	0	1	1	Line 3	
			0	1	0	0	Line 4	
4	LNB1	0	0	1	0	1	Line 5	
			0	1	1	0	Line 6	
		1	0	1	1	1	Line 7	
			1	0	0	0	Line 8	
3	LNB0	0	1	0	0	1	Line 9	
			1	0	1	0	Line 10	
		1	1	0	1	1	Line 11	
			1	1	—	—	Line 12	
2	LPB2	0	LPB2	LPB1	LPB0	Background color (phase)		Specifies the background color
		1	0	0	0	Cyan*		
1	LPB1	0	0	0	1	Yellow*		
			0	1	0	Red*		
		1	0	1	1	Blue*		
			1	0	0	Cyan blue		
0	LNB0	0	1	0	1	Green*		
			1	1	0	Orange		
		1	1	1	1	Magenta*		
			*: When 2fsc is used.					

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND10 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 3 identification code	
2	—	0		
1	—	1		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents					Notes	
		State	Function					
7	—	0	Second byte identification bit					
6	LNC3	0	LNC3	LNC2	LNC1	LNC0	Specified line	Specifies the line whose background is to be changed. (This specification is illegal for the same line as LNA*, LNB*, and LNC*)
		1	0	0	0	0	Do not change the line background	
5	LNC2	0	0	0	0	1	Line 1	
			0	0	1	0	Line 2	
		1	0	0	1	1	Line 3	
			0	1	0	0	Line 4	
4	LNC1	0	0	1	0	1	Line 5	
			0	1	1	0	Line 6	
		1	0	1	1	1	Line 7	
			1	0	0	0	Line 8	
3	LNC0	0	1	0	0	1	Line 9	
			1	0	1	0	Line 10	
		1	1	0	1	1	Line 11	
			1	1	—	—	Line 12	
2	LPC2	0	LPC2	LPC1	LPC0	Background color (phase)	Specifies the background color	
		1	0	0	0	Cyan*		
1	LPC1	0	0	0	1	Yellow*		
			0	1	0	Red*		
		1	0	1	1	Blue*		
			1	0	0	Cyan blue		
0	LNC0	0	1	0	1	Green*		
			1	1	0	Orange		
		1	1	1	1	Magenta*		
			*: When 2fsc is used.					

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND11 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 4 identification code	
2	—	1		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	VSPDCK	0	Character display VCO operating	Character display VCO control
		1	Character display VCO stopped	
4	VSPSLC	0	Data slice VCO operating	Data slice VCO control
		1	Data slice VCO stopped	
3	LNCSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNB* for characters specified for RV display
		1	RV characters have the background color specified by PH* and the RV character background color is white	
2	MOD3	0	The LNCSEL = 1 setting specifications	Valid when LNCSEL is high
		1	RV characters have the background color specified by PH* and characters are white	
1	LNBSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNB* for characters specified for RV display
		1	RV characters have the background color specified by PH* and the RV character background color is white.	
0	MOD2	0	The LNBSEL = 1 setting specifications	Valid when LNBSEL is high
		1	RV characters have the background color specified by PH* and characters are white	

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND12 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 5 identification code	
2	—	1		
1	—	0		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents				Notes																																	
		State	Function																																				
7	—	0	Second byte identification bit																																				
6	VINNP	0	Negative CSYNC input polarity			CSYNC input polarity selection																																	
		1	Positive CSYNC input polarity																																				
5	VIN2	0	Normal input			SEP _{IN} pin input switching																																	
		1	CSYNC input to the SEP _{IN} pin																																				
4	SEL22	0	<table><tr><th>SEL22</th><th>SEL2</th><th>HLFTOM</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>0</td><td>SYNC_{JDG}</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Halftone</td></tr><tr><td>0</td><td>1</td><td>0</td><td>O/E</td></tr><tr><td>0</td><td>1</td><td>1</td><td>LOCK</td></tr><tr><td>1</td><td>0</td><td>0</td><td>SYNDET2</td></tr><tr><td>1</td><td>0</td><td>1</td><td>SENDET</td></tr><tr><td>1</td><td>1</td><td>0</td><td>LOCK2</td></tr></table>				SEL22	SEL2	HLFTOM	Output	0	0	0	SYNC _{JDG}	0	0	1	Halftone	0	1	0	O/E	0	1	1	LOCK	1	0	0	SYNDET2	1	0	1	SENDET	1	1	0	LOCK2	SYNC _{JDG} pin (pin 8) output switching. The halftone output line specification depends on background color specification (the logical or of the 3-line specification) SYNDET2: Used for character display LOCK2: Used for character display
SEL22	SEL2	HLFTOM					Output																																
0	0	0					SYNC _{JDG}																																
0	0	1					Halftone																																
0	1	0					O/E																																
0	1	1					LOCK																																
1	0	0					SYNDET2																																
1	0	1					SENDET																																
1	1	0					LOCK2																																
3	HLFTON	0																																					
		1																																					
2	SEL2	0																																					
		1																																					
1	SEL1	0	Vertical synchronization signal input (external synchronization)			SEP _{IN} (pin 27) input switching. Only valid when CTL3 is high.																																	
		1	Frame signal input																																				
0	CTL3	0	Internal V separation used			V separation switching																																	
		1	Internal V separation not used (external V separation)																																				

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND13 (VPS/PDC control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 6 identification code	
2	—	1		
1	—	1		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes																																																																											
		State	Function																																																																												
7	—	0	Second byte identification bit																																																																												
6	CPA1	0	<table><tr><td>CPA1</td><td>CPA0</td><td>Clock</td></tr><tr><td>0</td><td>0</td><td>No.4</td></tr><tr><td>0</td><td>1</td><td>No.3</td></tr><tr><td>1</td><td>0</td><td>No.2</td></tr><tr><td>1</td><td>1</td><td>No.1</td></tr></table>	CPA1	CPA0	Clock	0	0	No.4	0	1	No.3	1	0	No.2	1	1	No.1	Data acquisition clock switching																																																												
CPA1	CPA0	Clock																																																																													
0	0	No.4																																																																													
0	1	No.3																																																																													
1	0	No.2																																																																													
1	1	No.1																																																																													
	1																																																																														
5	CPA0	0																																																																													
	1																																																																														
4	—	0																																																																													
3	VPM3	0	<table><tr><td>VPM3</td><td>VPM2</td><td>VPM1</td><td>VPM0</td><td>Operating mode</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>VPS</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8/30/2 (PDC)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Automatic PDC/VPS switching</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8/30/1 (UDT)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Header time 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Header time 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Header time 3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Header time 4</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Status display 1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Status display 2</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Status display 3</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Status display 4</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>PAL Pulse</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Automatic PDC/VPS switching 2</td></tr></table>	VPM3	VPM2	VPM1	VPM0	Operating mode	0	0	0	0	VPS	0	0	0	1	8/30/2 (PDC)	0	0	1	0	Automatic PDC/VPS switching	0	0	1	1	8/30/1 (UDT)	0	1	0	0	Header time 1	0	1	0	1	Header time 2	0	1	1	0	Header time 3	0	1	1	1	Header time 4	1	0	0	0	Status display 1	1	0	0	1	Status display 2	1	0	1	0	Status display 3	1	0	1	1	Status display 4	1	1	0	0	PAL Pulse	1	1	0	1	Automatic PDC/VPS switching 2	
VPM3	VPM2	VPM1		VPM0	Operating mode																																																																										
0	0	0		0	VPS																																																																										
0	0	0		1	8/30/2 (PDC)																																																																										
0	0	1		0	Automatic PDC/VPS switching																																																																										
0	0	1		1	8/30/1 (UDT)																																																																										
0	1	0		0	Header time 1																																																																										
0	1	0		1	Header time 2																																																																										
0	1	1		0	Header time 3																																																																										
0	1	1		1	Header time 4																																																																										
1	0	0		0	Status display 1																																																																										
1	0	0		1	Status display 2																																																																										
1	0	1		0	Status display 3																																																																										
1	0	1		1	Status display 4																																																																										
1	1	0		0	PAL Pulse																																																																										
1	1	0		1	Automatic PDC/VPS switching 2																																																																										
	1																																																																														
2	VPM2	0																																																																													
	1																																																																														
1	VPM1	0																																																																													
	1																																																																														
0	VPM0	0																																																																													
	1																																																																														

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND14 (VPS/PDC control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 7 identification code	
2	—	1		
1	—	1		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	VMWSE2	0	V mask period start - From the retrace period	CPOUT pin (pin 13) V mask period switching 2
		1	V mask period start - From 10H before the retrace period	
5	VMWSEL	0	The V mask period is the retrace period	CPOUT pin (pin 13) V mask period switching
		1	The V mask period is 9H	
4	HBS2	0	Discrimination mode 1	Clock line
		1	Discrimination mode 2	
3	HBS1	0	Discrimination mode 1	Framing code
		1	Discrimination mode 2	
2	BMS	0	Error check valid (Error checking can be turned on or off on a per-byte basis.)	When set to 0, if there are no errors in bytes for which error checking is turned on, those bytes are written to P-S. When set to 1, all bytes are written to P-S regardless of the error status.
		1	Error check invalid (Applications can select whether data for which an error is detected is held or writing on a per-byte basis.)	
1	EMS	0	Data hold	Specifies handling of bytes for which error checking is set to off but in which an error occurred when error checking is turned on.
		1	Data write (When the error bit is 0 in VPS mode.)	
0	DCE	0	Error checking enabled for unused data bytes. VPS: bytes 3, 4, and 6 to 10, PDCC (8/30/2): bytes 7 to 12, header 1: bytes 14 to 37, header 2: bytes 14 to 29, header 3: bytes 14 to 21, status 1 (3): bytes 7 to 25, status 2 (4): bytes 7 to 35	Error checking setting for unused data bytes. Biphase (VPS), Hamming (PDC), and odd parity (header).
		1	Error checking disabled for unused data bytes. VPS: bytes 3, 4, and 6 to 10, PDCC (8/30/2): bytes 7 to 12, header 1: bytes 14 to 37, header 2: bytes 14 to 29, header 3: bytes 14 to 21, status 1 (3): bytes 7 to 25, status 2 (4): bytes 7 to 35	

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND15 (VPS/PDC control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 8 identification code	
2	—	0		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	ECV15	0	Byte 15 biphas error check on (Data hold)	Specification when the VPS data BMS bit is 0. The item in parentheses is the specification when the VPS data BMS bit is 1.
		1	Byte 15 biphas error check off (Data write)	
4	ECV14	0	Byte 14 biphas error check on (Data hold)	
		1	Byte 14 biphas error check off (Data write)	
3	ECV13	0	Byte 13 biphas error check on (Data hold)	
		1	Byte 13 biphas error check off (Data write)	
2	ECV12	0	Byte 12 biphas error check on (Data hold)	
		1	Byte 12 biphas error check off (Data write)	
1	ECV11	0	Byte 11 biphas error check on (Data hold)	
		1	Byte 11 biphas error check off (Data write)	
0	ECV5	0	Byte 5 biphas error check on (Data hold)	
		1	Byte 5 biphas error check off (Data write)	

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND16 (VPS/PDC control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 9 identification code	
2	—	0		
1	—	0		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	ECP19	0	Byte 19 Hamming error check on (Data hold) {Bytes 44, 28, 36, 20, 32, 42, 32, and 42}	Specification when the PDC data (8/30/2) BMS bit is 0. The item in parentheses is the specification when the BMS bit is 1. The item in curl braces lists the odd parity check on/off bytes for header modes 1, 2, 3, and 4 and status mode 1, 2, 3, and 4.
		1	Byte 19 Hamming error check off (Data write) {Bytes 44, 28, 36, 20, 32, 42, 32, and 42}	
5	ECP18	0	Byte 18 Hamming error check on (Data hold) {Bytes 43, 27, 35, 19, 31, 41, 31, and 41}	
		1	Byte 18 Hamming error check off (Data write) {Bytes 43, 27, 35, 19, 31, 41, 31, and 41}	
4	ECP17	0	Byte 17 Hamming error check on (Data hold) {Bytes 42, 26, 34, 18, 30, 40, 30, and 40}	
		1	Byte 17 Hamming error check off (Data write) {Bytes 42, 26, 34, 18, 30, 40, 30, and 40}	
3	ECP16	0	Byte 16 Hamming error check on (Data hold) {Bytes 41, 25, 33, 17, 29, 39, 29, and 39}	
		1	Byte 16 Hamming error check off (Data write) {Bytes 41, 25, 33, 17, 29, 39, 29, and 39}	
2	ECP15	0	Byte 15 Hamming error check on (Data hold) {Bytes 40, 24, 32, 16, 28, 38, 28, and 38}	
		1	Byte 15 Hamming error check off (Data write) {Bytes 40, 24, 32, 16, 28, 38, 28, and 38}	
1	ECP14	0	Byte 14 Hamming error check on (Data hold) {Bytes 39, 23, 31, 15, 27, 37, 27, and 37}	
		1	Byte 14 Hamming error check off (Data write) {Bytes 39, 23, 31, 15, 27, 37, 27, and 37}	
0	ECP13	0	Byte 13 Hamming error check on (Data hold) {Bytes 38, 22, 30, 14, 26, 36, 26, and 36}	
		1	Byte 13 Hamming error check off (Data write) {Bytes 38, 22, 30, 14, 26, 36, 26, and 36}	

Note: All registers are set to 0 when the LC74798/M is reset by the RST pin.

COMMAND17 (VPS/PDC control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command A identification code	
2	—	0		
1	—	1		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	ECP25	0	Byte 25 Hamming error check on (Data hold)	Specification when the PDC data (8/30/2) BMS bit is 0. The item in parentheses is the specification when the BMS bit is 1. The item in curly braces lists the odd parity check off bytes for header modes 1, 2, 3, and 4 and status mode 1, 2, 3, and 4.
		1	Byte 25 Hamming error check off (Data write)	
4	ECP24	0	Byte 24 Hamming error check on (Data hold)	
		1	Byte 24 Hamming error check off (Data write)	
3	ECP23	0	Byte 23 Hamming error check on (Data hold)	
		1	Byte 23 Hamming error check off (Data write)	
2	ECP22	0	Byte 22 Hamming error check on (Data hold) {Bytes -, -, -, -, 35, 45, 35, and 45}	
		1	Byte 22 Hamming error check off (Data write) {Bytes -, -, -, -, 35, 45, 35, and 45}	
1	ECP21	0	Byte 21 Hamming error check on (Data hold) {Bytes -, -, -, -, 34, 44, 34, and 44}	
		1	Byte 21 Hamming error check off (Data write) {Bytes -, -, -, -, 34, 44, 34, and 44}	
0	ECP20	0	Byte 20 Hamming error check on (Data hold) {Bytes 45, 29, 37, 21, 33, 43, 33, and 43}	
		1	Byte 20 Hamming error check off (Data write) {Bytes 45, 29, 37, 21, 33, 43, 33, and 43}	

Note: All registers are set to 0 when the LC74798/M is reset by the $\overline{\text{RST}}$ pin.

PDC/VPS Output Data Format

Data is output in order starting with bit 7 of byte 1.

Output data		PDC 8/30 mode				VPS mode	Header time mode 1 (3)		Header time mode 2 (4)		
		Format 1		Format 2							
Data update bits *: Set to 0 when data is updated, and set to 1 when not updated.											
Byte 1	Bit 7	byte 15	bit 0	byte 16	bit 0	byte 11	bit 0	byte 38	bit 0	byte 22	bit 0
	6		1		1		1	(30)	1	(14)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 17	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 2	Bit 7	byte 16	bit 0	byte 18	bit 0	byte 12	bit 0	byte 39	bit 0	byte 23	bit 0
	6		1		1		1	(31)	1	(15)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 19	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 3	Bit 7	byte 17	bit 0	byte 20	bit 0	byte 13	bit 0	byte 40	bit 0	byte 24	bit 0
	6		1		1		1	(32)	1	(16)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 21	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 4	Bit 7	byte 18	bit 0	byte 22	bit 0	byte 14	bit 0	byte 41	bit 0	byte 25	bit 0
	6		1		1		1	(33)	1	(17)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 23	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 5	Bit 7	byte 19	bit 0	byte 14	bit 0	byte 5	bit 0	byte 42	bit 0	byte 26	bit 0
	6		1		1		1	(34)	1	(18)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 15	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 6	Bit 7	byte 20	bit 0	byte 24	bit 0	byte 15	bit 0	byte 43	bit 0	byte 27	bit 0
	6		1		1		1	(35)	1	(19)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 25	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7

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Output data		PDC 8/30 mode				VPS mode	Header time mode 1 (3)		Header time mode 2 (4)		
		Format 1		Format 2							
Byte 7	Bit 7	byte 21	bit 0	byte 13	bit 0	1		byte 44	bit 0	byte 28	bit 0
	6		1		1	1		(36)	1	(20)	1
	5		2		2	1			2		2
	4		3		3	1			3		3
	3		4	1		1			4		4
	2		5	1		1			5		5
	1		6	1		1			6		6
	0		7	1		1			7		7
Byte 8	Bit 7	byte 13	bit 0	Error	byte 16	Error	byte 11	byte 45	bit 0	byte 29	bit 0
	6		1	information 1	17	information 1	12	(37)	1	(21)	1
	5		2		18		13		2		2
	4		3		19		14		3		3
	3		4		20		5		4		4
	2		5		21		15		5		5
	1		6		22	0			6		6
	0		7		23	0			7		7
Byte 9	Bit 7	byte 14	bit 0	Error	14			Error	byte 38 (30)	Error	byte 22 (14)
	6		1	information 2	15			information 2	39 (31)	information 2	23 (15)
	5		2		24				40 (32)		24 (16)
	4		3		25				41 (33)		25 (17)
	3		4		13				42 (34)		26 (18)
	2		5	0					43 (35)		27 (19)
	1		6	0					44 (36)		28 (20)
	0		7	0					45 (37)		29 (21)
Byte 10	Bit 7	byte 22	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								
Byte 11	Bit 7	byte 23	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								
Byte 12	Bit 7	byte 24	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								
Byte 13	Bit 7	byte 25	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								

Bits for which data is not set are set to 1.

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Data is output in order starting with bit 7 of byte 1.

1, 2 : 8/30/2 3, 4 : 8/30/1

Output data		Status display mode 1 (3)		Status display mode 2 (4)		PAL Puls
Data update bits *: Set to 0 when data is updated.						
Byte 1	Bit 7	byte 26	bit 0	byte 36	bit 0	bit 0
	6	(26)	1	(36)	1	1
	5		2		2	2
	4		3		3	3
	3		4		4	4
	2		5		5	5
	1		6		6	6
	0		7		7	7
Byte 2	Bit 7	byte 27	bit 0	byte 37	bit 0	bit 8
	6	(27)	1	(37)	1	9
	5		2		2	10
	4		3		3	11
	3		4		4	12
	2		5		5	13
	1		6		6	0
	0		7		7	0
Byte 3	Bit 7	byte 28	bit 0	byte 38	bit 0	
	6	(28)	1	(38)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 4	Bit 7	byte 29	bit 0	byte 39	bit 0	
	6	(29)	1	(39)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 5	Bit 7	byte 30	bit 0	byte 40	bit 0	
	6	(30)	1	(40)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 6	Bit 7	byte 31	bit 0	byte 41	bit 0	
	6	(31)	1	(41)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 7	Bit 7	byte 32	bit 0	byte 42	bit 0	
	6	(32)	1	(42)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	

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Continued from preceding page.

Output data		Status display mode 1 (3)		Status display mode 2 (4)		PAL Puls
Byte 8	Bit 7	byte 33	bit 0	byte 43	bit 0	
	6	(33)	1	(43)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 9	Bit 7	byte 34	bit 0	byte 44	bit 0	
	6	(34)	1	(44)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 10	Bit 7	byte 35	bit 0	byte 45	bit 0	
	6	(35)	1	(45)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 11	Bit 7	Error	byte 26 (26)	Error	byte 36 (36)	
	6	information 1	27 (27)	information 1	37 (37)	
	5		28 (28)		38 (38)	
	4		29 (29)		39 (39)	
	3		30 (30)		40 (40)	
	2		31 (31)		41 (41)	
	1		32 (32)		42 (42)	
	0		33 (33)		43 (43)	
Byte 12	Bit 7	Error	byte 34 (34)	Error	byte 44 (44)	
	6	information 2	35 (35)	information 2	45 (45)	
	5		0		0	
	4		0		0	
	3		0		0	
	2		0		0	
	1		0		0	
	0		0		0	
Byte 13	Bit 7					
	6					
	5					
	4					
	3					
	2					
	1					
	0					

Display Screen Structure

The display consists of 12 lines of 24 characters.

Up to 288 characters can be displayed.

The number of characters that can be displayed is reduced from the 288 maximum when enlarged characters are displayed.

Display memory addresses are specified as row (0 to B hexadecimal) and column (0 to 17 hexadecimal) addresses.

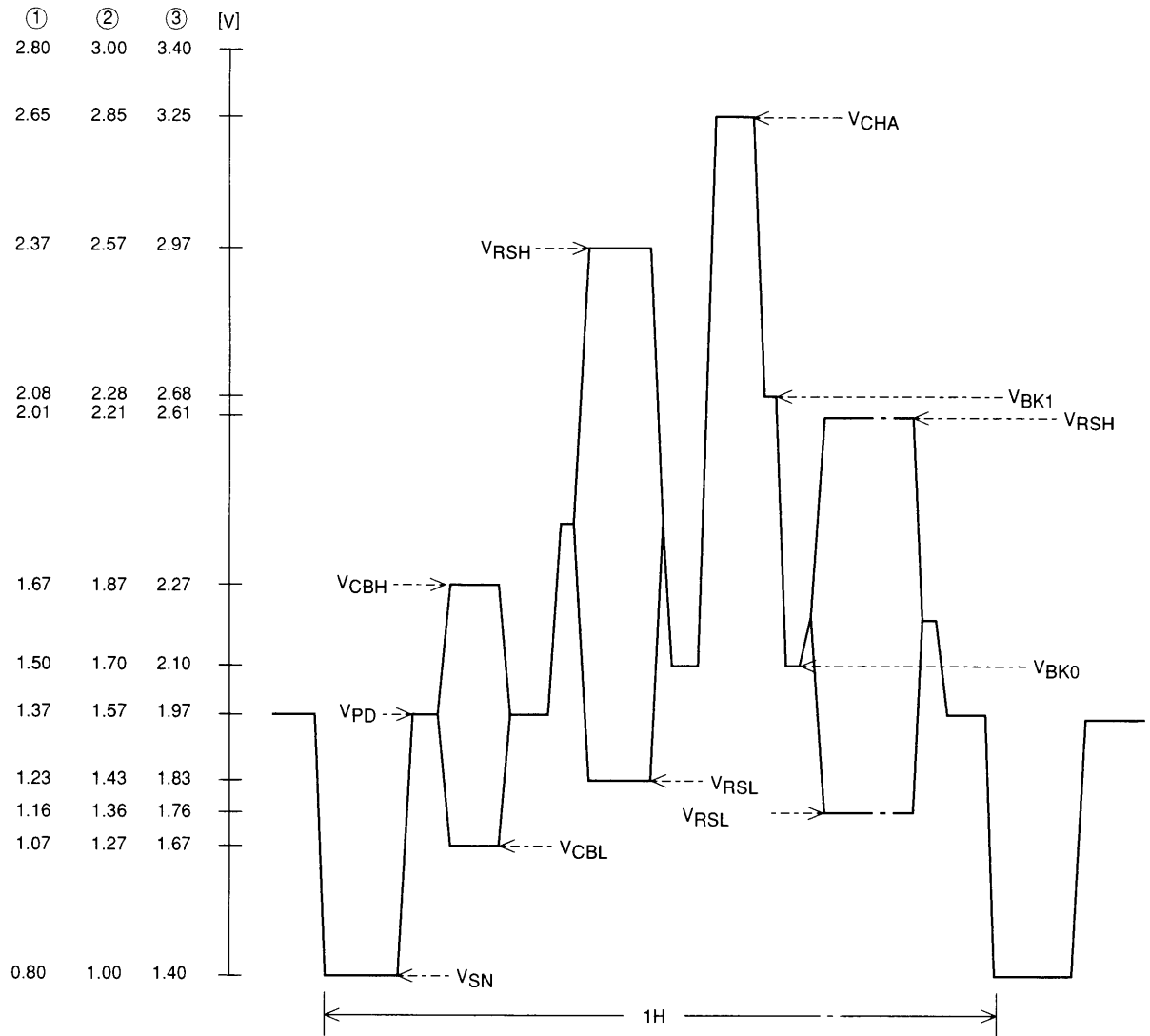
Display Screen Structure (display memory addresses)

← 24 Characters →																									
	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
0																									0
1																									1
2																									2
3																									3
4																									4
5																									5
6																									6
7																									7
8																									8
9																									9
10																									A
11																									B HEX
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	HEX

A10293

Composite Video Signal Output Levels (internally generated levels)

CV_{OUT} output level waveform (V_{DD2} = 5.00 V)



A10234

Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V _{CHA} : Character	2.65	2.85	3.25
V _{RSH} : Background color high	2.37 (2.01)	2.57 (2.21)	2.97 (2.61)
V _{CBH} : Color burst high	1.67	1.87	2.27
V _{RSL} : Background color low	1.23 (1.16)	1.43 (1.36)	1.83 (1.76)
V _{BK1} : Frame	2.08	2.28	2.68
V _{BK0} : Frame	1.50	1.70	2.10
V _{PD} : Pedestal	1.37	1.57	1.97
V _{CBL} : Color burst low	1.07	1.27	1.67
V _{SN} : Sync	0.80	1.00	1.40

Note: V_{DD2} = 5.00V. The values in parentheses for V_{RSH} and V_{RSL} are the values for a blue background.

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