

SANYO

No.3183A

LC7935ANGeneral-Purpose 32-Bit Shift Register
Latch Driver**Features**

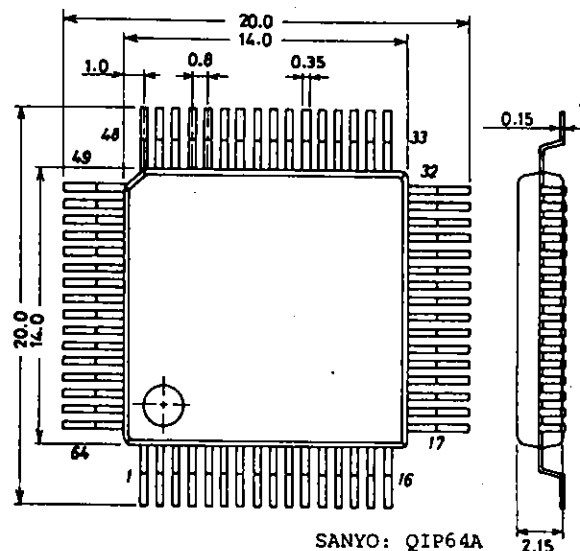
- High-speed, high-voltage silicon gate CMOS device
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock (CLOCK).
- 32-bit latch data is changed on the negative transition of the $\overline{\text{LATCH}}$ pad and is held on the positive transition.
- The $\overline{\text{STROBE}}$ pad, BEO pad can be used to exercise on/off control of the output driver.
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads)
- Maximum ratings of driver output : $V_O = 28\text{V}$, $I_{OL} = 30\text{mA}$
- Logic unit operating voltage : $V_{DD} = 4.5$ to 5.5V

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

				unit
Maximum Supply Voltage	V_{DD}		-0.3 to $+7.0$	V
Input Voltage	V_I		-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{O(1)}$	S_{OUT} output	-0.3 to $V_{DD} + 0.3$	V
	$V_{O(2)}$	D1 to D32 output, output Tr off	28	V
Output Current	I_O	D1 to D32 output, per output	30	mA
Allowable Power Dissipation	$P_d \text{ max}$	$T_a = 70^\circ\text{C}$	450	mW
Operating Temperature	T_{opr}		-10 to $+70$	$^\circ\text{C}$
Storage Temperature	T_{stg}		-35 to $+125$	$^\circ\text{C}$

Package Dimensions 3057

(unit : mm)



SANYO: QIP64A

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

LC7935AN

Allowable Operating Conditions at Ta = -10 to +70°C

	Pin Name	min	typ	max	unit
Supply Voltage	V _{DD}	4.5		5.5	V
'H'-Level Input Voltage	V _{IH}	0.8V _{DD}		V _{DD}	V
'L'-Level Input Voltage	V _{IL}	V _{SS} (L)	0.2V _{DD}		V
Clock Frequency	f _{CLK}			5.0	MHz
Clock Pulse Width	t _W	75			ns
Clock Rise/Fall Time	t _r , t _f			200	ns
Data Setup Time	t _{DS}	100			ns
Data Hold Time	t _{DH}	50			ns
Latch Pulse Width	t _{WL}	100			ns

Electrical Characteristics at Ta = 25°C

	Pin Name	min	typ	max	unit
'H'-Level Input Current	I _{IH} (1)			10	μA
	I _{IH} (2)	12		72	μA
'L'-Level Input Current	I _{IL} (1)	-10			μA
	I _{IL} (2)	-72		-12	μA
'H'-Level Output Voltage	V _{OH}	V _{DD} = 5V, I _{OH} = -0.5mA			V
'L'-Level Output Voltage	V _{OL} (1)	V _{DD} = 5V, I _{OL} = 0.5mA			0.5 V
	V _{OL} (2)	V _{DD} = 5V, I _{OL} = 30mA			0.5 V
Output OFF-State Leakage Current	I _{OFF}	D1 to D32 V _O = 24V			20 μA
Input Capacitance	C _{IN}	CLOCK	5.0		pF
Operating Current Dissipation	I _{DD}	V _{DD}	V _{DD} = 5V, f _{CLK} = 5MHz, all outputs : no load		5 mA

Switching Characteristics at Ta = 25°C

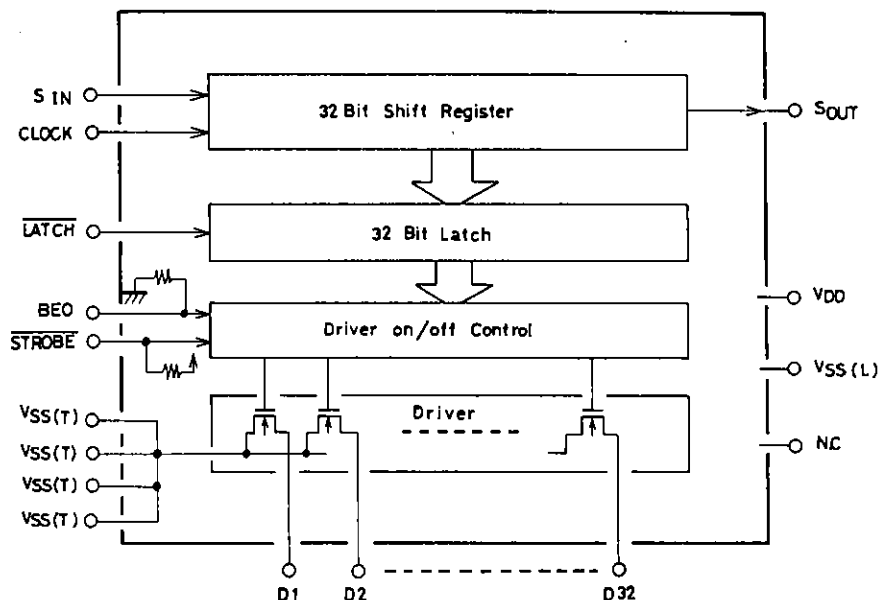
	Pin Name	min	typ	max	unit
Clock Latch Delay Width	t _{CL}	100			ns
Latch Clock Delay Width	t _{LC}	0			ns
'H'-Level Output Propagation Delay Time	t _{PLH} (1)	V _{DD} = 5V, Dn: R _L = 1.0kΩ, C _L = 15pF			400 ns
	t _{PLH} (2)	V _{DD} = 5V, Dn: R _L = 1.0kΩ, C _L = 15pF			300 ns
	t _{PLH} (3)	V _{DD} = 5V, S _{OUT} : C _L = 15pF			200 ns
'L'-Level Output Propagation Delay Time	t _{PHL} (1)	V _{DD} = 5V, Dn: R _L = 1.0kΩ, C _L = 15pF			200 ns
	t _{PHL} (2)	V _{DD} = 5V, Dn: R _L = 1.0kΩ, C _L = 15pF			100 ns
	t _{PHL} (3)	V _{DD} = 5V, S _{OUT} : C _L = 15pF			200 ns

Driver ON/OFF Truth Table

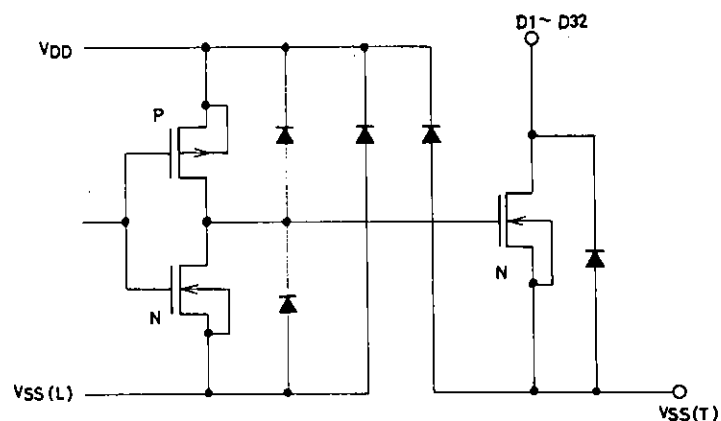
Latch Data (Q)	BEO	STROBE	Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Driver on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

LC7935AN

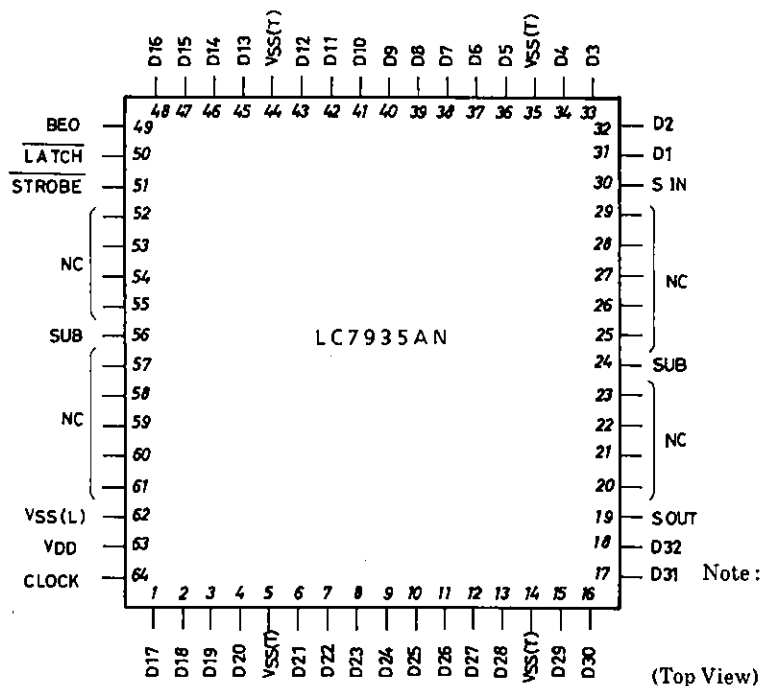
Equivalent Circuit Block Diagram



Output Driver Section Equivalent Circuit

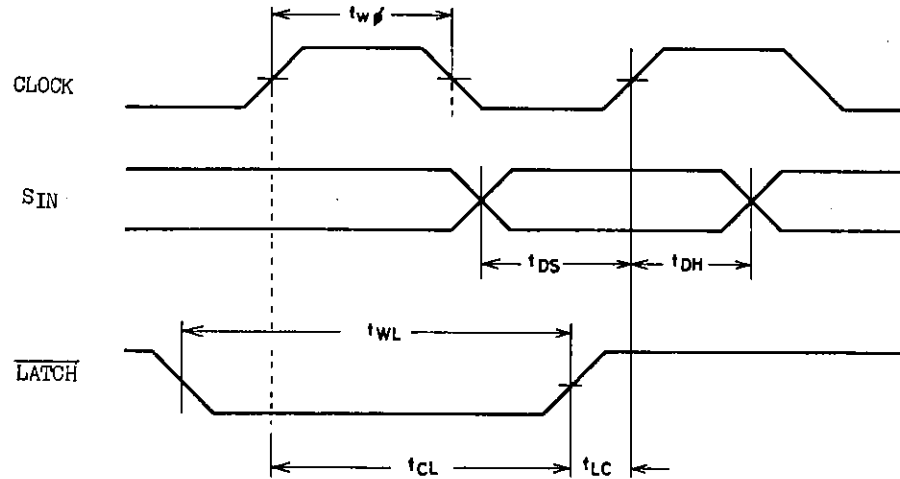


Pin Assignment

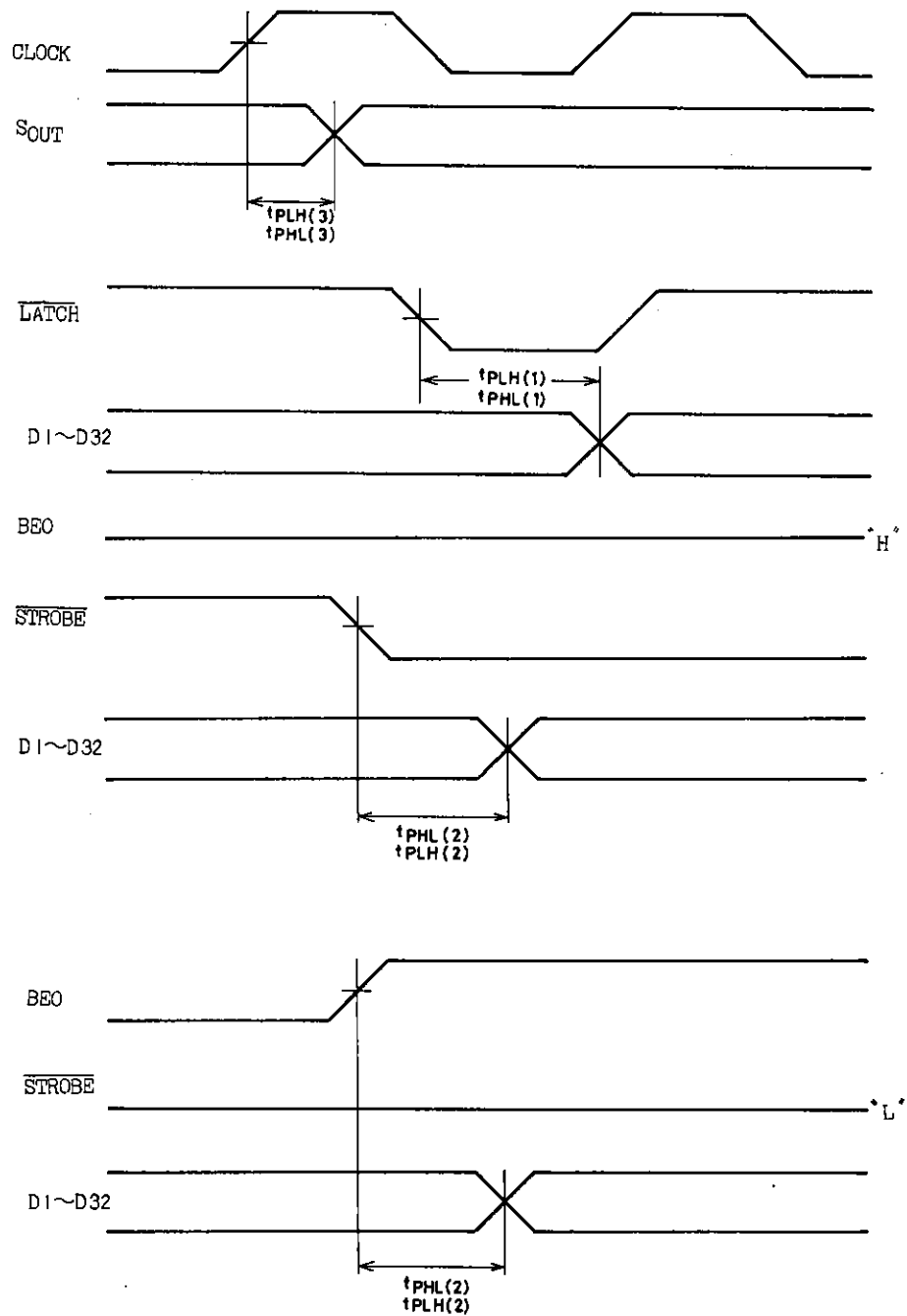


Note: SUB pin and NC pin must be kept open. [SUB pin is connected to the substrate (V_{DD}).]

Input Data Timing Chart



Output Data Timing Chart



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of June, 1995. Specifications and information herein are subject to change without notice.