

SANYO

No. 4348

LC79430D**Dot Matrix LCD Driver**

Overview

The LC79430D is a large-scale dot matrix LCD common driver LSI. The LC79430D contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79430D can be used in conjunction with segment driver LC79400D, LC79401D (QIP100D) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support further increases in bit number
- Supports externally supplied bias voltage
- On-chip 80-bit bidirectional shift register (supports 40-bit x 2 division)
- Supports single mode (80-bit shift register) and dual mode (40-bit x 2 shift register) applications

- | | |
|----------------------------|---------------|
| (1) O1 → O80 | } Single mode |
| (2) O80 → O1 | |
| (3) O1 → O40 and O41 → O80 | } Dual mode |
| (4) O80 → O41 and O40 → O1 | |

All four of the shift direction selections listed above all supported.

- Operating power supply voltage/operating temperature include

V_{DD} (logic section) : 5 V $\pm 10\%$ / -20 to +75 °C

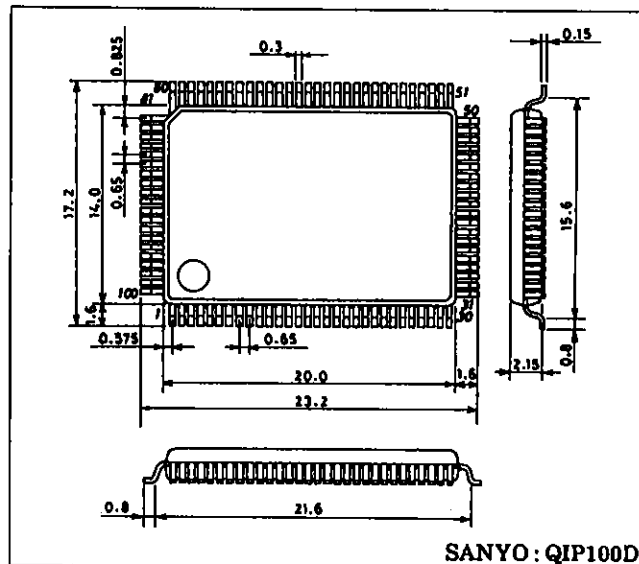
$V_{DD}-V_{EE}$ (LCD section) : 12 V to 32 V / -20 to +75°C

- CMOS process

Package Dimensions

unit : mm

3180-QIP100D



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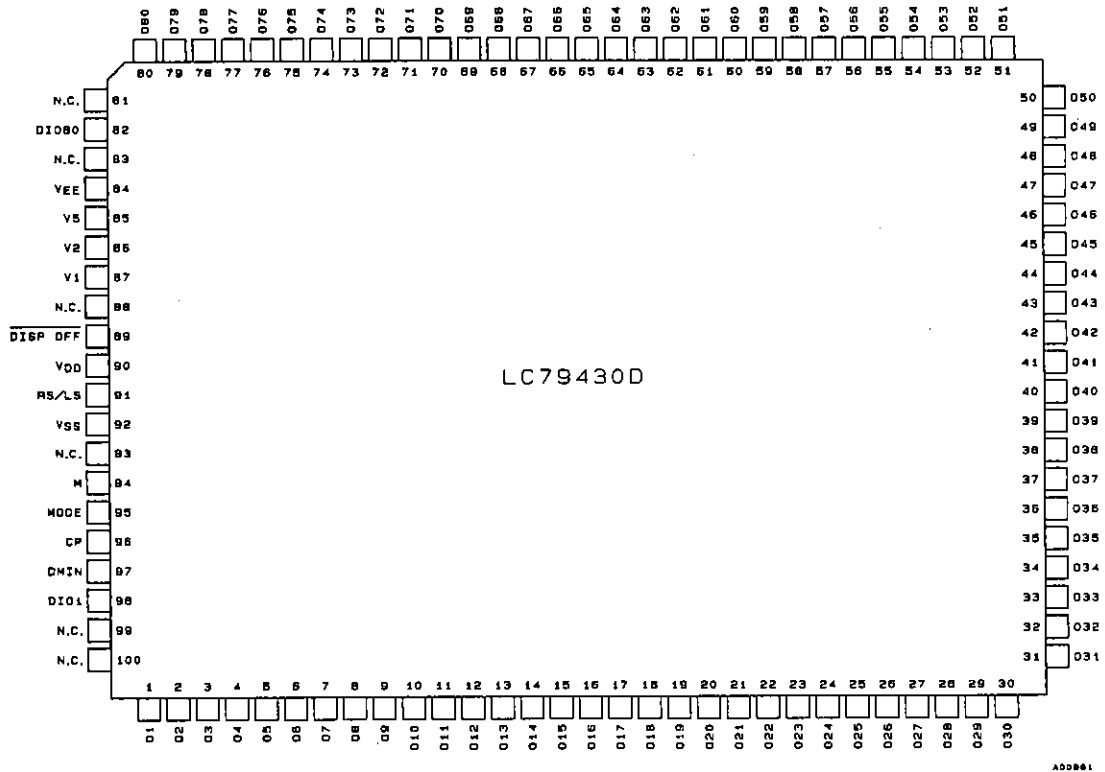
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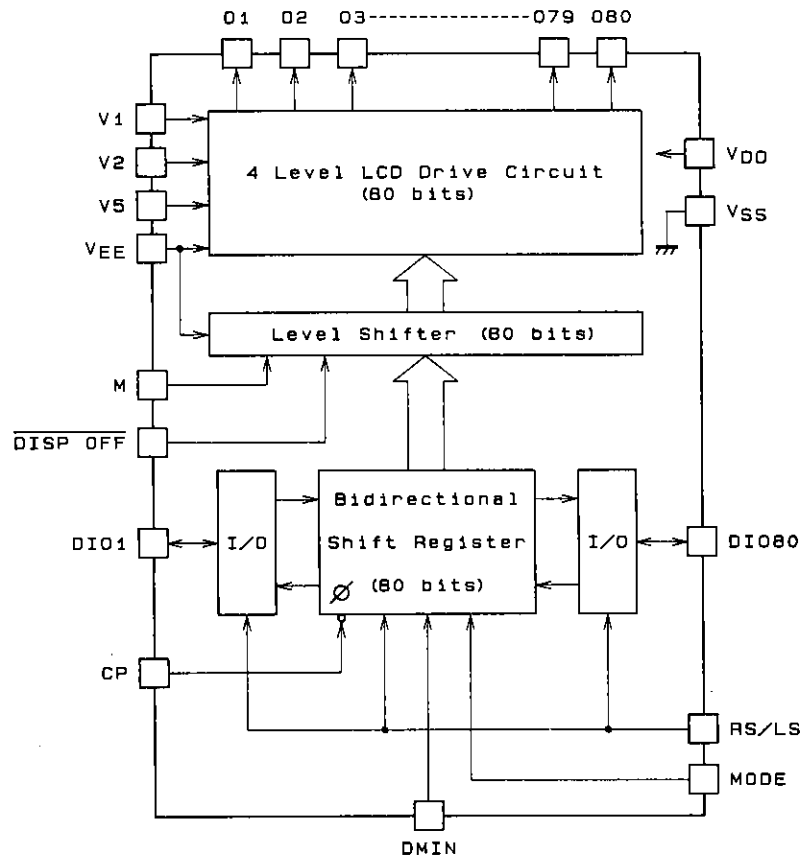
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

LC79430D

Pin Assignment



Equivalent Circuit Block Diagram



Pin Descriptions

Pin No	Pin name	Input/Output	Functions																														
90	V _{DD}	Power supply	V _{DD} and V _{SS} : Power supply for logic section																														
92	V _{SS}																																
84	V _{EE}		V _{DD} and V _{EE} : Power supply for LCD drive circuit																														
87	V1	Power supply	Power supply for LCD drive level																														
86	V2		V1 and V _{EE} : Select level																														
85	V5		V2 and V5 : Non-select level																														
96	CP	Input	Bidirectional shift register shift clock (triggering on the trailing edge)																														
98	DIO1	Input/Output	<table><tr><th>MODE</th><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO80</th><th>DMIN</th></tr><tr><td rowspan="2">L (Single)</td><td>L (Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td><td>*</td></tr><tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td><td>*</td></tr><tr><td rowspan="4">H (Dual)</td><td rowspan="2">L (Shift right)</td><td>O1 → O40</td><td rowspan="2">IN</td><td rowspan="2">OUT</td><td rowspan="2">IN</td></tr><tr><td>O41 → O80</td></tr><tr><td rowspan="2">H (Shift left)</td><td>O80 → O41</td><td rowspan="2">OUT</td><td rowspan="2">IN</td><td rowspan="2">IN</td></tr><tr><td>O40 → O1</td></tr></table> <p>* Don't care (May be set to either "H" or "L")</p>	MODE	RS/LS	Data Transfer Direction	DIO1	DIO80	DMIN	L (Single)	L (Shift right)	O1 → O80	IN	OUT	*	H (Shift left)	O80 → O1	OUT	IN	*	H (Dual)	L (Shift right)	O1 → O40	IN	OUT	IN	O41 → O80	H (Shift left)	O80 → O41	OUT	IN	IN	O40 → O1
MODE	RS/LS	Data Transfer Direction		DIO1	DIO80	DMIN																											
L (Single)	L (Shift right)	O1 → O80		IN	OUT	*																											
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		O41 → O80																															
	H (Shift left)	O80 → O41	OUT	IN	IN																												
		O40 → O1																															
82	DIO80	Input/Output																															
91	RS/LS	Input																															
95	MODE	Input																															
97	DMIN	Input																															
94	M	Input	LCD drive output alternating current (AC) signal																														
89	DISP OFF	Input	O1 to O80 output controlling input pins																														
1 80	O1 O80	Output	<p>LCD drive output</p> <p>As shown in the following table, output levels switch in response to the particular combination of scan data, M and DISP OFF signals.</p> <table><tr><th>M</th><th>Data</th><th>DISP OFF</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table> <p>* Don't care (May be set to either "H" or "L")</p>	M	Data	DISP OFF	Output	L	L	H	V2	L	H	H	V _{EE}	H	L	H	V5	H	H	H	V1	*	*	L	V1						
M	Data	DISP OFF	Output																														
L	L	H	V2																														
L	H	H	V _{EE}																														
H	L	H	V5																														
H	H	H	V1																														
*	*	L	V1																														

Common Driver Multi-Unit Connection Circuits.

* Using single mode DMIN input pins are fixed to either "H" or "L".

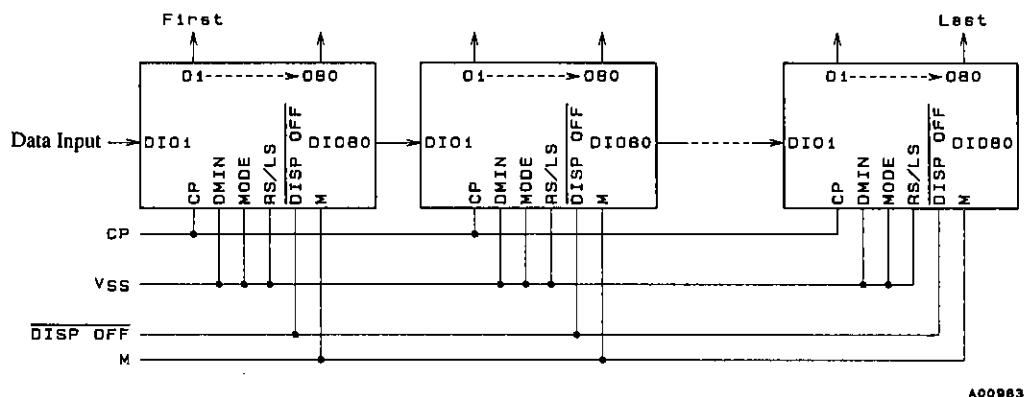


Figure 1 Single Mode (Right Directional Shift)

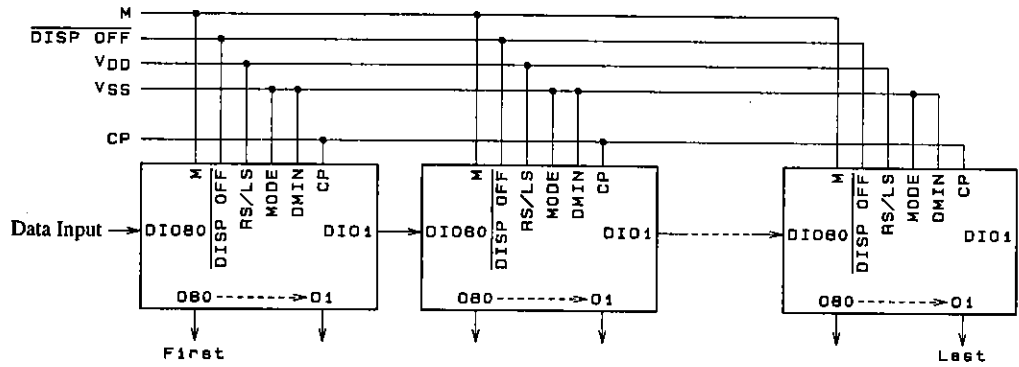


Figure 2 Single Mode (Left Directional Shift)

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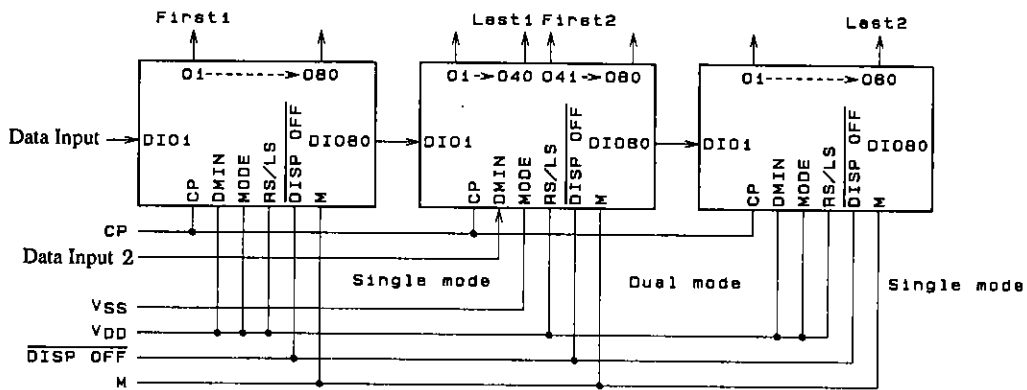


Figure 3 Dual Mode (Right Directional Shift)

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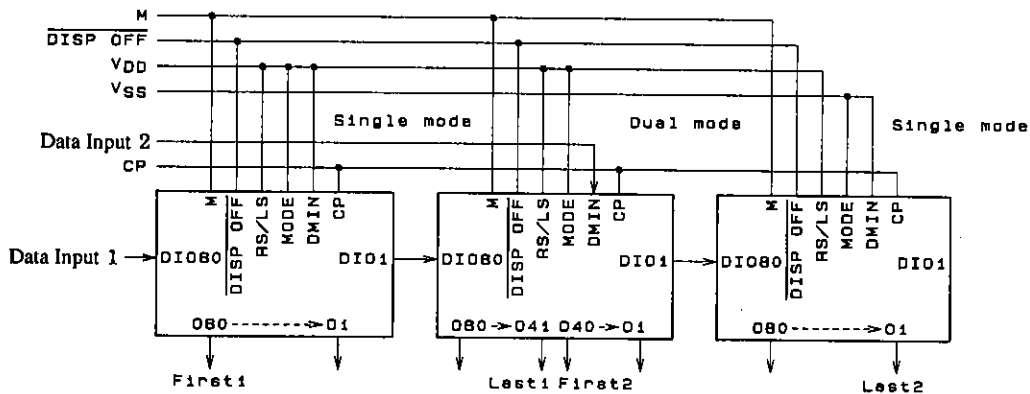


Figure 4 Dual Mode (Left Directional Shift)

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Specifications

Absolute Maximum Ratings at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$

			unit
Maximum supply voltage (LOGIC)	$V_{DD} \text{ max}$	-0.3 to +7.0	V
Maximum supply voltage (LCD)	$V_{DD} - V_{EE} \text{ max} *1$	0 to 35	V
Maximum input voltage	$V_I \text{ max}$	-0.3 to $V_{DD} + 0.3$	V
Storage temperature range	T_{stg}	-40 to +125	$^\circ\text{C}$

* 1: The following relations between elements should be maintained: $V_{DD} \geq V_I > V_2 > V_5 > V_{EE}$, $V_{DD} - V_2 \leq 7\text{V}$, $V_5 - V_{EE} \leq 7\text{V}$.

Allowable Operating Ranges at Ta = -20 to +75°C, V_{SS} = 0V

			min	typ	max	unit
Supply voltage (LOGIC)	V _{DD}		4.5		5.5	V
Supply voltage (LCD)	V _{DD} -V _{EE}	*2, *3	12		32	V
Input "H" level voltage	V _{IH}	[DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$	0.8V _{DD}			V
Input "L" level voltage	V _{IL}	[DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$			0.2V _{DD}	V
CP (Shift Clock)	f _{CP}	CP			1	MHz
CP (Pulse width)	t _{WC}	CP	63			ns
Setup time	t _{SETUP}	[DIO1 → CP, DIO80 → CP, DMIN → CP	100			ns
Hold time	t _{HOLD}	[DIO1 → CP, DIO80 → CP, DMIN → CP	100			ns
CP Rise-Fall Time	t _R	CP			50	ns
	t _F	CP			50	ns

*2 The following relations between elements should be maintained: V_{DD} ≥ V1 > V2 > V5 > V_{EE}, V_{DD} - V2 ≤ 7V, V5 - V_{EE} ≤ 7V.

*3 When the power supply is turned on, power to the LCD drive is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

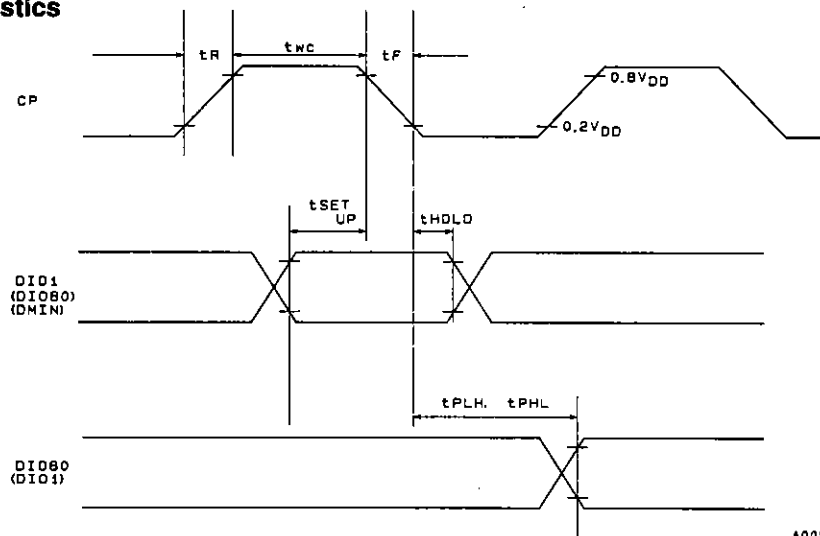
Electrical Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±10%

			min	typ	max	unit
Input "H" level current	I _{IH}	[V _{IN} = V _{DD} , V _{DD} = 5.5V; DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$			1	μA
Input "L" level current	I _{IL}	[V _{IN} = V _{SS} , V _{DD} = 5.5V; DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$	-1			μA
Output "H" level voltage	V _{OH}	[I _{OH} = -0.4mA, V _{DD} = 4.5V; DIO1, DIO80	V _{DD} -0.4			V
Output "L" level voltage	V _{OL}	[I _{OL} = 0.4mA, V _{DD} = 4.5V; DIO1, DIO80			0.4	V
Driver On Resistor	R _{ON} (1)	[V _{DD} -V _{EE} = 30V, V _{DE} -V _O = 0.5V, V _{DD} = 4.5V *4; O1 to O80			1.0	kΩ
	R _{ON} (2)	[V _{DD} -V _{EE} = 20V, V _{DE} -V _O = 0.5V, V _{DD} = 4.5V *4; O1 to O80			1.0	kΩ
Consumable current (1)	I _{SS}	[V _{DD} -V _{EE} = 30V, CP = 14kHz, no-load, V _{DD} = 5.5V; V _{SS}			100	μA
Consumable current (2)	I _{EE}	[V _{DD} -V _{EE} = 30V, CP = 14kHz, no-load, V _{DD} = 5.5V; V _{EE}			100	μA
Input Capacity	C _I	f = 1MHz; CP		5		pF

*4 V_{DE} = V1 or V2 or V5 or V_{EE}, V1 = V_{DD}, V2 = 16/17 (V_{DD}-V_{EE}), V5 = 1/17 (V_{DD}-V_{EE})

Switching Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±10%

			min	typ	max	unit
Output Delay Time	t _{PLH}	C _L = 15pF; CP → DIO1, CP → DIO80			250	ns
	t _{PHL}	C _L = 15pF; CP → DIO1, CP → DIO80			250	ns

Switching Characteristics

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