



# LC7972VA, 7972VB

## CMOS Operational Amplifier with Programmable Offset Correction Function

### Overview

The LC7972VA and LC7972VB are dual inverting/noninverting operational amplifier ICs that are fabricated in a CMOS process. These ICs provide a programmable offset correction function and a power saving function for use when the operational amplifier is unused, both of which can be controlled from a microprocessor interface.

### Features

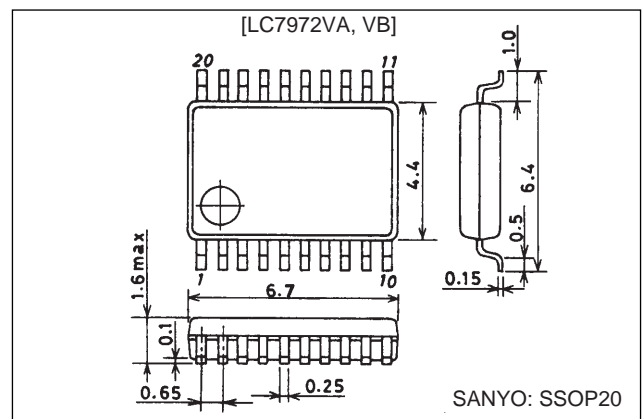
- High input impedance provided by fabrication in a CMOS process.
- Low power provided by fabrication in a CMOS process.
- One of two types of operational amplifier can be selected: inverting (operational amplifier 1) or noninverting (operational amplifier 2)
- Operating supply voltage: 4.9 to 5.2 V
- Package: SSOP20
- Operating temperature:  $T_a = -30$  to  $+70^\circ\text{C}$

- The following modes are supported. These are selected via port level settings.

### Package Dimensions

unit: mm

#### 3179A-SSOP20



Port	Level	Function
OP1ON	L	Operational amplifier 1: Operation stopped (low-power mode)
	H	Operational amplifier 1: Normal operation (OP2ON must be low in this mode.)
OP2ON	L	Operational amplifier 2: Operation stopped (low-power mode)
	H	Operational amplifier 2: Normal operation (OP1ON must be low in this mode.)
OFST1	L	Operational amplifier 1: Offset mode (inverting input = $V_{SS}$ )
	H	Operational amplifier 1: Operating mode (inverting input = normal input)
OFST2	L	Operational amplifier 2: Offset mode (noninverting input = $V_{SS}$ )
	H	Operational amplifier 2: Operating mode (noninverting input = normal input)
CLKC	L	Operational amplifier power supply clock: Internal clock

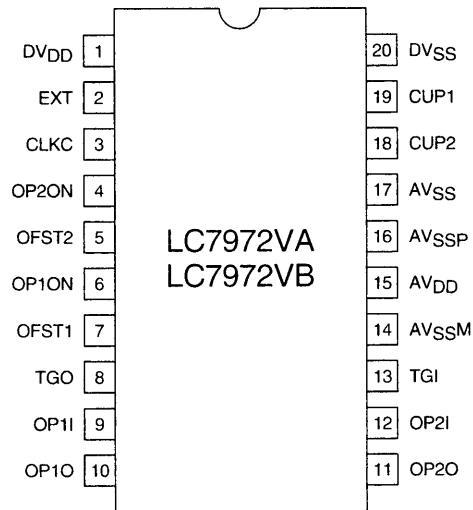
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## LC7972VA, 7972VB

### Pin Assignment



Top view

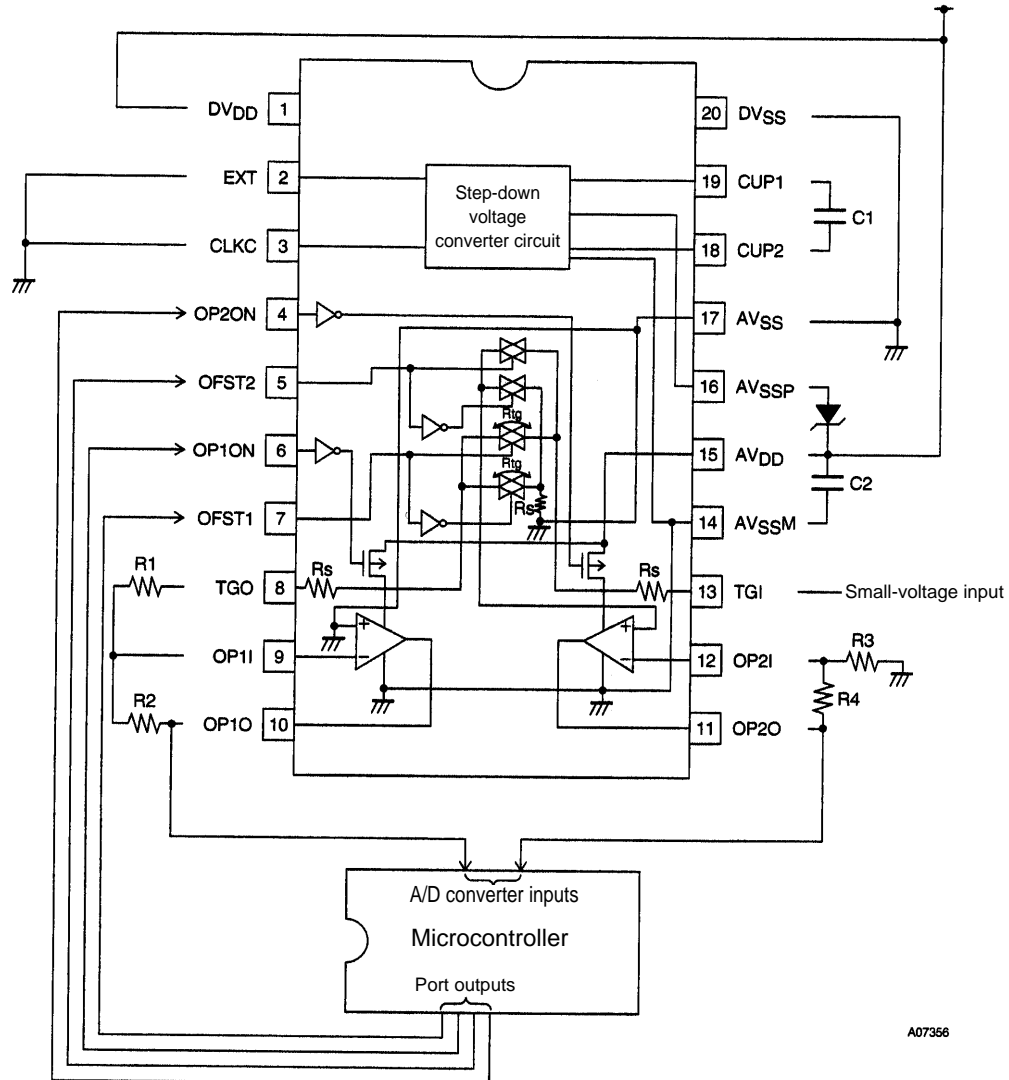
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### Pin Functions

Pin		Function
No.	Symbol	
1	DV <sub>DD</sub>	Digital system power supply. Normally connected to +5 V.
2	EXT	Must be tied low.
3	CLKC	Must be tied low.
4	OP2ON	Operational amplifier 2 operation control
5	OFST2	Operational amplifier 2 mode control
6	OP1ON	Operational amplifier 1 operation control
7	OFST1	Operational amplifier 1 mode control
8	TGO	Operational amplifier 1 VSS/small voltage output
9	OP1I	Operational amplifier 1 input
10	OP1O	Operational amplifier 1 output
11	OP2O	Operational amplifier 2 output
12	OP2I	Operational amplifier 2 input
13	TGI	Small voltage input common to operational amplifiers 1 and 2
14	AV <sub>SSM</sub>	Operational amplifier power supply minus voltage generation
15	AV <sub>DD</sub>	Analog system power supply. Normally connected to +5 V.
16	AV <sub>SSP</sub>	Operational amplifier power supply external Zener diode connection
17	AV <sub>SS</sub>	Analog system ground. Must be connected to 0 V.
18	CUP2	Operational amplifier power supply external capacitor connection 2
19	CUP1	Operational amplifier power supply external capacitor connection 1
20	DV <sub>SS</sub>	Digital system ground. Must be connected to 0 V.

## System Block Diagram and Sample Application

A circuit that amplifies very small voltages around the  $V_{SS}$  level can be constructed by adding the peripheral circuits shown in the figure below.



# LC7972VA, 7972VB

## Specifications

**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$V_{DD}$	-0.3 to +7.0	V
Output voltage	$V_O$	OP1O, OP2O, TGO	-0.3 to $V_{DD}+0.3$	V
Input voltage	$V_{I1}$	OP1ON, OFST1, OP2ON, OFST2, EXT, CLKC, CUP2, CUP1, $AV_{SSP}$ , OP1I, OP2I, TGI	-0.3 to $V_{DD}+0.3$	V
	$V_{I2}$	$AV_{SSM}$	-3 to +0.3	V
Peak output current	$I_{OP}$	OP1O, OP2O, TGO	-1 to +1	mA
Average output current	$I_{OA}$	OP1O, OP2O, TGO : The current per pin	-1 to +1	mA
Allowable power dissipation	$P_{d\text{ max}}$	SSOP20 : $T_a = -30$ to $+70^\circ\text{C}$	100	mW
Operating temperature	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

**Allowable Operating Ranges at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.9$  to  $5.2\text{ V}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$	$V_{DD}$	4.9		5.2	V
Input high-level voltage	$V_{IH}$	OP1ON, OFST1, OP2ON, OFST2	$0.7 V_{DD}$		$V_{DD}$	V
Input low-level voltage	$V_{IL1}$	OP1ON, OFST1, OP2ON, OFST2, CLKC	$V_{SS}$		$0.3 V_{DD}$	V
	$V_{IL2}$	EXT	$V_{SS}$		$0.3 V_{DD}$	V
Common-mode input voltage	$V_{IC}$		0		4.2	V
Voltage drop	$D_V$	$AV_{SSM}$ : Zener diode = 5.1 V (X rank specified)		-0.2		V

**Electrical Characteristics at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.9$  to  $5.2\text{ V}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH1}$	OP1ON, OFST1, OP2ON, OFST2 : $V_{IN} = V_{DD}$			1.0	$\mu\text{A}$
	$I_{IH2}$	TGI: $V_{IN} = V_{DD}$ , with the built-in TG off.			1.0	$\mu\text{A}$
Input low-level current	$I_{IL1}$	OP1ON, OFST1, OP2ON, OFST2, EXT, CLKC : $V_{IN} = V_{SS}$	-1.0			$\mu\text{A}$
	$I_{IL2}$	TGI: $V_{IN} = V_{SS}$ , with the built-in TG off.	-1.0			$\mu\text{A}$
Output high-level voltage	$V_{OH}$	OP1O, OP2O : $I_{OH} = -3\text{ }\mu\text{A}$	$V_{DD} - 0.5$			V
Output low-level voltage	$V_{OL}$	OP1O, OP2O : $I_{OL} = 3\text{ }\mu\text{A}$			0.5	V
Operational amplifier 1 gain-related resistance	$R_{tg} + 2R_s$	TGO, TGI	500	700	900	$\Omega$
Operational amplifier 1 gain-related resistance difference	$ R_x - R_y $	TGO, TGI: Offset mode: $R_x = R_{tg} + 2R_s$ Operating mode: $R_y = R_{tg} + 2R_s$			80	$\Omega$
Current drain						
Operating	$I_{DDOP}$	$V_{DD}$ : Using the internal clock, with the operational amplifier 1 circuit operating.		700	900	$\mu\text{A}$
Standby	$I_{DDST}$	$V_{DD}$ : Both operational amplifiers 1 and 2 stopped.		0.05	10	$\mu\text{A}$

**Operational Amplifier Characteristics at  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.9$  to  $5.2\text{ V}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input offset voltage	$V_{IO}$	OP1I, OP2I : LC7972VA LC7972VB		5	10.5	mV
				5	15	mV
Supply voltage rejection ratio	$P_{SRR}$	1 kHz		60		dB
Common-mode rejection ratio	$C_{MRR}$			60		dB
Open-loop voltage gain	$A_O$			80		dB
0-dB bandwidth	$f_T$			90		kHz
Maximum output voltage	$V_O$	OP1O, OP2O : $R_L \geq 100\text{ k}\Omega$		$V_{DD} - 0.5$		V
Current drain	$I_{CC}$	For the operational amplifier 1 circuit		100		$\mu\text{A}$
Settling time	$T_{SET}$	OP1O, OP2O		900		$\mu\text{s}$