



LC864164B/56B/48B/40B

8-bit Single Chip Microcontroller

Overview

The LC864164B/56B/48B/40B microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks:

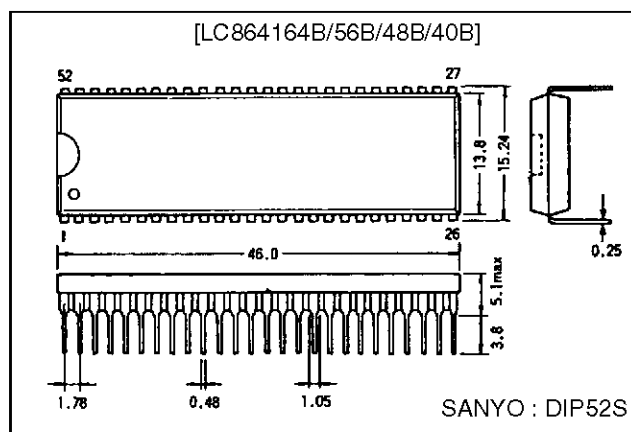
- CPU : Operable at a minimum bus cycle time of 0.5 μ s
- On-chip ROM maximum capacity : 64 K bytes
- On-chip RAM capacity : 384 bytes
- CRT display RAM : 640 \times 9 bits
- Closed-caption TV controller and the on-screen display controller
- 16-bit timer/counter
- 4 channel \times 4-bit A/D Converter
- 8-bit synchronous serial-interface circuit
- Closed-caption data slicer
- 12-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Package Dimensions

unit : mm

3128-DIP52S



Features

- (1) Read-only memory (ROM) :
- | | |
|-----------|-----------------------|
| LC864164B | 65280×8 bits |
| LC864156B | 57344×8 bits |
| LC864148B | 49152×8 bits |
| LC864140B | 40960×8 bits |
- (2) Random access memory (RAM) :
- | |
|---------------------------------------|
| 384×8 bits |
| 640×9 bits (for CRT display) |

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(3) OSD functions

- Screen for display : 34 columns \times 16 rows (at standard character size)
- Display for RAM : 640 \times 9 bits (6 columns for control + 34 columns for display) \times 16 rows \times 9 bits
- 252 kinds of user specified characters
 - 125 kinds 9 \times 9 dots
 - 127 kinds 12 \times 18 dots
- Various character attributes
 - Character colors : 16 colors
 - Character background colors : 16 colors
 - Fringe / shadow colors : 16 colors
 - Full screen colors : 16 colors
 - Fringe / shadow
 - Rounding
 - Underline
 - Italic character (slanting)
- Close-character attribute data changing available
- Vertical display start line setting available (Row overlapping available)
- Horizontal display start position setting available
- Display mode specification by row (Display mode mixable)
 - capio mode / text mode / OSD mode
- Eight kinds of characters size
 - Horiz \times Vert. = (1 \times 1), (1 \times 2), (2 \times 2), (2 \times 4)
 - (1.5 \times 1), (1.5 \times 2), (3 \times 2), (3 \times 4)
- Shuttering and scrolling in row unit available
- Horizontal character pitch selectable : 9 to 16 dots
- Polarity of R, G, B, I, BL output programmable
- Polarity of HS, VS input programmable

(4) Bus cycle time / Instruction-cycle time

The LC864164A/56A/48A/40A microcontrollers are designed to read the ROM twice within one instruction cycle. It has about 1.7 times performance capability within the same instruction-cycle compared to our 4-bit microcontrollers (LC66000 series).

The bus cycle time indicates the speed to read ROM.

| Bus cycle time | Instruction cycle time | System clock oscillation | Oscillation frequency | Voltage |
|----------------|------------------------|--------------------------|-----------------------|----------------|
| 0.5 μ s | 1.0 μ s | Ceramic (CR) | 12 MHz | 4.5 V to 5.5 V |
| 7.5 μ s | 15.0 μ s | Internal RC | 800 kHz | 4.5 V to 5.5 V |

(5) Ports

- Input/output port : 2 ports (16 lines)
 - Input/output port programmable in nibble unit : 1 port (8 lines)
 (When the N-channel open drain output is selected, the data in a bit can be inputted.)
- Input/output port programmable in a bit : 1 port (8 lines)
- Input port : 2 ports (8 lines)

(6) A/D converter

- 4-channel \times 4-bit A/D converter (converted with program)

(7) PWM output

- 10-channel \times 7-bit PWM

(8) Timer

- Timer 0 : 16-bit timer / counter

2-bit prescaler + 8-bit built-in programmable prescaler

Mode 0 : Two 8-bit timers with a programmable prescaler

Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter

Mode 2 : 16-bit timer with a programmable prescaler

Mode 3 : 16-bit counter

The resolution of timer is 1 tCYC.

- Timer 1 : 16-bit timer / PWM

Mode 0 : Two 8-bit timers

Mode 1 : 8-bit timer + 8-bit PWM

Mode 2 : 16-bit timer

Mode 3 : Variable-bit PWM (9 to 16 bits)

In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.

In Mode 2 and Mode 3, the resolution of Timer and PWM selectable : tCYC or 1/2tCYC by program.

(9) Remote control receiver circuit (shares with the P73/INT3/T0IN terminal)

- Noise rejection function

- Polarity switching

(10) Watchdog timer

External RC circuit is required

Interrupt or system reset is selectable

(11) Interrupts

- 12-source 10-vectored interrupts

1. External interrupt INT0

2. External interrupt INT1

3. External interrupt INT2, Timer/counter T0L (Lower 8 bits)

4. External interrupt INT3

5. Timer/counter T0H (Upper 8 bits)

6. Timer T1H, T1L

7. Serial interface 0 (SIO0)

8. Data slicer

9. Vertical synchronous signal interrupt (\overline{VS})

10. Port 0

- Interrupt priority control available

Three interrupt priorities are supported (low, high and the highest) and multilevel nesting is possible. Low or high priority can be assigned to the interrupt from 3 to 10 listed above. For the external interrupt INT0 and INT1, high or the highest priority can be set.

(12) Sub-routine stack level

- A maximum of 128 levels (Sets the stack inside a RAM.)

(13) Multiplication/division instruction

- 16 bits \times 8 bits (7 instruction cycle times)

- 16 bits / 8 bits (7 instruction cycle times)

(14) 3 oscillation circuits

- On-chip RC oscillation circuit for the system clock
- On-chip CP oscillation circuit for the system clock
- On-chip LC oscillation circuit for the CRT synchronization

(15) Standby function

- HALT mode function

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped.

This mode can be released by the interrupt request signals or the system reset.

- HOLD mode

The HOLD mode is used to stop oscillations ; the RC (internal) and the ceramic oscillations.

This mode can be released by the following conditions.

- Pull the reset terminal (RES) to low level.
- Feed the selected level to either P70/INT0 or P71/INT1.
- Feed the Port 0 interrupt condition.

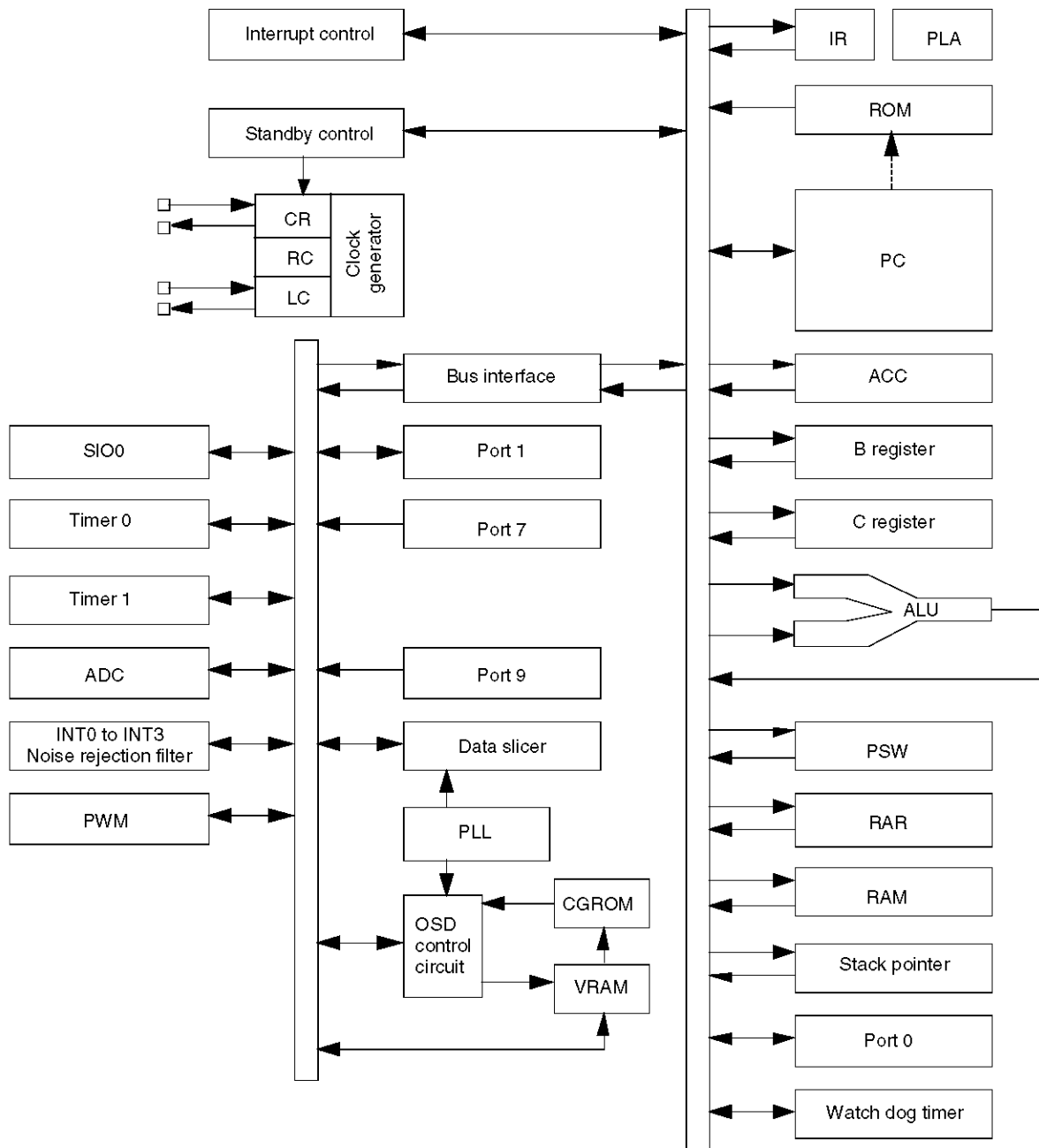
(16) Factory shipment

DIP52S

(17) Development Tool

- Evaluation chip : LC866098
- EPROM with a window : LC86E4164
- One time : LC86P4164
- Emulator : EVA86000 (Main) + ECB864100 (Evaluation board) + POD864100 (Pod)

System Block Diagram



Pin Assignment

| | | | |
|-------------|----|----|---------------|
| P10/SO0 | 1 | 52 | P07 |
| P11/SI0/SB0 | 2 | 51 | P06 |
| P12/SCK0 | 3 | 50 | P05 |
| P13 | 4 | 49 | P04 |
| P14 | 5 | 48 | P03 |
| P15 | 6 | 47 | P02 |
| P16 | 7 | 46 | P01 |
| P17/PWM | 8 | 45 | P00 |
| DVSS | 9 | 44 | P73/INT3/T0IN |
| CF1 | 10 | 43 | P72/INT2/T0IN |
| CF2 | 11 | 42 | P71/INT1 |
| DVDD | 12 | 41 | P70/INT0 |
| P90/AN0 | 13 | 40 | PWM9 |
| P91/AN1 | 14 | 39 | PWM8 |
| P92/AN2 | 15 | 38 | PWM7 |
| P93/AN3 | 16 | 37 | PWM6 |
| RES | 17 | 36 | PWM5 |
| LC1 | 18 | 35 | PWM4 |
| LC2 | 19 | 34 | PWM3 |
| FILT | 20 | 33 | PWM2 |
| AVDD | 21 | 32 | PWM1 |
| AVSS | 22 | 31 | PWM0 |
| CVIN | 23 | 30 | BL |
| VS | 24 | 29 | B |
| HS | 25 | 28 | G |
| I | 26 | 27 | R |

Top view

Pin Description

- Port option can be specified in bit units except the pull-up resistor selection of port 0.

| Pin name | Pin No. | I/O | Function description | Option | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|--|--------------|--|---|--|--------|--|-----|--------------------------------|-----|--|-----|-------------------------|---------|----------------------|---------|---------|--------|------|--------|--------|---------|--------|--------|-----|------|--------|--------|---------|--------|--------|-----|------|--------|--------|--------|---------|---------|-----|------|--------|--------|--------|---------|---------|-----|--|
| DVSS | 9 | — | Negative power supply for digital circuit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CF1 | 10 | Input | Input terminal for ceramic resonator | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CF2 | 11 | Output | Output terminal for ceramic resonator | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DVDD | 12 | — | Positive power supply for digital circuit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{RES}}$ | 17 | Input | Reset terminal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LC1 | 18 | Input | LC oscillation circuit input terminal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LC2 | 19 | Output | LC oscillation circuit output terminal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FILT | 20 | Output | Filter terminal for PLL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AVDD | 21 | — | Positive power supply for analog circuit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AVSS | 22 | — | Negative power supply for analog circuit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CVIN | 23 | Input | Video signal input terminal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{VS}}$ | 24 | Input | Vertical synchronization signal input terminal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{HS}}$ | 25 | Input | Horizontal synchronization signal input terminal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | 26 | Output | Image intensity output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | 27 | Output | Red (R) output terminal of RGB image output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | 28 | Output | Green (G) output terminal of RGB image output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | 29 | Output | Blue (B) output terminal of RGB image output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BL | 30 | Ouptut | Fast blanking control signal Switch TV image signal and caption/OSD image signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PWM0 to PWM9 | 31 to 40 | Output | PWM0 to 9 output terminals 15 V withstand | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 0 P00 to P07 | 45 to 52 | I/O | 8-bit Input/output port Input/output can be specified in nibble units HOLD release input Interrupt input | Pull-up resistor Provided/not provided (in bit units) Output Format CMOS/Nch-OD (in bit units) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 1 P10 to P17 | | | | | 1 to 8 | I/O | 8-bit Input/output port Input/output can be specified in bit units Other function <table border="1"><tr><td>P10</td><td>SIO0 data output</td></tr><tr><td>P11</td><td>SIO0 data input / bus input/output</td></tr><tr><td>P12</td><td>SIO0 clock input/output</td></tr><tr><td>P17</td><td>Timer 1 (PWM) output</td></tr></table> | P10 | SIO0 data output | P11 | SIO0 data input / bus input/output | P12 | SIO0 clock input/output | P17 | Timer 1 (PWM) output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P10 | SIO0 data output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P11 | SIO0 data input / bus input/output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P12 | SIO0 clock input/output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P17 | Timer 1 (PWM) output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 7 P70 P71 to P73 | 41 42 to 44 | I/O Input | 4-bit input port Other function <table border="1"><tr><td>P70</td><td>INT0 input/HOLD release input/ Nch-transistor output for watchdog timer</td></tr><tr><td>P71</td><td>INT1 input/HOLD release input</td></tr><tr><td>P72</td><td>INT2 input/timer 0 event input</td></tr><tr><td>P73</td><td>INT3 input (noise rejection filter attached input/ timer 0 event input)</td></tr></table> Interrupt receiver format vector address <table border="1"><thead><tr><th></th><th>Rising</th><th>Falling</th><th>Rising/Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr></thead><tbody><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr></tbody></table> | P70 | INT0 input/HOLD release input/ Nch-transistor output for watchdog timer | P71 | INT1 input/HOLD release input | P72 | INT2 input/timer 0 event input | P73 | INT3 input (noise rejection filter attached input/ timer 0 event input) | | Rising | Falling | Rising/Falling | H level | L level | Vector | INT0 | enable | enable | disable | enable | enable | 03H | INT1 | enable | enable | disable | enable | enable | 0BH | INT2 | enable | enable | enable | disable | disable | 13H | INT3 | enable | enable | enable | disable | disable | 1BH | Pull-up resistor provided/ not provided (in bit units) |
| P70 | | | | INT0 input/HOLD release input/ Nch-transistor output for watchdog timer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P71 | INT1 input/HOLD release input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P72 | INT2 input/timer 0 event input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P73 | INT3 input (noise rejection filter attached input/ timer 0 event input) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Rising | Falling | Rising/Falling | H level | L level | Vector | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT0 | enable | enable | disable | enable | enable | 03H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT1 | enable | enable | disable | enable | enable | 0BH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT2 | enable | enable | enable | disable | disable | 13H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT3 | enable | enable | enable | disable | disable | 1BH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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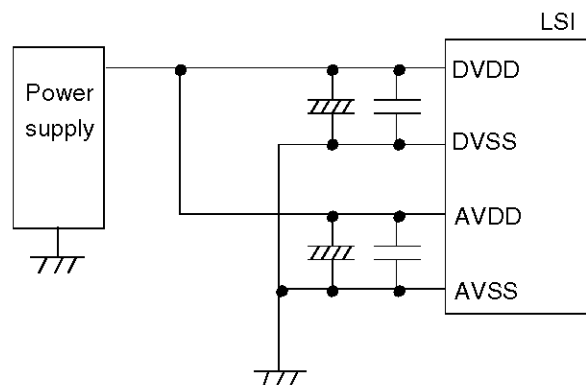
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| Pin name | Pin No. | I/O | Function description | Option |
|------------|----------|-------|---|--------|
| Port 9 | 13 to 16 | Input | 4-bit input port | |
| P90 to P93 | | | Other functions A/D converter input port (4 lines) | |

- Any port option can be selected in bit units.
- Port 0 option : Pull-up resistor is provided when CMOS output is selected.
The pull-up resistor is not provided when N-ch Open Drain is selected.
- Port 1 option: Programmable pull-up resistor is provided when any output form is selected.
- Port status during reset

| Terminal | I/O | Pull-up resistor status at selecting pull-up option |
|----------|-------|---|
| Port 0 | Input | Pull-up resistor OFF, ON after reset release |
| Port 1 | Input | Programmable pull-up resistor OFF |
| Port 7 | Input | Fixed pull-up resistor provided |

* AVDD and AVSS are the power supply terminals for built-in analog circuit while DVDD and DVSS are the power supply terminals for built-in digital circuit. Connect them like the following figure to reduce the mutual noise influence.



Specifications

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

| Parameter | | Symbol | Pins | Conditions | V _{DD} [V] | Ratings | | | Unit |
|-----------------------------|----------------------|-----------------------|--|--|---------------------|---------|-----|----------------------|------|
| | | | | | | min | typ | max | |
| Supply voltage | | V _{DDmax} | DVDD, AVDD | DVDD = AVDD | | −0.3 | | 7.0 | V |
| Input voltage | | V _I (1) | • P71, 72, 73 • Port 9 • RES, HS, VS, CVIN | | | −0.3 | | V _{DD} +0.3 | |
| Output voltage | | V _O (1) | R, G, B, BL, I, FILT | | | −0.3 | | V _{DD} +0.3 | |
| | | V _O (2) | PWM0 to PWM9 | | | −0.3 | | 15 | |
| Input/output voltage | | V _{IO} (1) | Ports 0, 1, P70 | | | −0.3 | | V _{DD} +0.3 | mA |
| High-level output current | Peak output current | I _{OPH} (1) | Ports 0, 1 | • Pull-up MOS Transistor output • At each pin | | −2 | | | |
| | | I _{OPH} (2) | Ports 0, 1 | • CMOS output • At each pin | | −4 | | | |
| | | I _{OPH} (3) | R, G, B, BL, I | • CMOS output • At each pin | | −5 | | | |
| | Total output current | ΣI _{OA} H(1) | Port 1 | The total of all pins | | −10 | | | |
| | | ΣI _{OA} H(2) | Port 0 | The total of all pins | | −10 | | | |
| | | ΣI _{OA} H(3) | R, G, B, BL, I | The total of all pins | | −15 | | | |
| Low-level output current | Peak output current | I _{OPL} (1) | Ports 0, 1 | At each pin | | | | 20 | |
| | | I _{OPL} (2) | P70 | At each pin | | | | 30 | |
| | | I _{OPL} (3) | • R, G, B, BL, I • PWM0 to PWM9 | At each pin | | | | 5 | |
| | Total output current | ΣI _{OA} L(1) | Port 0 | The total of all pins | | | | 40 | |
| | | ΣI _{OA} L(2) | Port 1, P70 | The total of all pins | | | | 40 | |
| | | ΣI _{OA} L(3) | R, G, B, BL, I | The total of all pins | | | | 15 | |
| | | ΣI _{OA} L(4) | PWM0 to PWM9 | The total of all pins | | | | 30 | |
| Maximum power dissipation | | P _d max | DIP52S | T _a = −30 to +70°C | | | | 430 | mW |
| Operating temperature range | | T _{opr} | | | | −30 | | +70 | °C |
| Storage temperature range | | T _{stg} | | | | −55 | | +150 | |

*DVSS and AVSS must be supplied the same voltage, V_{SS}.
 DVDD and AVDD must be supplied the same voltage, V_{DD}.

V_{SS} = DVSS = AVSS
 V_{DD} = DVDD = AVDD

2. Recommended Operating Range at Ta = -30°C to +70°C, V_{SS} = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|--------------------------------|---------------------|--|--|---------------------|----------------------|-------|---------------------|--------|
| | | | | V _{DD} [V] | min | typ | max | |
| Operating supply voltage range | V _{DD} | DVDD, AVDD | 0.98 μs ≤ tCYC tCYC ≤ 1.02 μs | | 4.5 | | 5.5 | V |
| Hold voltage | V _{HD} | DVDD, AVDD | RAMs and the registers hold data at HOLD mode. | | 2.0 | | 5.5 | |
| Input high-level voltage | V _{IH} (1) | Port 0 (Schmitt) | Output disable | 4.5 to 5.5 | 0.6V _{DD} | | V _{DD} | |
| | V _{IH} (2) | • Port 1 (Schmitt) • P72,73 • HS,VS | Output disable | 4.5 to 5.5 | 0.75V _{DD} | | V _{DD} | |
| | V _{IH} (3) | • P70 port input / interrupt • P71 • RES (Schmitt) | Output N-channel transistor OFF | 4.5 to 5.5 | 0.75V _{DD} | | V _{DD} | |
| | V _{IH} (4) | P70 Watchdog timer input | Output N-channel transistor OFF | 4.5 to 5.5 | V _{DD} -0.5 | | V _{DD} | |
| | V _{IH} (5) | Port 9 port input | | 4.5 to 5.5 | 0.7V _{DD} | | V _{DD} | |
| Input low-level voltage | V _{IL} (1) | Port 0 (Schmitt) | Output disable | 4.5 to 5.5 | V _{SS} | | 0.2V _{DD} | |
| | V _{IL} (2) | • Port 1 (Schmitt) • P72,73 • HS,VS • Port 9 | Output disable | 4.5 to 5.5 | V _{SS} | | 0.25V _{DD} | |
| | V _{IL} (3) | • P70 port input / interrupt • P71 • RES (Schmitt) | N-channel transistor OFF | 4.5 to 5.5 | V _{SS} | | 0.25V _{DD} | |
| | V _{IL} (4) | P70 Watchdog timer input | N-channel transistor OFF | 4.5 to 5.5 | V _{SS} | | 0.6V _{DD} | |
| | V _{IL} (5) | Port 9 port input | | 4.5 to 5.5 | V _{SS} | | 0.3V _{DD} | |
| CVIN input amplitude | V _{CVIN} | CVIN | | 5.0 | 1Vp-p -3dB | 1Vp-p | 1Vp-p +3dB | Vp-p * |
| Operation cycle time | tCYC(1) | | OSD function | 4.5 to 5.5 | 0.98 | 1 | 1.02 | μs |
| | tCYC(2) | | Except OSD function | 4.5 to 5.5 | 0.98 | | 30 | |

* Vp-p : Peak-to-peak voltage

LC864164B/56B/48B/40B

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|--|--------|----------|--|---------------------|-------|-------|-------|------|
| | | | | V _{DD} [V] | min | typ | max | |
| Oscillation frequency range (Note 1) | FmCF | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 1. | 4.5 to 5.5 | 11.76 | 12 | 12.24 | MHz |
| | FmLC | LC1, LC2 | 14.11 MHz (LC oscillation) Refer to Figure 2. | 4.5 to 5.5 | | 14.11 | | |
| | FmRC | | RC oscillation | 4.5 to 5.5 | 0.4 | 1.5 | 3.0 | |
| Oscillation stable time period (Note 2) | tmsCF | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 3. | 4.5 to 5.5 | | 0.02 | 0.2 | ms |

(Note 1) The oscillation constant is shown on Table 1 and Table 2.

(Note 2) The oscillation stable time period is the time necessary for the oscillation to become stable after the following conditions.

1. Supplying voltage.
 2. Release the HOLD mode.
 3. Release stopping the main-clock oscillation.
- Refer to Page 3 for details.

3. Electrical Characteristics at Ta = -30°C to +70°C, V_{SS} = 0 V

| Parameter | Symbol | Pins | Conditions | V _{DD} [V] | Ratings | | | Unit |
|-----------------------------------|---------------------|---|---|---------------------|----------------------|--------------------|-----|------|
| | | | | | min | typ | max | |
| Input high-level current | I _{IH} (1) | <ul style="list-style-type: none"> Port 1 Port 0 without pull-up MOS transistor | <ul style="list-style-type: none"> Output disable Pull-up MOS transistor OFF V_{IN} = V_{DD} (including the off-leak current of the output transistor) | 4.5 to 5.5 | | | 1 | μA |
| | I _{IH} (2) | <ul style="list-style-type: none"> Port 7 without pull-up MOS transistor Port 9 <u>RES</u> HS, VS | V _{IN} = V _{DD} | 4.5 to 5.5 | | | 1 | |
| Input low-level current | I _{IL} (1) | <ul style="list-style-type: none"> Port 1 Port 0 without pull-up MOS transistor | <ul style="list-style-type: none"> Output disable Pull-up MOS transistor OFF V_{IN} = V_{SS} (including the off-leak current of the output transistor) | 4.5 to 5.5 | -1 | | | |
| | I _{IL} (2) | <ul style="list-style-type: none"> Port 7 without pull-up MOS transistor Port 9 | V _{IN} = V _{SS} | 4.5 to 5.5 | -1 | | | |
| | I _{IL} (3) | <ul style="list-style-type: none"> <u>RES</u> HS, VS | V _{IN} = V _{SS} | 4.5 to 5.5 | -1 | | | |
| Output high-level voltage | V _{OH} (1) | CMOS output of ports 0, 1 | I _{OH} = -1.0 mA | 4.5 to 5.5 | V _{DD} -1 | | | V |
| | V _{OH} (2) | R, G, B, BL, I | I _{OH} = -0.1 mA | 4.5 to 5.5 | V _{DD} -0.5 | | | |
| Output low-level voltage | V _{OL} (1) | Ports 0, 1 | I _{OL} = 10 mA | 4.5 to 5.5 | | | 1.5 | |
| | V _{OL} (2) | Ports 0, 1 | <ul style="list-style-type: none"> I_{OL} = 1.6 mA The total current of the ports 0,1 is not over 40 mA. | 4.5 to 5.5 | | | 0.4 | |
| | V _{OL} (3) | <ul style="list-style-type: none"> R, G, B, BL, I PWM0 to PWM9 | <ul style="list-style-type: none"> I_{OL} = 3.0 mA The current of any unmeasured pin is not over 3 mA. | 4.5 to 5.5 | | | 0.4 | |
| | V _{OL} (4) | P70 | I _{OL} = 1 mA | 4.5 to 5.5 | | | 0.4 | |
| Pull-up MOS transistor resistance | R _{pu} | <ul style="list-style-type: none"> Ports 0, 1 Port 7 | V _{OH} = 0.9V _{DD} | 4.5 to 5.5 | 13 | 38 | 80 | kΩ |
| Output off-leakage current | I _{OFF} | PWM0 to PWM9 | V _{OUT} = 13.5V | 4.5 to 5.5 | | | 5 | μA |
| Hysteresis voltage | V _{HIS} | <ul style="list-style-type: none"> Ports 0, 1 Port 7 <u>RES</u> HS, VS | Output disable | 4.5 to 5.5 | | 0.1V _{DD} | | V |

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| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---------------------|-------------------|----------|--|---------------------|-----|-----|-----|------|
| | | | | V _{DD} [V] | min | typ | max | |
| Input clamp voltage | V _{CLMP} | CVIN | | 5.0 | 2.3 | 2.5 | 2.7 | V |
| Pin capacitance | CP | All pins | • f = 1 MHz • Unmeasured terminals for the input are set to V _{SS} level. • Ta = 25°C | 4.5 to 5.5 | | 10 | | pF |

4. Serial Input/Output Characteristics at Ta = -30°C to +70°C , V_{SS} = 0 V

| Parameter | | | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---------------|---|------------------------|----------|---|--|---------------------|-----|---------------|-----|------|
| | | | | | | V _{DD} [V] | min | typ | max | |
| Serial clock | Input clock | Cycle | tCKCY(1) | • SCK0 • SCLK0 | Refer to Figure 5 | 4.5 to 5.5 | 2 | | | tCYC |
| | | Low-level pulse width | tCKL(1) | | | 4.5 to 5.5 | 1 | | | |
| | | High-level pulse width | tCKH(1) | | | 4.5 to 5.5 | 1 | | | |
| | Output clock | Cycle | tCKCY(2) | • SCK0 • SCLK0 | • Use a pull-up resistor (1 kΩ) during open drain output • Refer to Figure 5. | 4.5 to 5.5 | 2 | | | |
| | | Low-level pulse width | tCKL(2) | | | 4.5 to 5.5 | | 1/2tCKCY | | |
| | | High-level pulse width | tCKH(2) | | | 4.5 to 5.5 | | 1/2tCKCY | | |
| Serial input | Data set-up time | tICK | SI0 | • Data set-up to SCK0 rising • Data hold from SCK0 rising • Refer to Figure 5. | 4.5 to 5.5 | 0.1 | | | μs | |
| | Data hold time | tCKI | | | 4.5 to 5.5 | 0.1 | | | | |
| Serial output | Output delay time (External serial clock) | tCKO(1) | SO0 | • Use a pull-up resistor (1 kΩ) during open drain output. • Data set-up to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 5. | 4.5 to 5.5 | | | 7/12tCYC +0.2 | μs | |
| | Output delay time (Internal serial clock) | tCKO(2) | | | 4.5 to 5.5 | | | 1/3tCYC +0.2 | | |

5. Pulse Input Conditions at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|----------------------------|--------------------|---|--|---------------------|-------|-------|-------|---------------|
| | | | | $V_{DD} [\text{V}]$ | min | typ | max | |
| High/low level pulse width | tPIH(1) tPIL(1) | •INT0, INT1 •INT2/T0IN | •Interrupt acceptable •Timer0-countable | 4.5 to 5.5 | 1 | | | tCYC |
| | tPIH(2) tPIL(2) | INT3/T0IN (The noise rejection filter time constant is 1/1) | •Interrupt acceptable •Timer0-countable | 4.5 to 5.5 | 2 | | | |
| | tPIH(3) tPIL(3) | INT3/T0IN (The noise rejection filter time constant is 1/16) | •Interrupt acceptable •Timer0-countable | 4.5 to 5.5 | 32 | | | |
| | tPIL(4) | RES | Reset acceptable | 4.5 to 5.5 | 200 | | | μs |
| | tPIH(5) tPIL(5) | HS, VS | Display position controllable Each active edge of HS, VS must be more than 1tCYC. Refer to Figure 7. | 4.5 to 5.5 | 10 | | | tCYC |
| | | | | | | | | |
| Rising/falling time | tTHL tTLH | HS | Refer to Figure 7. | 4.5 to 5.5 | | | 500 | ns |
| Horizontal pull-in range | FH | HS | The monitor point in figure 10 is $1/2 V_{DD}$. | 4.5 to 5.5 | 15.23 | 15.73 | 16.23 | kHz |

6. A/D Converter Characteristics at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|----------------------------|-------------------|----------------------------------|------------------------------------|---------------------|-----------------|-----------|-----------------|---------------|
| | | | | $V_{DD} [\text{V}]$ | min | typ | max | |
| Resolution | N | | | 4.5 to 5.5 | | 4 | | bit |
| Absolute precision | ET | | (Note 3) | 4.5 to 5.5 | | $\pm 1/4$ | $\pm 1/2$ | LSB |
| Conversion time | tCAD | From selecting Vref to resulting | 1 bit conversion time = 2tCYC | 4.5 to 5.5 | | | 1.96 | μs |
| Reference current | I _{REF} | | (Regulate the ladder resistor) | 4.5 to 5.5 | | 1.0 | 2.0 | mA |
| Analog input voltage range | V _{AIN} | AN0 to AN3 | | 4.5 to 5.5 | V _{SS} | | V _{DD} | V |
| Analog port input current | I _{AINH} | | V _{AIN} = V _{DD} | 4.5 to 5.5 | | | 1 | μA |
| | I _{AINL} | | V _{AIN} = V _{SS} | 4.5 to 5.5 | -1 | | | |

(Note 3) Absolute precision excepts quantizing error ($\pm 1/2$ LSB).

7. Current Drain Characteristics at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Pins | Conditions | V _{DD} [V] | Ratings | | | Unit |
|---|-------------------------|------------|--|---------------------|---------|------|------|------|
| | | | | | min | typ | max | |
| Current drain during basic operation (Note 4) | I _{DDOP} (1) | DVDD, AVDD | <ul style="list-style-type: none"> FmCF = 12 MHz Ceramic resonator oscillation FmLC = 14.11 MHz LC oscillation System clock : CF oscillation Internal RC oscillation stops. | 4.5 to 5.5 | | 16 | 28 | mA |
| Current drain in HALT mode (Note 4) | I _{DDHALT} (1) | DVDD, AVDD | <ul style="list-style-type: none"> HALT mode FmCF = 12 MHz Ceramic resonator oscillation FmLC = 0 Hz (oscillation stops) System clock : CF oscillation Internal RC oscillation stops. | 4.5 to 5.5 | | 5 | 10 | mA |
| | I _{DDHALT} (2) | DVDD, AVDD | <ul style="list-style-type: none"> HALT mode FmCF = 0 MHz (oscillation stops) FmLC = 0 Hz (oscillation stops) System clock : Internal RC | 4.5 to 5.5 | | 600 | 1200 | μA |
| Current drain in HOLD mode (Note 4) | I _{DDHOLD} | DVDD, AVDD | <ul style="list-style-type: none"> HOLD mode All oscillation stops. | 4.5 to 5.5 | | 0.05 | 20 | μA |

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

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| Oscillation type | Manufacturer | Oscillator | C1 | C2 |
|--------------------------------------|--------------|------------|---------|-------|
| 12 MHz ceramic resonator oscillation | Murata | CSA12.0MTZ | 33 pF | 33 pF |
| | | CST12.0MTW | on chip | |
| | Kyocera | KBR-12.0M | 47 pF | 47 pF |

* Both C1 and C2 must use an K rank ($\pm 10\%$) and an SL characteristics.

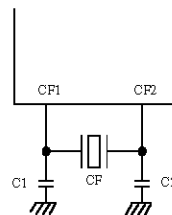
Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)

| Oscillation type | L | C3 | C4 |
|-------------------------|--------------------------------------|-------|-----------------|
| 14.11MHz LC oscillation | 4.7 μ H | 33 pF | 45 pF (Trimmer) |
| | 4.7 μ H $\pm 10\%$ (Variable) | 33 pF | 33 pF |

* See Figure 11,12.

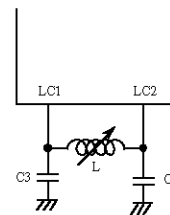
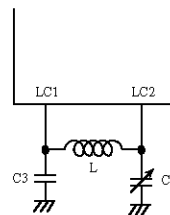
Table 2. LC Oscillation Guaranteed Constant (OSD clock)

- (Notes)
- Since the circuit pattern may affect the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
 - If you use other oscillators than those shown above, we provide no guarantee for the characteristics.
 - Adjust the voltage of monitor point in figure 10 to $1/2V_{DD} \pm 10\%$ by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



Main clock

Figure 1 Ceramic Resonator Oscillation



OSD clock

Figure 2 LC Resonator Oscillation

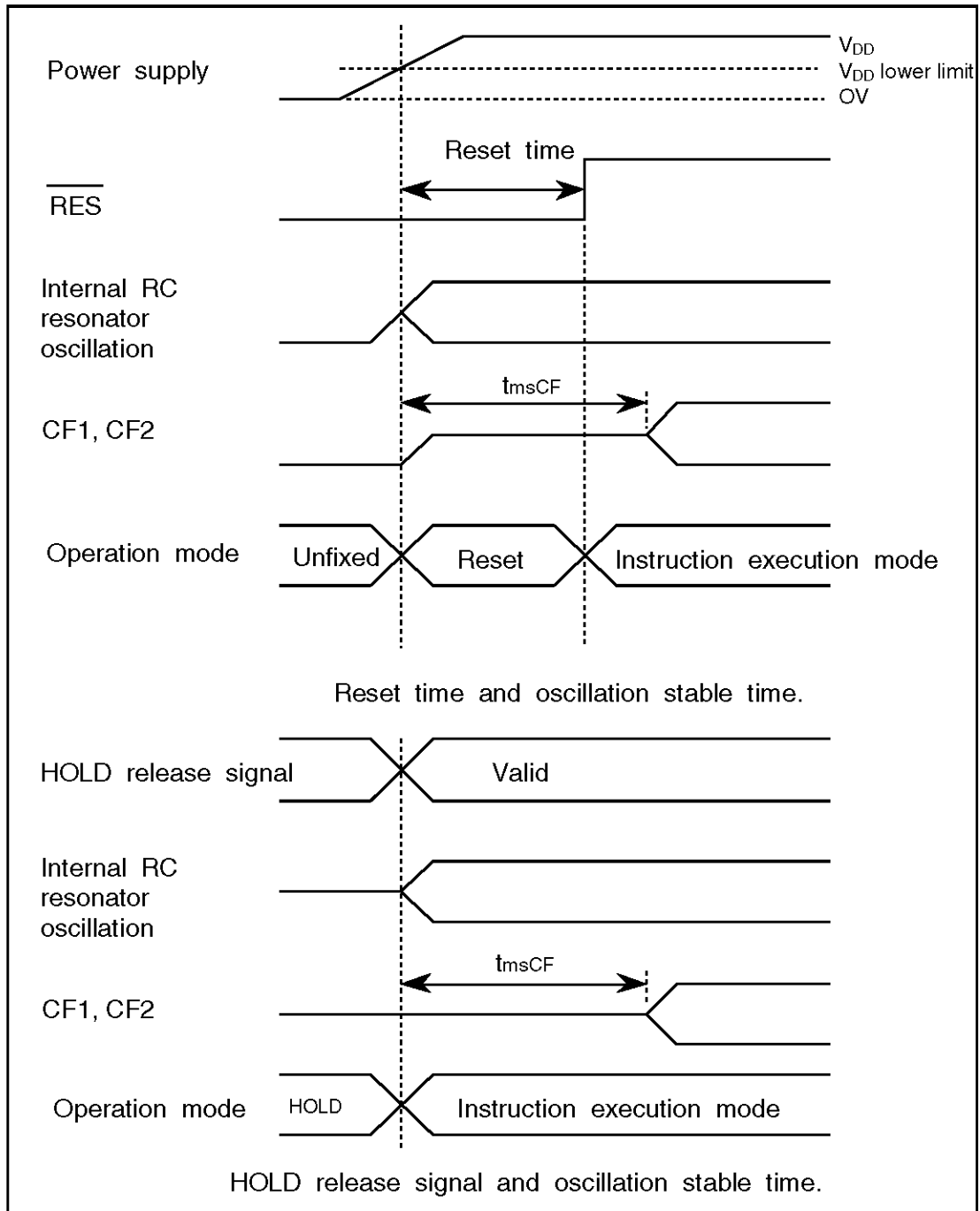


Figure 3 Oscillation Stable Time

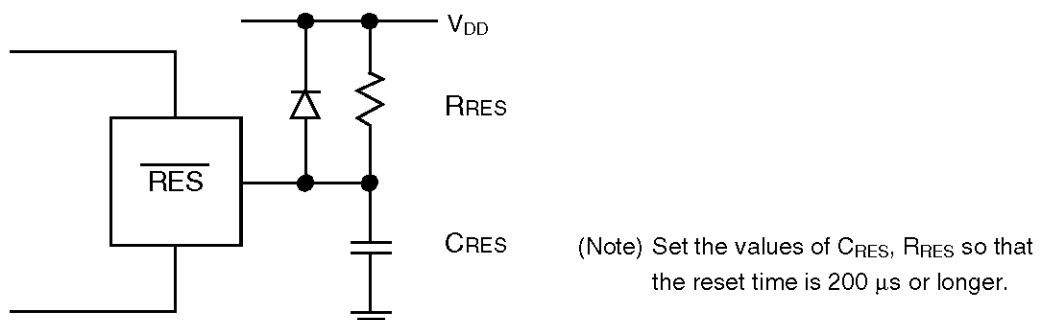


Figure 4 Reset Circuit

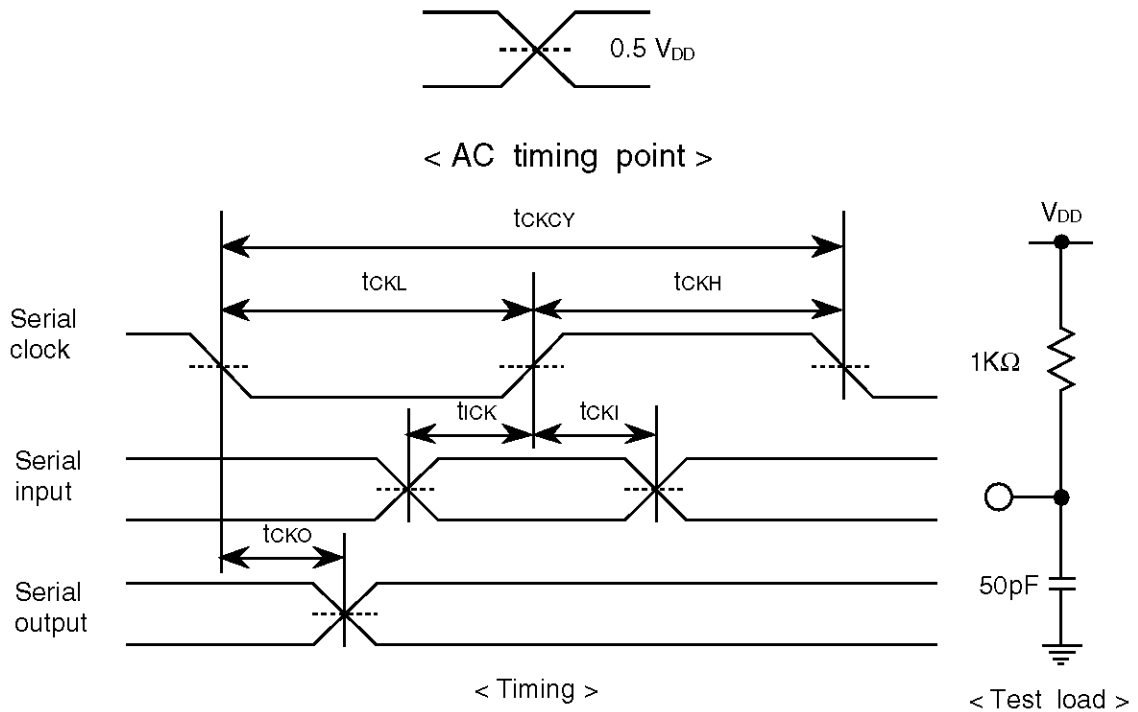


Figure 5 Serial Input/output Test Condition

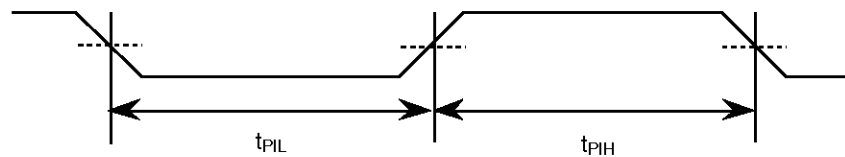


Figure 6 Pulse Input Timing Condition - 1

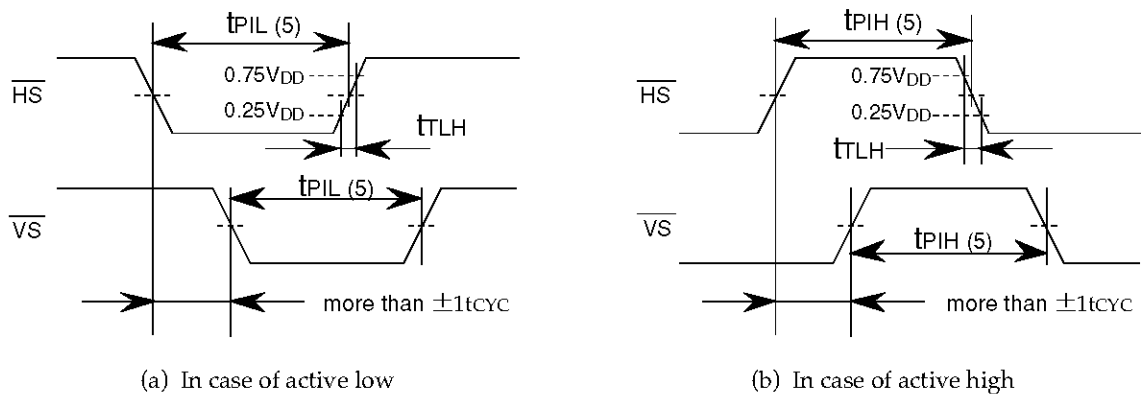


Figure 7 Pulse Input Timing Condition - 2

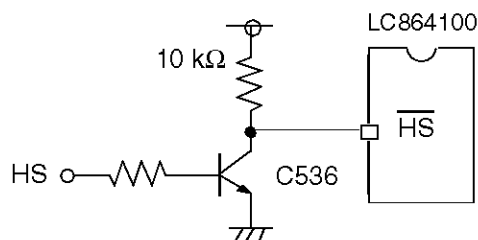


Figure 8 Recommended Interface Circuit

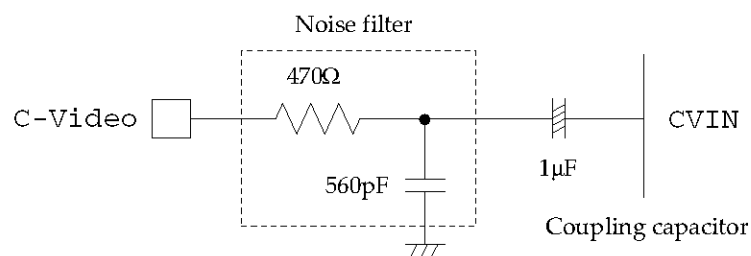


Figure 9 CVIN Recommended Circuit

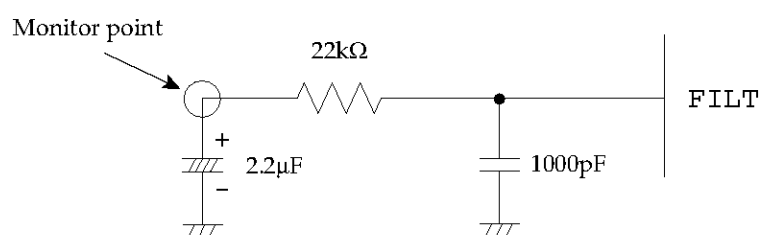


Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected to the FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

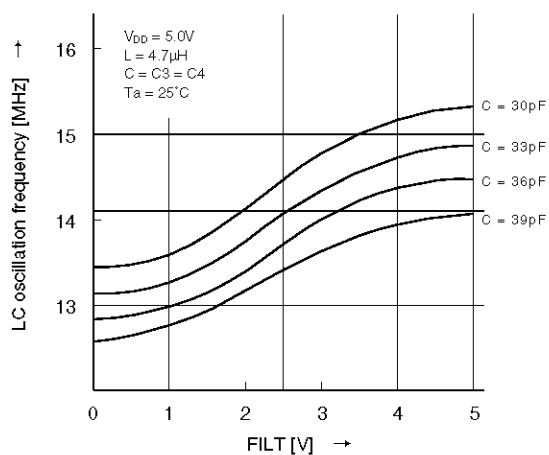


Figure 11 FILT-LC Oscillation Frequency (1)

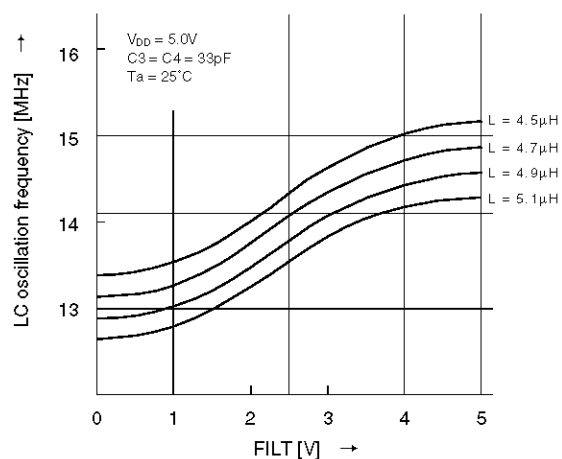


Figure 12 FILT-LC Oscillation Frequency (2)

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