

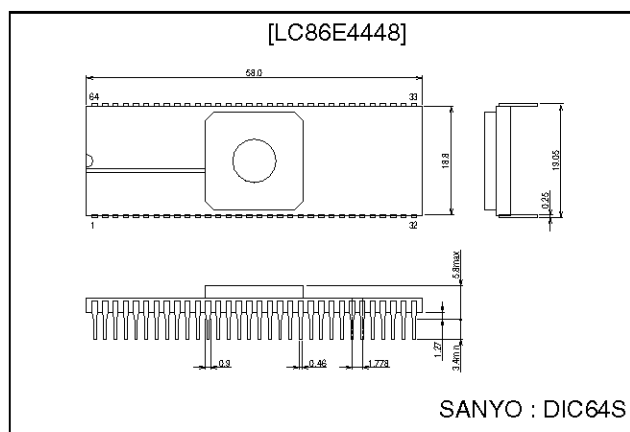
**LC86E4448****UVEPROM built-in 8-bit Single Chip  
Microcontroller****Preliminary****Overview**

The LC86E4448 is a CMOS 8-bit single chip microcontroller with UVEPROM for the LC864400 series.

This microcontroller has the function and pin description of the LC864400 series mask ROM version, and the 48K-byte EPROM. The program data is rewritable. It is suitable for developing programs.

**Package Dimensions**

unit : mm

**3162-DIC64S****Features**

- (1) Option switching by EPROM data  
The option function of the LC864400 series can be specified by the EPROM data.  
The functions of the trial pieces can be evaluated using mass production board.
- (2) Internal EPROM capacity : 49152 bytes (for Program)  
: 8192 x 12-bit (for Character data)
- (3) Internal RAM capacity : 384 bytes  
The LC86E4448 contains 49152-byte EPROM and 386-byte RAM, each size is the maximum capacity of the LC864400 mask-ROM series. Be careful of ROM size.

Mask ROM version	EPROM capacity	RAM capacity
LC864448	49152 bytes	384 bytes
LC864444	45056 bytes	384 bytes
LC864440	40960 bytes	384 bytes
LC864436	36864 bytes	384 bytes
LC864432	32768 bytes	384 bytes
LC864428	28672 bytes	384 bytes
LC864424	24576 bytes	384 bytes
LC864420	20480 bytes	384 bytes

- (4) Operating supply voltage : 4.5 V to 5.5 V
- (5) Instruction cycle time : 0.99  $\mu$ s to 366  $\mu$ s
- (6) Operating temperature : +10°C to +40°C
- (7) The pin compatible with the LC864400 series mask ROM devices
- (8) Applicable mask ROM version : LC864448/LC864444/LC864440/LC864436/LC864432  
LC864428/LC864424/LC864420
- (9) Factory shipment : DIC64S

**SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

**Usage Notes**

At using, take notice of the followings.

- (1) A point of difference the LC86E4448 and the LC864400 series

Item	LC86E4448	LC864448/44/40/36/32/28/24/20
Operation after reset releasing	The option is specified by degrees until 3 ms after going to 'H' level to the reset to the reset terminal. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to 'H' level to the reset terminal.
Operating supply voltage range (V <sub>DD</sub> )	4.5 V to 5.5 V	2.7 V to 5.5 V
Operating temperature range (Topr)	+10 to +40°C	-30 to +70°C
Power dissipation	Refer to 'electrical characteristics' on the semiconductor news.	

The LC86E4448 uses the program memory area of 256 bytes from FF00H to FFFFH to select the options.  
All options of the LC864400 series can be specified.

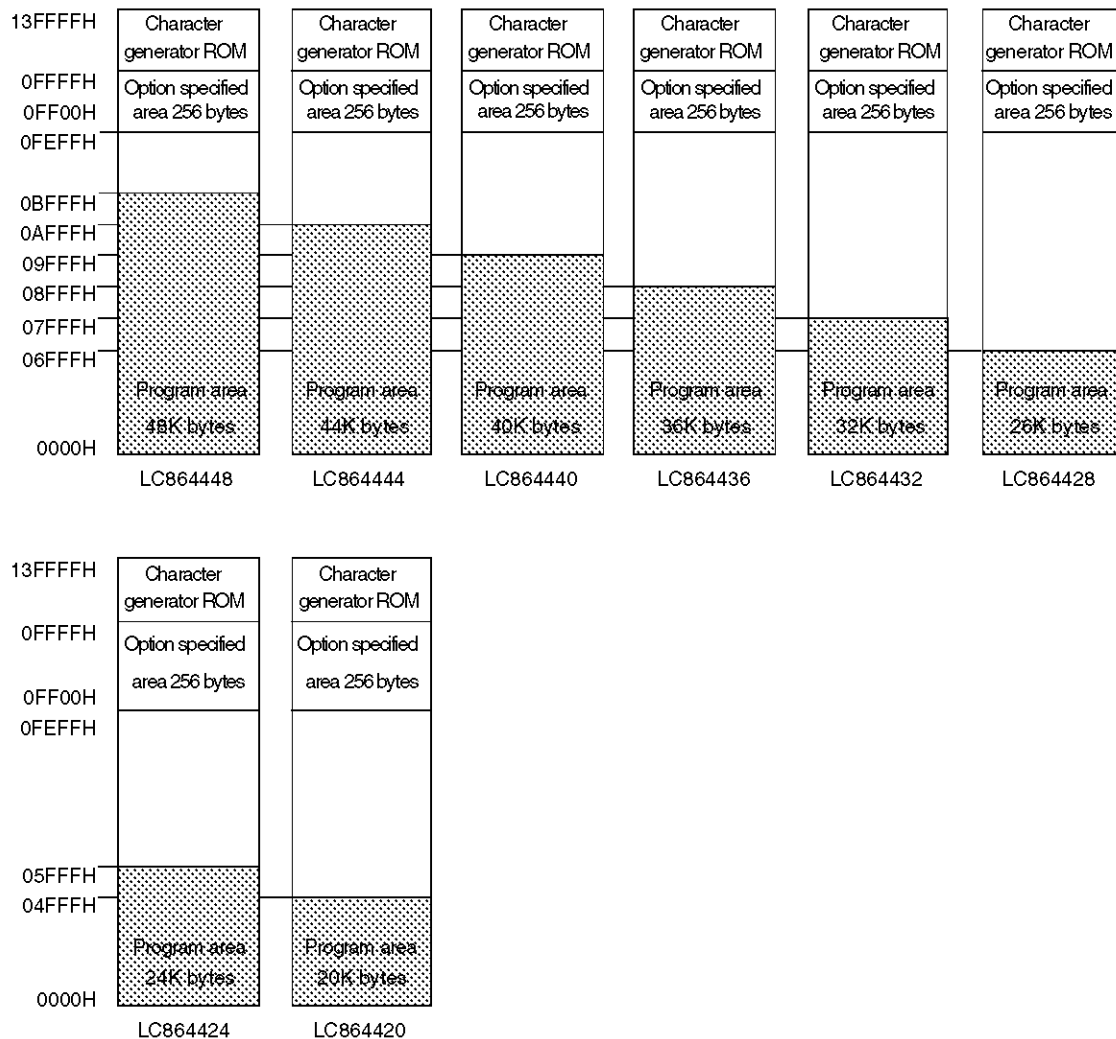
- (2) Option

The option data is written with the option specifying program "SU86K.EXE". The option data is to the program area by the linkage loader "L86K.EXE".

## LC86E4448

### (3) ROM space

The LC86E4448 and LC864400 series use the program memory area of 256 bytes from FF00H to FFFFH to select the options. The program memory capacity of the series is 49152 bytes addressed on 0000H to BFFFH.



## Writing to EPROM

### (1) Preparation

A complete evaluation (EVA) file must be converted to an INTEL-HEX formatted (HEX) file for program to the LC86E4448.  
An EVA2HEX.EXE can convert an EVA file to a HEX file.  
Program the file that converted by the EVA2HEX to the LC86E4448.

### (2) How to write data to EPROM

The LC86E4448 can be programmed by the EPROM programmer with attachment ; W86EP4448D.

- Recommended EPROM programmer

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato Electronics	MODEL1890A

- "27010 (V<sub>p-p</sub> = 12.5 V) Intel high-speed programming" mode should be used. The address must be set to "0 to 13FFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

### (3) How to use the data security function

"Data security" is the function to prevent the EPROM data from being read out.

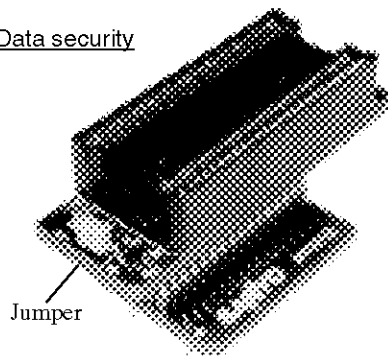
The following is the process in order to execute the data security.

1. Set the jumper of attachment 'ON'.
2. Program again. The the EPROM programmer will display an error. The error indication means normal activity of data security. It does not trouble the EPROM programmer or the LSI.

### Notes

- Data security is not executed when the data of all address have 'FF' at procedure 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at procedure 2 above.
- Set the jumper to 'OFF' after executing the data security.

Data security



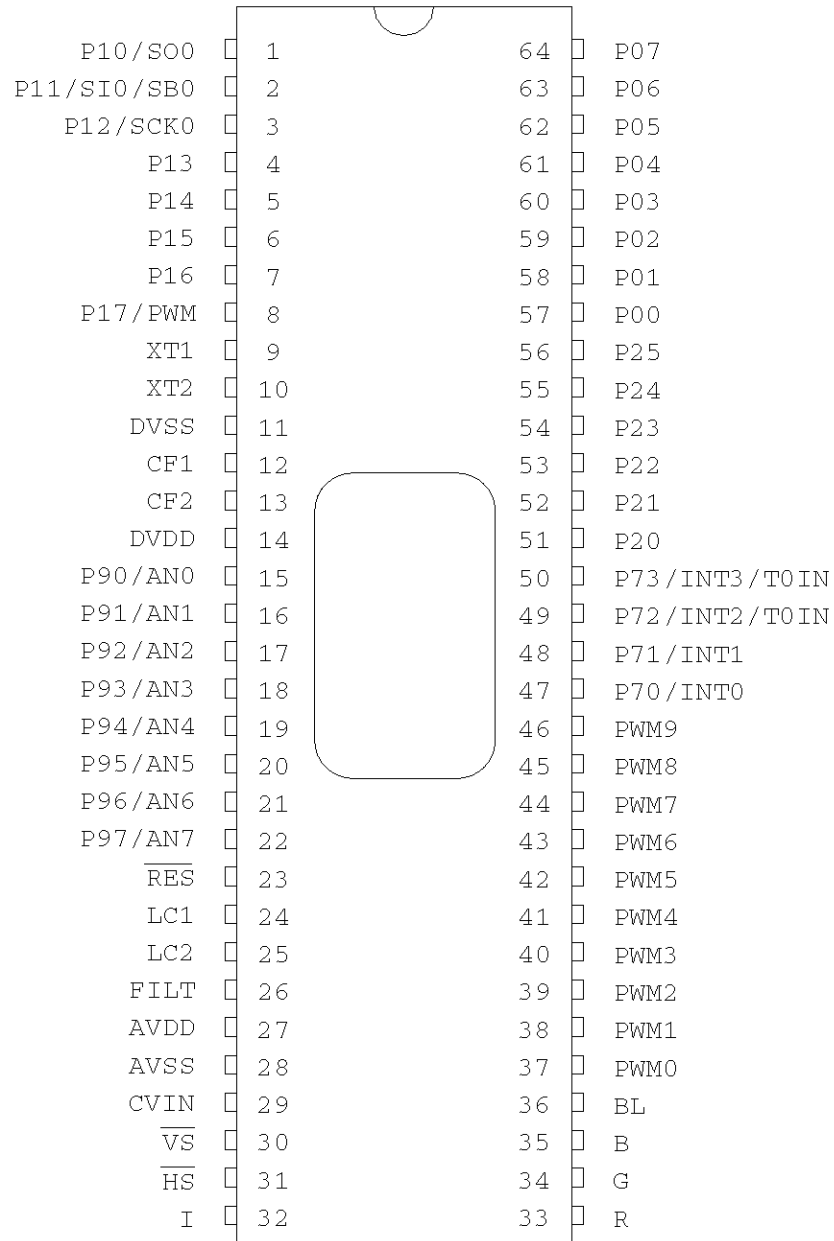
Data security OFF



Pin 1 W86EP4448D

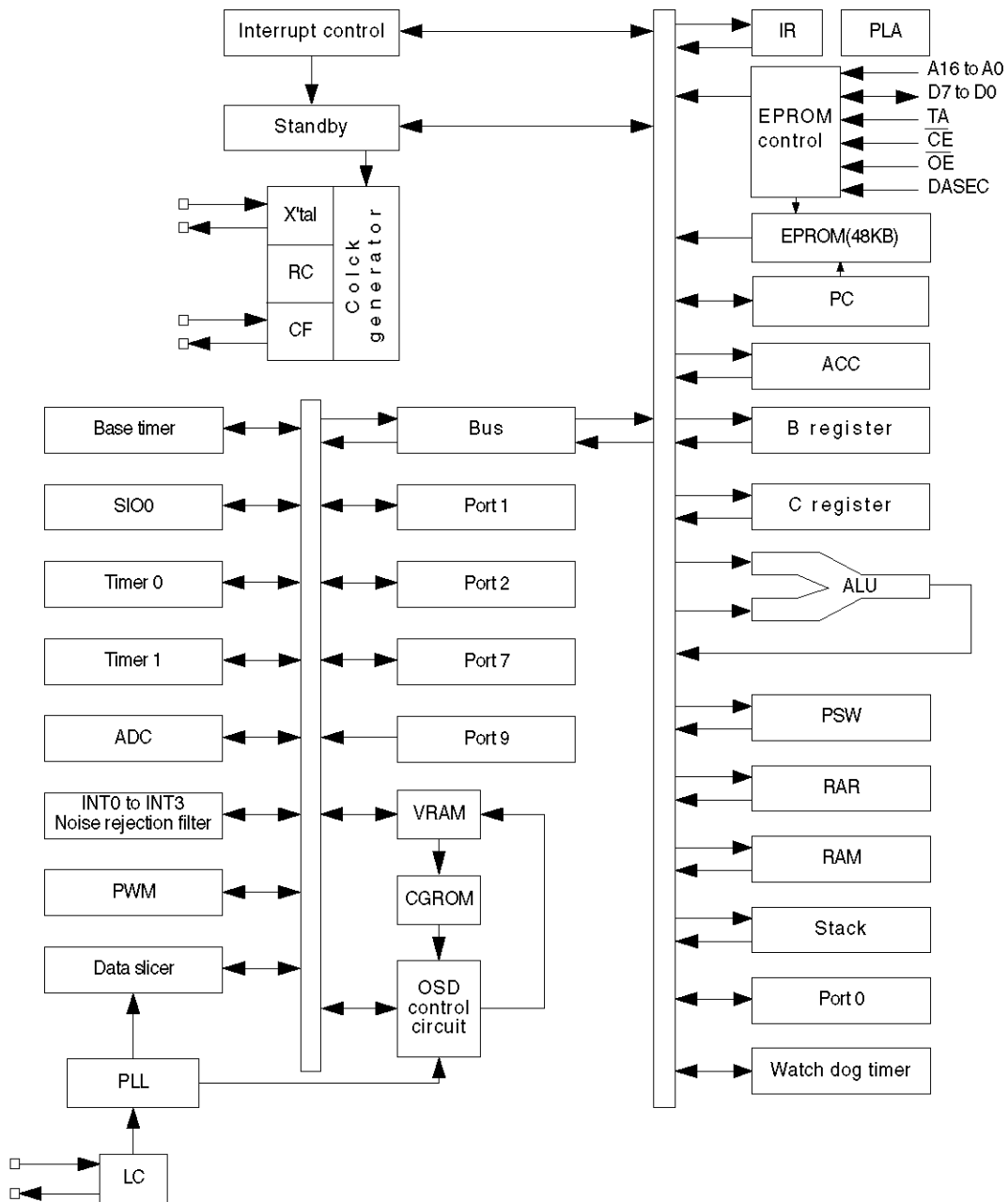
# LC86E4448

## Pin Assignment



Top view

## System Block Diagram



## Pin Description

- Port option can be specified by bit units.
- At port 0, 'Pull-up resistor provided' when specifying CMOS output.  
'Pull-up resistor not provided' when specifying N-ch open drain output.
- At port 1 and 2, 'Programmable pull-up resistor provided' when specifying either CMOS or N-ch open drain output.

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option	PROM mode				
DVSS	11	–	Negative power supply for digital circuit						
XT1	9	I	Input pin for the crystal oscillation						
XT2	10	O	Output pin for the crystal oscillation						
CF1	12	I	Input terminal for ceramic resonator						
CF2	13	O	Output teminal for ceramic resonator						
DVDD	14	–	Positive power supply for digital circuit						
$\overline{\text{RES}}$	23	I	Reset terminal						
LC1	24	I	LC oscillation circuit input terminal						
LC2	25	O	LC oscillation circuit output terminal						
FILT	26	O	Filter terminal for PLL						
AVDD	27	–	Positive power supply for analog circuit						
AVSS	28	–	Negative power supply for analog circuit						
CVIN	29	I	Video signal input terminal						
$\overline{\text{VS}}$	30	I	Vertical synchronization signal input terminal						
$\overline{\text{HS}}$	31	I	Horizontal synchronization signal input terminal						
I	32	O	Image intensity output						
R	33	O	Red (R) output terminal of RGB image output						
G	34	O	Green (G) output terminal of RGB image output		A5 (*1)				
B	35	O	Blue (B) output terminal of RGB image output		A6 (*1)				
BL	36	O	Fast blanking control signal Switch TV image signal and caption/ OSD image signal		A7 (*1)				
PWM0 to PWM9	37 to 46	O	PWM0 to 9 output terminal 15 V withstand		PWM 0 to 8 : A8 to A16 (*1) PWM 9 : "L" fixed				
Port 0 P00 to P07	57 to 64	I/O	8-bit Input/output port Input/output can be specified in nibble units HOLD release input Interrupt input	Pull-up resistor Provided/not provided (in bit units)  Output Format CMOS/Nch-OD (in bit units)					
Port 1 P10 to P17	1 to 8	I/O	8-bit Input/output port Input/output can be specified in bit units. Other function	Output Format CMOS/Nch-OD (in bit units)	D0 to D7 (*2)				
			<table><tr><td>P10</td><td>SIO0 data output</td></tr><tr><td>P11</td><td>SIO0 data input /bus input/output</td></tr><tr><td>P12</td><td>SIO0 clock input/output</td></tr><tr><td>P17</td><td>Timer 1 (PWM) output</td></tr></table>			P10	SIO0 data output	P11	SIO0 data input /bus input/output
P10	SIO0 data output								
P11	SIO0 data input /bus input/output								
P12	SIO0 clock input/output								
P17	Timer 1 (PWM) output								
Port 2 P20 to P25	51 to 56	I/O	6-bit Input/output port Input/output can be specified in bit units.	Output Format CMOS/Nch-OD (in bit units)					

## LC86E4448

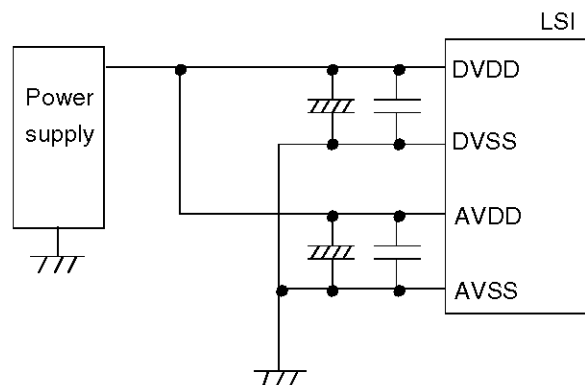
Pin name	Pin No.	I/O	Function description			Option		PROM mode					
Port 7	47 48 to 50	I/O  I	4-bit input port			Pull-up resistor provided/  not provided (in bit units)		P70 : VPP (*3) P71 : DASEC (*4)  P72 : $\overline{OE}$ (*5) P73 : $\overline{CE}$ (*6)					
P70			Other function										
P71 to P73			<table border="1"><tr><td>P70</td><td>INT0 input/HOLD release input/ Nch-transistor output for watchdog timer</td></tr><tr><td>P71</td><td>INT1 input/HOLD release input</td></tr><tr><td>P72</td><td>INT2 input/timer 0 event input</td></tr><tr><td>P73</td><td>INT3 input (noise rejection filter attached input/timer 0 event input</td></tr></table>							P70	INT0 input/HOLD release input/ Nch-transistor output for watchdog timer	P71	INT1 input/HOLD release input
P70			INT0 input/HOLD release input/ Nch-transistor output for watchdog timer										
P71			INT1 input/HOLD release input										
P72			INT2 input/timer 0 event input										
P73			INT3 input (noise rejection filter attached input/timer 0 event input										
	Interrupt receiver format vector address												
		Rise	Fall	Rise/Fall	H level	L level	Vector						
	INT0	enable	enable	disable	enable	enable	03H						
	INT1	enable	enable	disable	enable	enable	0BH						
	INT2	enable	enable	enable	disable	disable	13H						
	INT3	enable	enable	enable	disable	disable	1BH						
Port 9	15 to 22	I	8-bit input port						P90 to P93 :				
P90 to P97			Other function A/D converter input port (8 lines)						A0 to A3 (*1)				

- \*1 An → Address input
- \*2 Data I/O
- \*3 Power for programming
- \*4 Memory select input/output for data security
- \*5 Output Enable input
- \*6 Chip Enable input

- Port status during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1,2	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

\*AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect them like the following figure to reduce the mutual noise influence.





## Specifications

### 1. Absolute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V

Parameter		Symbol	Pins	Conditions	Ratings			Unit	
					V <sub>DD</sub> [V]	min	typ		max
Supply voltage		V <sub>DD</sub> max	DVDD, AVDD	DVDD = AVDD		−0.3		+7.0	V
Input voltage		V <sub>I</sub> (1)	• P 71,72,73 • Port 9 • $\overline{RES}$ , $\overline{HS}$ , $\overline{VS}$ , CVIN			−0.3		V <sub>DD</sub> +0.3	
Output voltage		V <sub>O</sub> (1)	R, G, B, BL, I, FILT			−0.3		V <sub>DD</sub> +0.3	
		V <sub>O</sub> (2)	PWM0 to PWM9			−0.3		+15	
Input/output voltage		V <sub>IO</sub> (1)	Ports 0, 1, 2, P70			−0.3		V <sub>DD</sub> +0.3	
High-level output current	Peak output current	I <sub>OPH</sub> (1)	Ports 0, 1, 2	• Pull-up MOS transistor output • At each pin		−2			mA
		I <sub>OPH</sub> (2)	Ports 0, 1, 2	• CMOS output • At each pin		−4			
		I <sub>OPH</sub> (3)	R, G, B, BL, I	• CMOS output • At each pin		−5			
	Total output current	ΣI <sub>OA</sub> H(1)	Port 1	The total of all pins		−10			
		ΣI <sub>OA</sub> H(2)	Ports 0, 2	The total of all pins		−10			
		ΣI <sub>OA</sub> H(3)	R, G, B, BL, I	The total of all pins		−15			
Low-level output current	Peak output current	I <sub>OPL</sub> (1)	Ports 0, 1, 2	At each pin				20	
		I <sub>OPL</sub> (2)	P70	At each pin				30	
		I <sub>OPL</sub> (3)	• R, G, B, BL, I • PWM0 to PWM9	At each pin				5	
	Total output current	ΣI <sub>OAL</sub> (1)	Ports 0, 2	The total of all pins				40	
		ΣI <sub>OAL</sub> (2)	Port 1, P70	The total of all pins				40	
		ΣI <sub>OAL</sub> (3)	R, G, B, BL, I	The total of all pins				15	
		ΣI <sub>OAL</sub> (4)	PWM0 to PWM9	The total of all pins				30	
Maximum power dissipation		Pd max	DIC64S	Ta = +10 to +40°C				720	mW
Operating temperature range		Topr				+10		+40	°C
Storage temperature range		Tstg				−55		+150	

\* DVSS and AVSS must be supplied the same voltage, V<sub>SS</sub>.  
 DVDD and AVDD must be supplied the same voltage, V<sub>DD</sub>.

V<sub>SS</sub> = DVSS = AVSS  
 V<sub>DD</sub> = DVDD = AVDD

2. Recommended Operating Range at Ta = +10°C to +40°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Operating supply voltage range	V <sub>DD</sub> (1)	DVDD, AVDD	0.97 μs ≤ tCYC ≤ 1.02 μs		4.5		5.5	V
	V <sub>DD</sub> (2)		0.97 μs ≤ tCYC ≤ 400 μs		4.5		5.5	
Hold voltage	V <sub>HD</sub>	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high-level voltage	V <sub>IH</sub> (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	• Ports 1, 2 (Schmitt) • P72, 73 • HS, VS	Output disable	4.5 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (4)	P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V <sub>DD</sub> −0.5		V <sub>DD</sub>	
	V <sub>IH</sub> (5)	Port 9 port input		4.5 to 5.5	0.7V <sub>DD</sub>		V <sub>DD</sub>	
Input low-level voltage	V <sub>IL</sub> (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	• Ports 1, 2 (Schmitt) • P72, 73 • HS, VS • Port 9	Output disable	4.5 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
	V <sub>IL</sub> (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
	V <sub>IL</sub> (4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V <sub>SS</sub>		0.6V <sub>DD</sub>	
	V <sub>IL</sub> (5)	Port 9 port input		4.5 to 5.5	V <sub>SS</sub>		0.3V <sub>DD</sub>	
CV <sub>IN</sub> input amplitude	V <sub>CVIN</sub>	CVIN		5.0	1Vp-p −3dB	1Vp-p	1Vp-p +3dB	Vp-p *
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.97	1	1.02	μs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.97		400	

\* Vp-p : Peak-to-peak voltage

## LC86E4448

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V <sub>DD</sub> [V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmCF(2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.84	12.08	12.32	
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.4	0.8	3.0	
	FsXtal	XT1, XT2	32.768 kHz (crystal resonator oscillation) Refer to Figure 3.	4.5 to 5.5		32.768		kHz
Oscillation stable time period (Note 2)	tmsCF(1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 4.	4.5 to 5.5		0.02	0.2	ms
	tmsCF(2)		12 MHz (ceramic resonator oscillation) Refer to Figure 4.	4.5 to 5.5		0.02	0.2	
	tss Xtal	XT1, XT2	32.768 kHz (crystal resonator oscillation) Refer to Figure 4.	4.5 to 5.5		1.0	5.0	s

(Note 1) Refer to table 1, 2 and 3 for oscillation constant.

(Note 2) The oscillation stable time period refers to the time it takes to oscillate stably after the following conditions.

1. Applying the first supply voltage.
2. Release of the HOLD mode.
3. Release of the stopping of the main-clock oscillation. (Refer to Figure 4)

3. Electrical Characteristics at Ta = +10°C to +40°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V <sub>DD</sub> [V]	min	typ	max	
Input high current	I <sub>IH</sub> (1)	• Ports 1, 2 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • V <sub>IN</sub> = V <sub>DD</sub> (including the off-leak current of the output transistor)	4.5 to 5.5			1	μA
	I <sub>IH</sub> (2)	• Port 7 without pull-up MOS transistor • Port 9 • $\overline{\text{RES}}$ • $\overline{\text{HS}}$ , $\overline{\text{VS}}$	V <sub>IN</sub> = V <sub>DD</sub>	4.5 to 5.5			1	
Input low current	I <sub>IL</sub> (1)	• Ports 1, 2 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • V <sub>IN</sub> = V <sub>SS</sub> (including the off-leak current of the output transistor)	4.5 to 5.5	−1			
	I <sub>IL</sub> (2)	• Port 7 without pull-up MOS transistor • Port 9	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 5.5	−1			
	I <sub>IL</sub> (3)	• $\overline{\text{RES}}$ • $\overline{\text{HS}}$ , $\overline{\text{VS}}$	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 5.5	−1			
Output high voltage	V <sub>OH</sub> (1)	CMOS output of Ports 0, 1, 2	I <sub>OH</sub> = −1.0 mA	4.5 to 5.5	V <sub>DD</sub> −1			V
	V <sub>OH</sub> (2)	R, G, B, BL, I	I <sub>OH</sub> = −0.1 mA	4.5 to 5.5	V <sub>DD</sub> −0.5			
Output low voltage	V <sub>OL</sub> (1)	Ports 0, 1, 2	I <sub>OL</sub> = 10 mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (2)	Ports 0, 1, 2	• I <sub>OL</sub> = 1.6 mA • The total current of the ports 0, 1 is 40 mA or less.	4.5 to 5.5			0.4	
	V <sub>OL</sub> (3)	• R, G, B, BL, I • PWM0 to PWM9	• I <sub>OL</sub> = 3.0 mA • The current of any unmeasured pin is 3 mA or less.	4.5 to 5.5			0.4	
	V <sub>OL</sub> (4)	P70	I <sub>OL</sub> = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	R <sub>pu</sub>	• Ports 0, 1, 2 • Port 7	V <sub>OH</sub> = 0.9 V <sub>DD</sub>	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I <sub>OFF</sub>	PWM0 to PWM9	V <sub>OUT</sub> = 13.5 V	4.5 to 5.5			5	μA
Hysteresis voltage	V <sub>HIS</sub>	• Ports 0, 1, 2 • Port 7 • $\overline{\text{RES}}$ • $\overline{\text{HS}}$ , $\overline{\text{VS}}$	Output disable	4.5 to 5.5		0.1V <sub>DD</sub>		V

## LC86E4448

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Input clamp voltage	V <sub>CLMP</sub>	CVIN		5.0	2.3	2.5	2.7	V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"><li>• f = 1 MHz</li><li>• Unmeasured input pins are set to V<sub>SS</sub> level.</li><li>• Ta = 25°C</li></ul>	4.5 to 5.5		10		pF

### 4. Serial Input/output Characteristics at Ta = +10°C to +40°C , V<sub>SS</sub> = 0 V

Parameter			Symbol	Pins	Conditions	V <sub>DD</sub> [V]	Ratings			Unit
							min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	• SCK0 • SCLK0	Refer to Figure 6.	4.5 to 5.5	2			tCYC
		Low-level pulse width	tCKL(1)				1			
		High-level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	• SCK0 • SCLK0	• Use a pull-up resistor (1 kΩ) when open drain output • Refer to Figure 6.	4.5 to 5.5	2			
		Low-level pulse width	tCKL(2)					1/2tCKCY		
		High-level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time	tICK	SI0	• Data set-up to SCK0 rising • Data hold from SCK0 rising • Refer to Figure 6.	4.5 to 5.5	0.1			μs	
	Data hold time	tCKI				0.1				
Serial output	Output delay time (External serial clock)	tCKO(1)	SO0	• Use a pull-up resistor (1 kΩ) when open drain output	4.5 to 5.5			7/12tCYC +0.2		
	Output delay time (External serial clock)	tCKO(2)		• Data set-up to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 6.	4.5 to 5.5			1/3tCYC +0.2		

**5. Pulse Input Conditions at Ta = +10°C to +40°C, V<sub>SS</sub> = 0 V**

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V <sub>DD</sub> [V]	min	typ	max	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0,INT1 • INT2/T0IN	• Interrupt acceptable • Timer/counter 0 pulse countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is set to 1/1)	• Interrupt acceptable • Timer/counter 0 pulse countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is set to 1/16)	• Interrupt acceptable • Timer/counter 0 pulse countable	4.5 to 5.5	32			
	tPIL(4)	RES	Reset acceptable	4.5 to 5.5	200			μs
	tPIH(5) tPIL(5)	HS, VS	Display position controllable Each active edge of HS, VS must be more than 1tCYC. Refer to Figure 8.	4.5 to 5.5	10			tCYC
Rise/fall time	tTHL tTLH	HS	Refer to Figure 8.	4.5 to 5.5			500	ns
Horizontal pull-in range	FH	HS	The monitor point in figure 11 is 1/2 V <sub>DD</sub> .	4.5 to 5.5	15.23	15.73	16.23	kHz

**6. A/D Converter Characteristics at Ta = +10°C to +40°C, V<sub>SS</sub> = 0 V**

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Resolution				4.5 to 5.5		5		bit
Absolute precision			(Note 3)	4.5 to 5.5		±1/4	±3/4	LSB
Conversion time	tCAD	From Vref selection to when the result is produced	1 bit conversion time = 2tCYC	4.5 to 5.5		2		μs
Reference current	I <sub>REF</sub>		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	V <sub>AIN</sub>	AN0 to AN7		4.5 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	V
Analog port input current	I <sub>AINH</sub>		V <sub>AIN</sub> = V <sub>DD</sub>	4.5 to 5.5			1	μA
	I <sub>AINL</sub>		V <sub>AIN</sub> = V <sub>SS</sub>	4.5 to 5.5	−1			

(Note 3) Absolute precision excepts quantizing error (±1/2 LSB).

7. Current Drain Characteristics at Ta = +10°C to +40°C , V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Current drain during basic operation (Note 4)	I <sub>DDOP</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"><li>FmCF = 12 MHz or FmCF = 12.08 MHz when ceramic resonator oscillation</li><li>FsXtal = 32.768 kHz when crystal oscillation</li><li>FmLC = 14.11 MHz when LC oscillation</li><li>System clock : CF oscillation</li><li>Internal RC oscillation stops</li></ul>	4.5 to 5.5		25	38	mA
	I <sub>DDOP</sub> (2)		<ul style="list-style-type: none"><li>FmCF = 0 Hz (when oscillation stops)</li><li>FmLC = 0 Hz (when oscillation stops)</li><li>FsXtal = 32.768 kHz when crystal oscillation</li><li>System clock : LC oscillation</li><li>Internal RC oscillation stops</li></ul>	4.5 to 5.5		8	16	
Current drain in halt mode (Note 4)	I <sub>DDHALT</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"><li>HALT mode</li><li>FmCF = 12 MHz or FmCF = 12.08 MHz when eramic resonator oscillation</li><li>FmLC = 0 Hz (when oscillation stops)</li><li>FsXtal = 32.768 kHz when crystal oscillation</li><li>System clock : CF oscillation</li><li>Internal RC oscillation stops</li></ul>	4.5 to 5.5		5	10	mA
	I <sub>DDHALT</sub> (2)	DVDD, AVDD	<ul style="list-style-type: none"><li>HALT mode</li><li>FmCF = 0 Hz (when oscillation stops)</li><li>FmLC = 0 Hz (when oscillation stops)</li><li>FsXtal = 32.768 kHz when crystal oscillation</li><li>System clock : Internal RC</li></ul>	4.5 to 5.5		400	1600	μA
	I <sub>DDHALT</sub> (3)	DVDD, AVDD	<ul style="list-style-type: none"><li>FmCF = 0 Hz (when oscillation stops)</li><li>FmLC = 0 Hz (when oscillation stops)</li><li>FsXtal = 32.768 kHz when crystal oscillation</li><li>System clock : LC oscillation</li><li>Internal RC oscillation stops</li></ul>	4.5 to 5.5		25	100	
Current drain in hold mode (Note 4)	I <sub>DDHOLD</sub>	DVDD, AVDD	<ul style="list-style-type: none"><li>HOLD mode</li><li>All oscillation stop</li></ul>	4.5 to 5.5		0.05	30	μA

(Note 4) The currents into the output transistors and the pull-up MOS transistors are ignored.

# LC86E4448

Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ021	33 pF	33 pF
		CST12.0MTW021	on chip	
	Kyocera	KBR-12.08M	33 pF	33 pF

\* Both C1 and C2 must use K rank ( $\pm 10\%$ ) and SL characteristics.

**Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)**

Oscillation type	L	C3	C4
14.11MHz LC oscillation	4.7 $\mu$ H	33 pF	45 pF (Trimmer)
	4.7 $\mu$ H $\pm 10\%$ (Variable)	33 pF	33 pF

\* See Figures 12 and 13.

**Table 2. LC Oscillation Guaranteed Constant (OSD clock)**

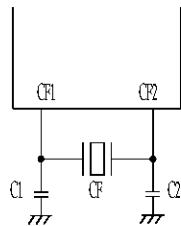
Oscillation type	Supplier	Oscillator	C5	C6	Rd
32.768 MHz crystal oscillation	Seiko Epson	C-002RX	10 pF	10 pF	0 $\Omega$

\* Both C5 and C6 must use J rank ( $\pm 5\%$ ) and CH characteristics.

For the application which does not require the accurate oscillation, use K rank ( $\pm 10\%$ ) with SL characteristics.

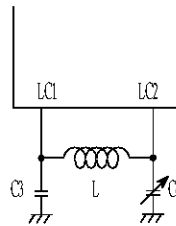
**Table 3. Crystal Oscillation Guaranteed Constant (sub-clock)**

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
  - If you use other oscillators herein, we provide no guarantee for the characteristics.
  - Adjust the voltage of monitor point in Figure 11 to  $1/2V_{DD} \pm 10\%$  by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



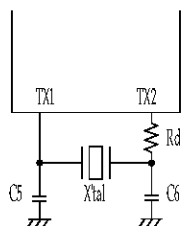
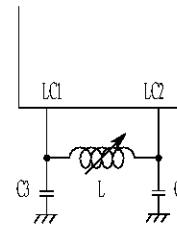
main clock

**Figure 1 Ceramic Resonator Oscillation**



OSD clock

**Figure 2 LC Resonator Oscillation**



main clock

**Figure 3 Crystal Resonator Oscillation**



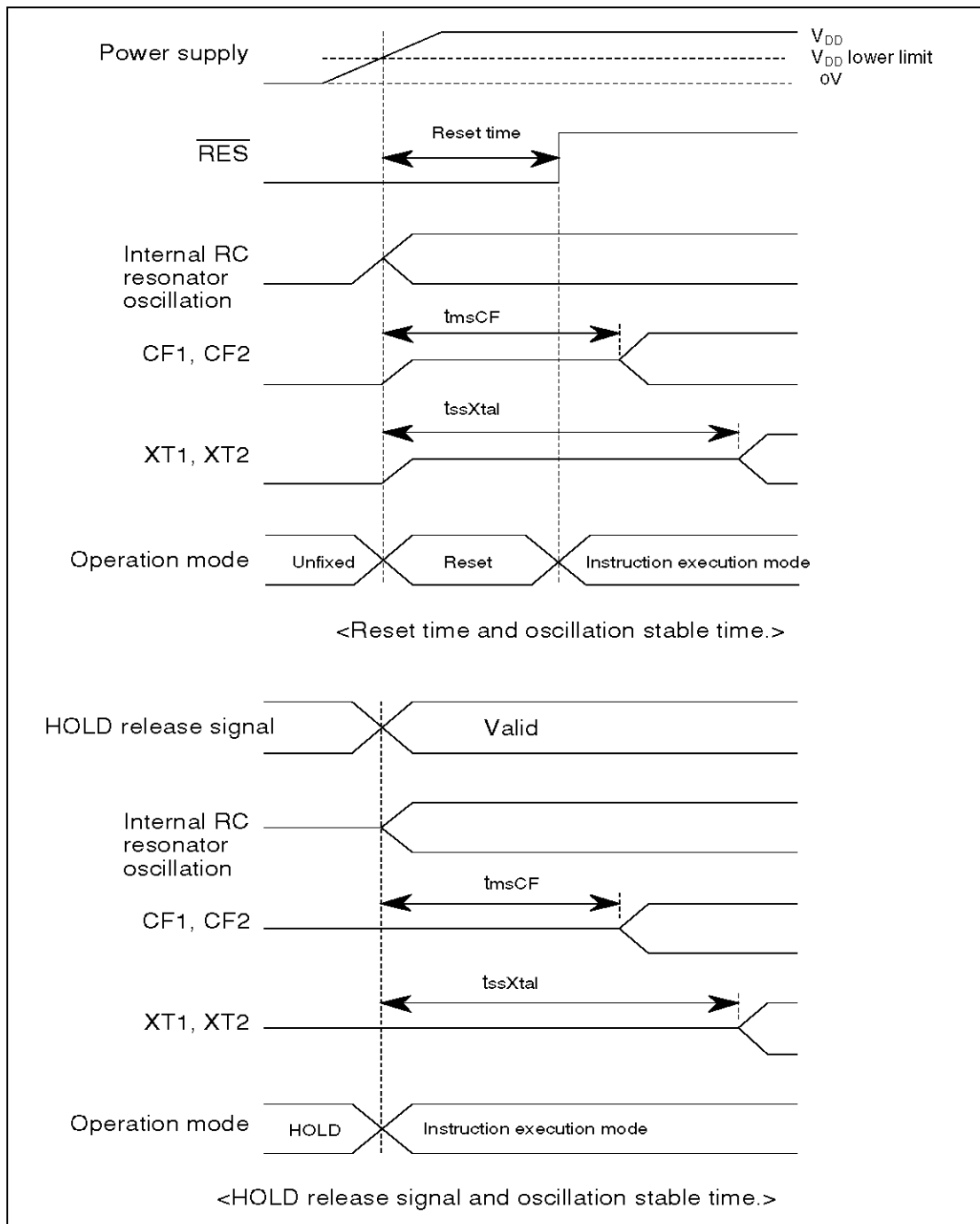


Figure 4 Oscillation Stable Time

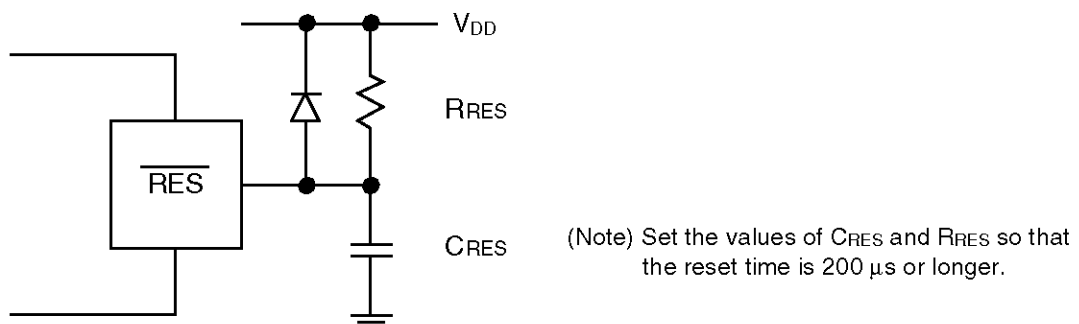


Figure 5 Reset Circuit

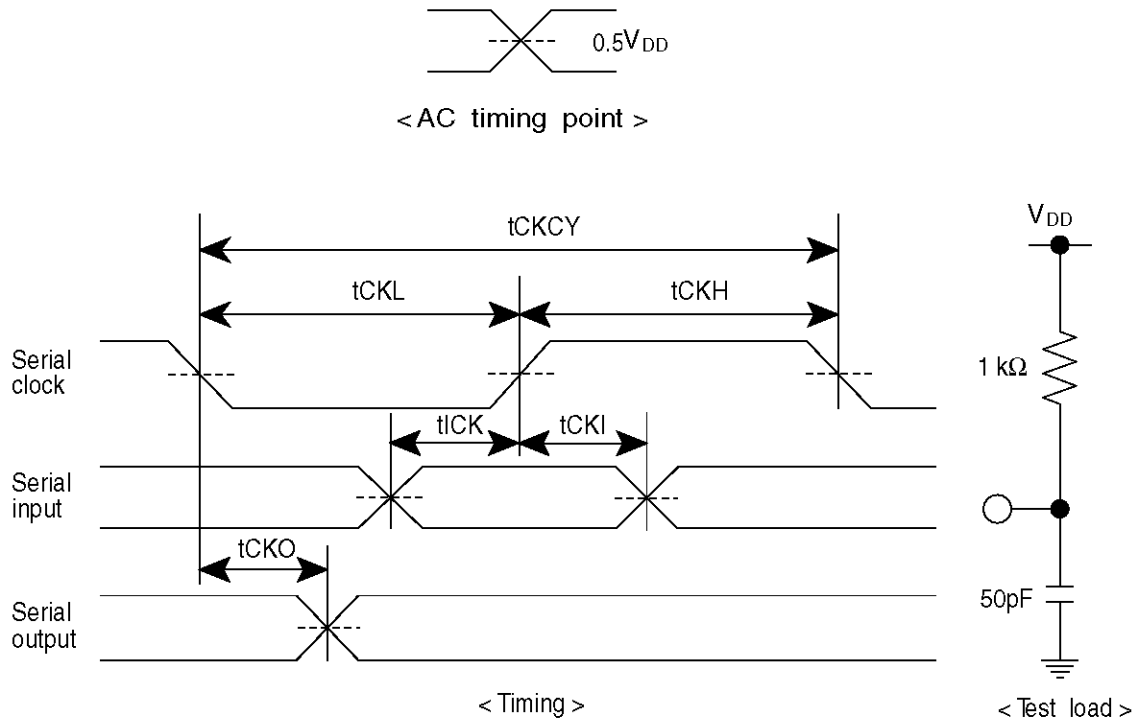


Figure 6 Serial Input/output Test Condition

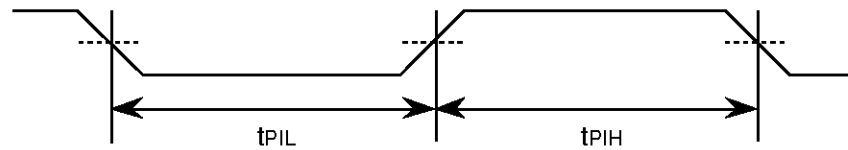


Figure 7 Pulse Input Timing Condition - 1

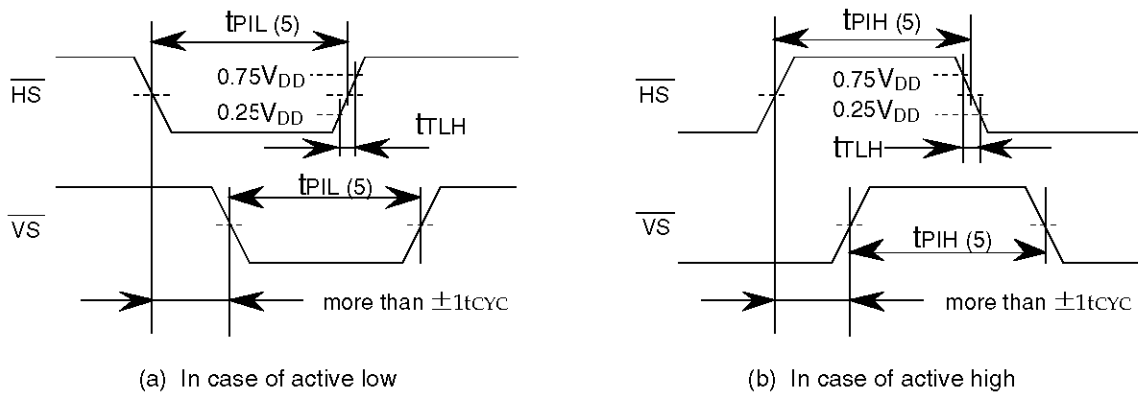


Figure 8 Pulse Input Timing Condition - 2

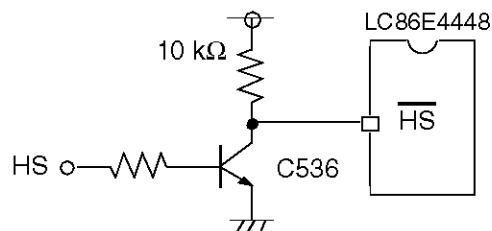


Figure 9 Recommended Interface Circuit

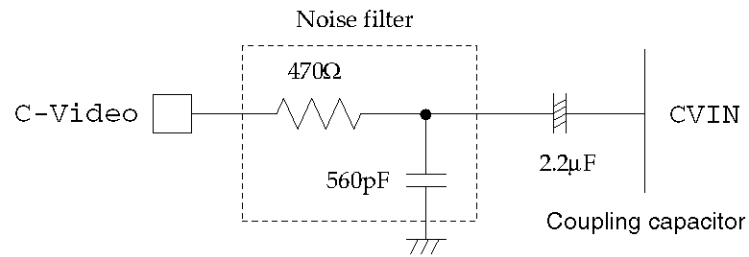


Figure 10 CVIN Recommended Circuit

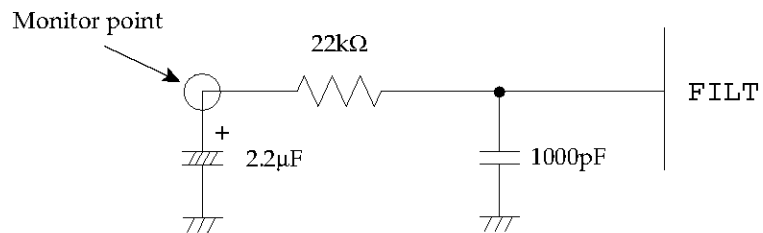


Figure 11 FILT Recommended Circuit

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

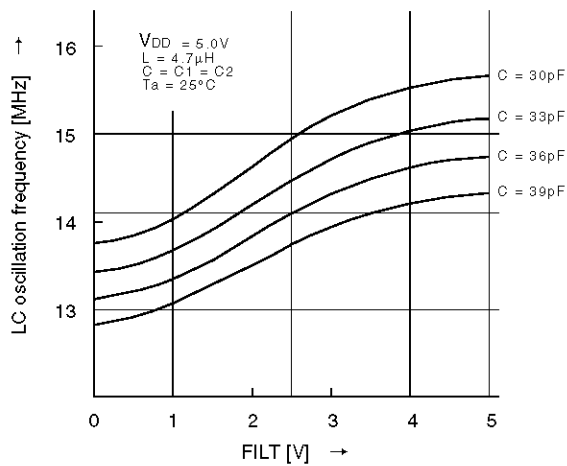


Figure 12 FILT-LC Oscillation Frequency (1)

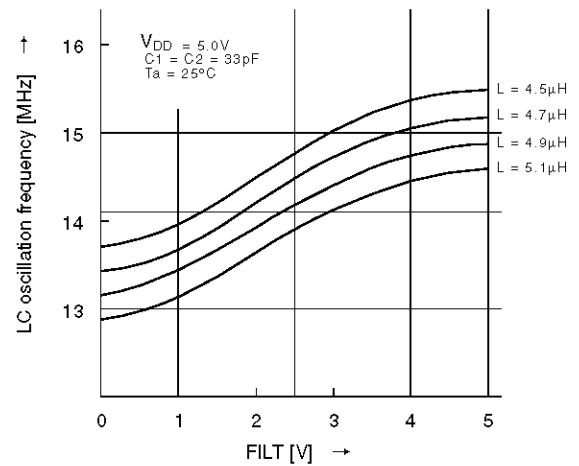


Figure 13 FILT-LC Oscillation Frequency (2)

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of February, 1998. Specifications and information herein are subject to change without notice.

---