



LC876572A/64A

8-Bit Single Chip Microcontroller with 72/64 KB ROM and 2048-Byte RAM On Chip

Preliminary

Overview

The LC876572A and LC876564A are 8 bit single chip microcontrollers with the following on-chip functional blocks :

- CPU: operable at a minimum bus cycle time of 100 ns
- On-chip ROM Maximum Capacity :

| | |
|-----------|-----------|
| LC876572A | 72K bytes |
| LC876564A | 64K bytes |
- On-chip RAM: 2048 bytes
- VFD automatic display controller / driver
- 16 bit timer / counter (can be divided into two 8 bit timers)
- 16 bit timer / PWM (can be divided into two 8 bit timers)
- timer for use as date / time clock
- synchronous serial I/O port (with automatic block transmit / receive function)
- asynchronous / synchronous serial I/O port
- 12-channel \times 8-bit AD converter
- Weak signal detector
- 15-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

- (1) Read-Only Memory (ROM): LC876572A 73728 × 8 bits
 LC876564A 65536 × 8 bits
- (2) Random Access Memory (RAM): LC876572A/64A 2048 × 9 bits
- (3) Minimum Bus Cycle Time: 100 ns (10 MHz)

Note: The bus cycle time indicates ROM read time.

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(4) Minimum Instruction Cycle Time: 300 ns (10MHz)

(5) Ports

- Input/output ports
 - Data direction programmable for each bit individually : 20 (P1n, P70 to P73, P8n)
- 15V withstand input/output ports
 - Data direction programmable in nibble units : 8 (P0n)
 - (When N-channel open drain output is selected, data can be input in bit units.)
 - Data direction programmable for each bit individually : 8 (P3n)
- Input ports : 2 (XT1,XT2)
- VFD output ports
 - Large current outputs for digits : 9 (S0 / T0 to S8 / T8)
 - Large current outputs for digits / segments : 7 (S9 / T9 to S15 / T15)
 - digit / segment outputs : 8 (S16 to S23)
 - segment outputs : 28 (S24 to S51)
- Other functions
 - Input/output ports : 12 (PFn, PG0 to 3)
 - Input ports : 24 (PCn, PDn, PEn)
- Oscillator pins : 2 (CF1,CF2)
- Reset pin : 1 (RES#)
- Power supply : 6 (VSS1 to 2, VDD1 to 4)
- VFD power supply : 1 (VP)

(6) VFD automatic display controller

- Programmable segment/digit output pattern
 - Output can be switched between digit/segment waveform output (pins 9?u24 can be used for output of digit waveforms.
 - parallel-drive available for large current VFD.
- 16-step dimmer function available

(7) Weak signal detection (MIC signals etc)

- Counts pulses with width greater than a preset value
- 2 bit counter

(8) Timers

- Timer 0: 16 bit timer / counter with capture register
 - Mode 0: 2 channel 8-bit timer with programmable 8 bit prescaler and 8 bit capture register
 - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit Counter with 8-bit capture register
 - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
 - Mode 3: 16 bit counter with 16 bit capture register
- Timer 1: PWM / 16 bit timer toggle output
 - Mode 0: 2 channel 8 bit timer (with toggle output)
 - Mode 1: 2 channel 8 bit PWM
 - Mode 2: 16 bit timer (with toggle output) Toggle output also possible using lower order 8 bits.
 - Mode 3: 16 bit timer (with toggle output) Lower order 8 bits can be used as PWM output.
- Base Timer
 - 1) The clock signal can be selected from any of the following :
 - Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0
 - 2) Interrupts can be selected to occur at one of five different times.

(9) Serial-interface

- SIO 0: 8 bit synchronous serial Interface
 - 1) LSB first / MSB first function available
 - 2) Internal 8 bit baud-rate generator (maximum transmit clock period $4 / 3 T_{cyc}$)
 - 3) Continuous automatic data communication (1-256 bits)
- SIO 1: 8 bit asynchronous / synchronous serial interface
 - Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2–512 T_{cyc})
 - Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8–2048 T_{cyc})
 - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2–512 T_{cyc})
 - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(10) AD converter

- 8 bits \times 12 channels

(11) Remote control receiver circuit (connected to P73 / INT3 / T0IN terminal)

- Noise rejection function (noise rejection filter time constant can selected from 1 / 32 / 128 T_{cyc})

(12) Watchdog timer

- The watching timer period is set using an external RC.
- Watchdog timer can produce interrupt, system reset

(13) Interrupts: 15-source, 10-vector interrupts

- 1) Three priority (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is refused.
- 2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

(14) Subroutine stack levels: 1024 levels max. Stack is located in RAM.

(15) Multiplication and division

- 16 bit \times 8 bit (executed in 5 cycles)
- 24 bit \times 16 bit (12 cycles)
- 16 bit \div 8 bit (8 cycles)
- 24 bit \div 16 bit (12 cycles)

(16) Oscillation circuits

- On-chip RC oscillation circuit for system clock use.
- On-chip CF oscillation circuit for system clock use. (R_f built in)
- On-chip Crystal oscillation circuit low speed system clock use. (R_d , R_f external)

(17) Standby function

- HALT mode

HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate but VFD display and some serial transfer operations stop.

- 1) Oscillation circuits are not stopped automatically.
- 2) Release occurs on system reset or by interrupt.

- HOLD mode

HOLD mode is used to reduce power consumption. Both program execution and peripheral circuits are stopped.

- 1) CF, RC and crystal oscillation circuits stop automatically.
- 2) Release occurs on any of the following conditions.
 - (1) input to the reset pin goes low
 - (2) a specified level is input at least one of INT0, INT1, INT2
 - (3) an interrupt condition arises at port 0

-X'tal HOLD made

X'tal HOLD mode is used to reduce power consumption. Program execution is stopped.

All peripheral circuits except the base timer are stopped.

- 1) CF and RC oscillation circuits stop automatically.
- 2) Crystal oscillator is maintained in its state at HOLD mode inception.
- 3) Release occurs on any an any of the following conditions
 - (1) input to the reset pin goes low
 - (2) a specified level is input to at least one of INT0, INT1, INT2
 - (3) an interrupt condition arises at port 0
 - (4) an interrupt condition arises at the base-timer

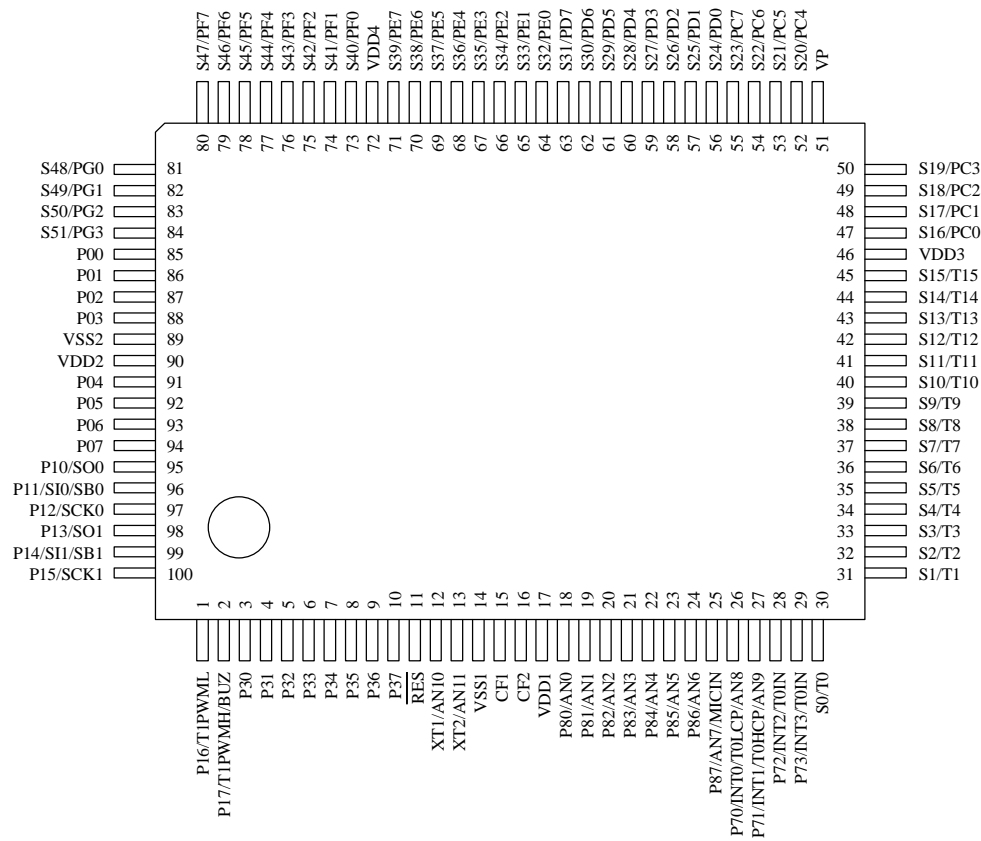
(18) Factory shipment

-delivery form QIP100E

(19) Development tools

- Evaluation chip: LC876096
- Emulator: EVA62S + ECB876500 (Evaluation chip board) + SUB876500 + POD100QFP
- Flash ROM version: LC87F65C8A

Pin Assignment

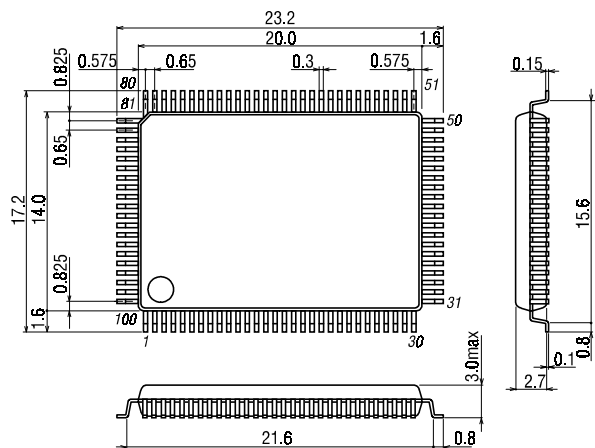


SANYO : QIP-100E Ver.1.00

Package Dimension

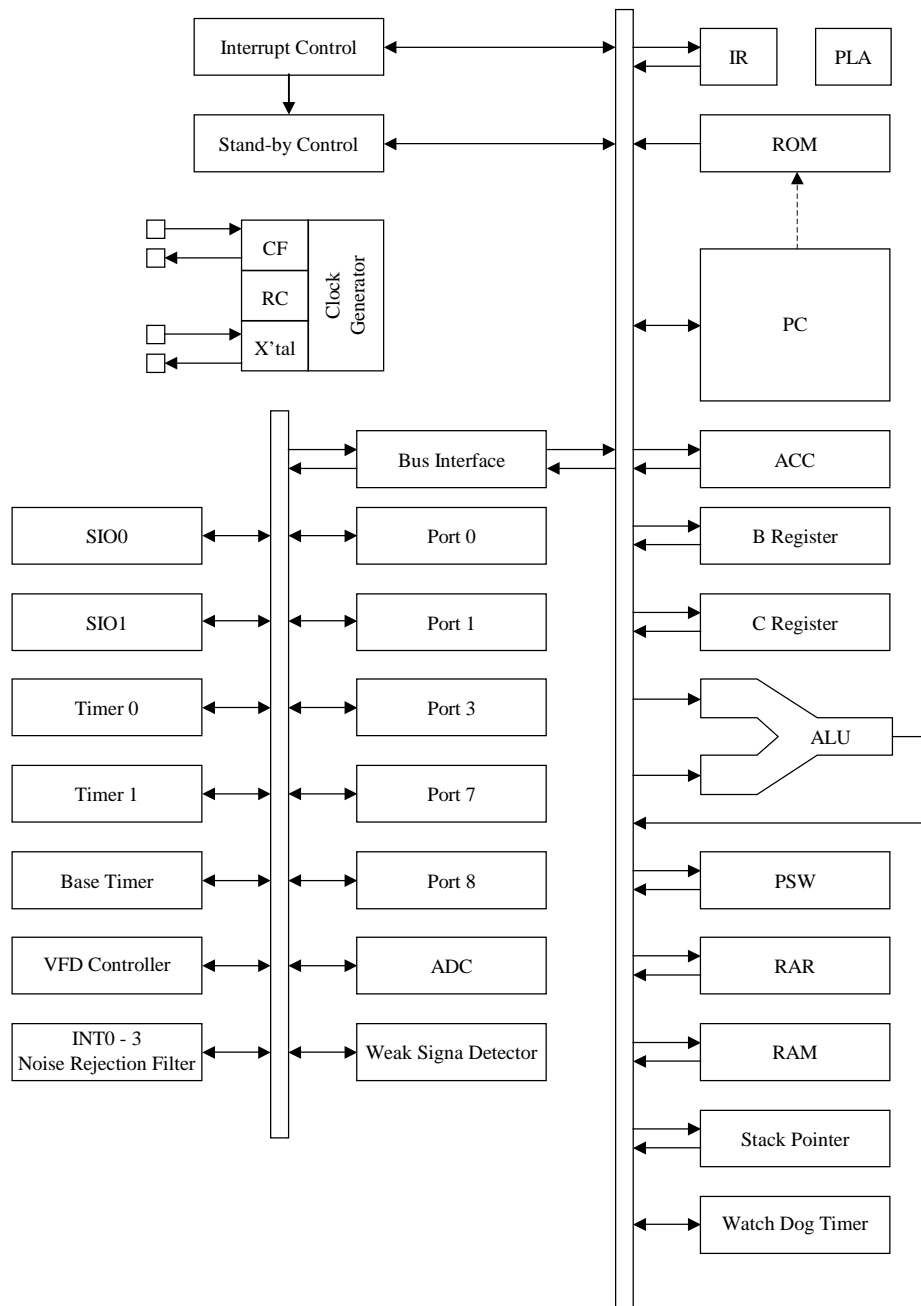
(unit : mm)

3151



SANYO : QIP-100E

System Block Diagram



Pin Assignment

| Pin name | I/O | Function | Option | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|--------|--|--------------------|---------|---------|--------------------|---------|---------|------|-----|-----|----|-----|-----|------|-----|-----|----|-----|-----|------|-----|-----|-----|----|----|------|-----|-----|-----|----|----|----|
| VSS1 VSS2 | - | • Power supply (-) | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD1 VDD2 VDD3 VDD4 | - | • Power supply (+) | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VP | - | • Power supply (-) | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT0 P00 to P07 | I/O | • 8bit input/output port • data direction programmable in nibble units • Use of pull-up resistor can be specified in nibble units • Input for HOLD release • Input for port 0 interrupt • 15V withstand at N-channel open drain output | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT1 P10 to P17 | I/O | • 8bit input/output port • data direction programmable for each bit • Use of pull-up resistor can be specified for each bit • Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16: Timer 1 PWML output P17: Timer 1 PWMH output/Buzzer output | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT3 P30 to P33 | I/O | • 8bit Input/output port • Data direction can be specified for each bit • Use of pull-up resistor can be specified for each bit • 15V withstand at N-channel open drain output | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT7 P70 to P73 | I/O | • 4bit Input/output port • Data direction can be specified for each bit • Use of pull-up resistor can be specified for each bit • Other functions P70: INT0 input/HOLD release input/Timer0L capture Input/output for watchdog timer P71: INT1 input/HOLD release input/Timer0H capture input P72: INT2 input/HOLD release input/timer 0 event input/Timer0L capture input P73: INT3 input(noise rejection filter attached input)/timer 0 event input/Timer0H capture input AD input port: AN8(P70), AN9(P71) The following types of interrupt detection are possible: <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising/ falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr><tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr><tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr><tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr></table> | | Rising | Falling | Rising/ falling | H level | L level | INT0 | Yes | Yes | No | Yes | Yes | INT1 | Yes | Yes | No | Yes | Yes | INT2 | Yes | Yes | Yes | No | No | INT3 | Yes | Yes | Yes | No | No | No |
| | Rising | Falling | Rising/ falling | H level | L level | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT0 | Yes | Yes | No | Yes | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT1 | Yes | Yes | No | Yes | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT2 | Yes | Yes | Yes | No | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT3 | Yes | Yes | Yes | No | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Pin name | I/O | Function description | Option |
|-------------------------|-----|--|--------|
| PORT8 P80 to P87 | I/O | <ul style="list-style-type: none"> • 8bit Input/output port • Input/output can be specified in a bit unit • Other functions: AD input port: AN0 to AN7 Weak signal detector input port: MICIN(P87) | No |
| S0/T0 to S6/T6 | O | • Large current output for VFD display controller digit (can be used for segment) | Yes |
| S7/T7 to S8/T8 | O | • Large current output for VFD display controller digit (can be used for segment) | No |
| S9/T9 to S15/T15 | O | • Large current output for VFD display controller segment/digit | No |
| S16 to S23 | I/O | <ul style="list-style-type: none"> • Output for VFD display controller segment/digit • Other functions: High voltage input port: PC0 to PC7 | No |
| S24 to S31 | I/O | <ul style="list-style-type: none"> • Output for VFD display controller segment • Other functions: High voltage input port: PD0 to PD7 | No |
| S32 to S39 | I/O | <ul style="list-style-type: none"> • Output for VFD display controller segment • Other functions: High voltage input port: PE0 to PE7 | Yes |
| S40 to S47 | I/O | <ul style="list-style-type: none"> • Output for VFD display controller segment • Other functions: High voltage input/output port: PF0 to PF7 | Yes |
| S48 to S51 | I/O | <ul style="list-style-type: none"> • Output for VFD display controller segment • Other functions: High voltage input/output port: PG0 to PG3 | No |
| $\overline{\text{RES}}$ | I | Reset terminal | No |
| XT1 | I | <ul style="list-style-type: none"> • Input for 32.768kHz crystal oscillation • Other functions: General purpose input port When not in use, connect to VDD1. AD input port: AN10 | No |
| XT2 | I/O | <ul style="list-style-type: none"> • Output for 32.768kHz crystal oscillation • Other functions: General purpose input port When not in use, set to oscillation mode and leave open circuit. AD input port: AN11 | No |
| CF1 | I | Input terminal for ceramic oscillator | No |
| CF2 | O | Output terminal for ceramic oscillator | No |

Port Output Configuration

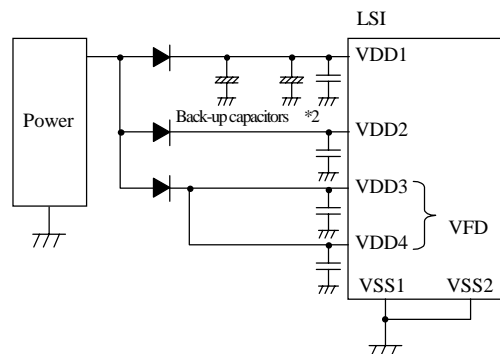
Output configuration and pull-up/pull-down resistor options are shown in the following table.
Input/output is possible even when port is set to output mode.

| Terminal | Option applies to: | Options | Output Format | Pull-up resistor | Pull-down resistor |
|--------------------------------|--------------------|---------|--|-----------------------|--------------------|
| P00 to P07 | 1 bit units | 1 | CMOS | Programmable (Note 1) | - |
| | | 2 | 15 voltage Nch-open drain | None | - |
| P10 to P17 | each bit | 1 | CMOS | Programmable | - |
| | | 2 | Nch-open drain | Programmable | - |
| P30 to P37 | each bit | 1 | CMOS | Programmable | - |
| | | 2 | 15V Nch-open drain | None | - |
| P70 | - | None | Nch-open drain | Programmable | - |
| P71 to P73 | - | None | CMOS | Programmable | - |
| P80 to P87 | - | None | Nch-open drain | None | - |
| S0/T0 to S6/T6 | each bit | 1 | High voltage Pch-open drain | - | Fixed |
| | | 2 | High voltage Pch-open drain | - | None |
| S7/T7 to S15/T15 S16 to S31 | - | None | High voltage Pch-open drain | - | fixed |
| S32 to S47 | each bit | 1 | High voltage Pch-open drain | - | Fixed |
| | | 2 | High voltage Pch-open drain | - | None |
| S48 to S51 | - | None | High voltage Pch-open drain | - | None |
| XT1 | - | None | Input only | None | - |
| XT2 | - | None | Output for 32.768kHz crystal oscillation | None | - |

Note 1 Programmable pull-up resistors of Port 0 can be attached in nibble units (P00-03, P04-07).

* Note 1: Connect as follows to reduce noise on VDD and increase the back-up time.
VSS1, and VSS2 must be connected together and grounded.

*Note 2 : The power supply for the internal memory is VDD1 but it uses the VDD2 as the power supply for ports. When the VDD2 is not backed up, the port level does not become “H” even if the port latch is in the “H” level. Therefore, when the VDD2 is not backed up and the port latch is “H” level, the port level is unstable in the HOLD mode, and the back up time becomes shorter because the through current runs from VDD to GND in the input buffer.
If VDD2 is not backed up, output “L” by the program or pull the port to “L” by the external circuit in the HOLD mode so that the port level becomes “L” level and unnecessary current consumption is prevented.



1. Absolute Maximum Ratings at Ta=25°C and VSS1=VSS2=0V

| Parameter | | Symbol | Pins | Conditions | VDD[V] | Ratings | | | unit |
|-----------------------------|----------------------|------------------|---|---|--------|---------|------|---------|------|
| | | | | | | min. | typ. | max. | |
| Supply voltage | | VDDMAX | VDD1,VDD2,VDD3, VDD4 | VDD1=VDD2= VDD3=VDD4 | | -0.3 | | +7.0 | V |
| Input voltage | | VI(1) | XT1,XT2,CF1, $\overline{\text{RES}}$ | | | -0.3 | | VDD+0.3 | |
| | | VI(2) | VP | | | VDD-45 | | VDD+0.3 | |
| Output voltage | | VO(1) | S0/T0 to S15/T15 | | | VDD-45 | | VDD+0.3 | |
| Input/Output voltage | | VIO(1) | •Port 0: CMOS output option •Port 1 •Port 3: CMOS output option •Port 7 •Port 8 | | | -0.3 | | VDD+0.3 | |
| | | VIO(2) | •Port 0 open drain •Port 3 open drain | | | -0.3 | | 15 | |
| | | VIO(3) | S16 to S51 | | | VDD-45 | | VDD+0.3 | |
| High level output current | Peak output current | IOPH(1) | Port 0, 1, 3 | •CMOS output selected •Current at each pin | | -10 | | | mA |
| | | IOPH(2) | Port71,72,73 | Current at each pin | | -3 | | | |
| | | IOPH(3) | S0/T0 to S15/T15 | Current at each pin | | -30 | | | |
| | | IOPH(4) | S16 to S51 | Current at each pin | | -15 | | | |
| | Total output current | Σ IOAH(1) | Port 0 | Total of all pins | | -30 | | | |
| | | Σ IOAH(2) | Port 1,3 | Total of all pins | | -30 | | | |
| | | Σ IOAH(3) | Port 7 | Total of all pins | | -5 | | | |
| | | Σ IOAH(4) | S0/T0 to S15/T15 | Total of all pins | | -65 | | | |
| | | Σ IOAH(5) | S16 to S27 | Total of all pins | | -60 | | | |
| | | Σ IOAH(6) | S28 to S39 | Total of all pins | | -60 | | | |
| | | Σ IOAH(7) | S40 to S51 | Total of all pins | | -60 | | | |
| Low level output current | Peak output current | IOPL(1) | Port 02, 03 | For each pin | | | | 30 | |
| | | IOPL(2) | •Port 00,01,04 to 07 •Port 1,3 | For each pin | | | | 20 | |
| | | IOPL(3) | Port 7,8 | For each pin | | | | 5 | |
| | Total output current | Σ IOAL(1) | Port 0 | For each pin | | | | 60 | |
| | | Σ IOAL(2) | Ports 1,3 | For each pin | | | | 50 | |
| | | Σ IOAL(3) | Ports 7,8 | For each pin | | | | 20 | |
| Maximum power dissipation | | Pdmax | QIP100E | Ta = -30 to+70°C | | | | 500 | mW |
| Operating temperature range | | Topr | | | | -30 | | 70 | °C |
| Storage temperature range | | Tstg | | | | -55 | | 125 | |

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings | | | unit |
|---------------------------------|----------|--|--|---------|------------|------|-------------|------|
| | | | | | min. | typ. | max. | |
| Operating supply voltage range | VDD(1) | VDD1=VDD2=VDD3=VDD4 | $0.294\mu\text{s} \leq t_{\text{CYC}} \leq 200\mu\text{s}$ | | 4.5 | | 6.0 | V |
| Hold voltage | VHD | VDD1 | RAM and the register data are kept in HOLD mode. | | 2.0 | | 6.0 | |
| Pull-down voltage | VP | VP | | 4.5–6.0 | -35 | | VDD | |
| Input high voltage | VIH(1) | •Port 0,3: CMOS output option •Port 8 | Output disable | 4.5–6.0 | 0.3VDD+0.7 | | VDD | |
| | VIH(2) | Port 0,3: N-ch open drain output | Output disable | 4.5–6.0 | 0.3VDD+0.7 | | 13.5 | |
| | VIH(3) | •Port 1 •Port71,72,73 •P70 port input/interrupt | Output disable | 4.5–6.0 | 0.3VDD+0.7 | | VDD | |
| | VIH(4) | S16 to S51 | Output P-channel Tr. OFF | 4.5–6.0 | 0.3VDD+1.0 | | VDD | |
| | VIH(5) | P70 Weak signal input | Output disable | 4.5–6.0 | 0.75VDD | | VDD | |
| | VIH(6) | Port 70 Watchdog timer | Output disable | 4.5–6.0 | 0.9VDD | | VDD | |
| | VIH(7) | XT1, XT2, CF1, $\overline{\text{RES}}$ | | 4.5–6.0 | 0.75VDD | | VDD | |
| Input low voltage | VIL(1) | •Port 0,3: CMOS output option •Port 8 | Output disable | 4.5–6.0 | VSS | | 0.15VDD+0.4 | |
| | VIL(2) | Port 0,3: N-ch open drain output | Output disable | 4.5–6.0 | VSS | | 0.15VDD+0.4 | |
| | VIL(3) | •Port 1 •Port 71,72,73 •P70 port input/interrupt | Output disable | 4.5–6.0 | VSS | | 0.1VDD+0.4 | |
| | VIL(4) | S16 to S51 | Output P-channel Tr. OFF | 4.5–6.0 | -35 | | 0.2VDD | |
| | VIL(5) | Port 87 weak signal input | Output disabled | 4.5–6.0 | VSS | | 0.25VDD | |
| | VIL(6) | Port 70 Watchdog timer | Output disabled | 4.5–6.0 | VSS | | 0.8VDD-1.0 | |
| | VIL(7) | XT1,XT2,CF1, $\overline{\text{RES}}$ | | 4.5–6.0 | VSS | | 0.25VDD | |
| Operation cycle time | tCYC | | | 4.5–6.0 | 0.294 | | 200 | μs |
| External system clock frequency | fEXCF(1) | CF1 | •CF2 open circuit •system clock divider set to 1/1 •external clock DUTY = 50±50% | 4.5–6.0 | 0.1 | | 10 | MHz |
| | | | •CF2 open circuit vsystem clock divider set to 1/2 | 4.5–6.0 | 0.2 | | 20 | |

Continued/

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|---|---------|----------|---|---------|------|--------|------|------|
| | | | | VDD[V] | min. | typ. | max. | |
| Oscillation stabilizing time period (Note 1) | FmCF(1) | CF1, CF2 | 10MHz ceramic resonator oscillation Refer to figure 1 | 4.5–6.0 | | 10 | | |
| | FmCF(2) | CF1, CF2 | 4MHz ceramic resonator oscillation Refer to figure 1 | 4.5–6.0 | | 4 | | |
| | FmRC | | RC oscillation | 4.5–6.0 | 0.3 | 1.0 | 2.0 | |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal resonator oscillation Refer to figure 2 | 4.5–6.0 | | 32.768 | | |

(Note 1) The oscillation constant is shown in table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit |
|---------------------|--------|--|--|---------|---------|------|------|
| | | | | VDD[V] | min. | typ. | max. |
| Input high current | IIH(1) | Ports 0,3: N-ch open drain output | •Output disabled •VIN=13.5V (including OFF state leak current of the output Tr.) | 4.5-6.0 | | | 5 |
| | IIH(2) | Port 0,1,3,7,8 | •Output disabled •Pull-up resistor OFF. •VIN=VDD (including OFF state leak current of the output Tr.) | 4.5-6.0 | | | 1 |
| | IIH(3) | S16 to S51 without pull-down resistor (Port C,D,E,F,G) | When configured as an input port VIN=VDD | 4.5-6.0 | | | 60 |
| | IIH(4) | $\overline{\text{RES}}$ | VIN=VDD | 4.5-6.0 | | | 1 |
| | IIH(5) | XT1,XT2 | When configured as an input port VIN=VDD | 4.5-6.0 | | | 1 |
| | IIH(6) | CF1 | VIN=VDD | 4.5-6.0 | | | 15 |
| | IIH(7) | P87/AN7/MICIN weak signal input | VIN=VBIS+0.5V (VBIS : Bias voltage) | 4.5-6.0 | 4.2 | 8.5 | 15 |
| Input low current | IIL(1) | Port 0,1,3,7,8 | •Output disabled •VIN=VSS (including OFF state leak current of the output Tr.) | 4.5-6.0 | -1 | | |
| | IIL(2) | $\overline{\text{RES}}$ | VIN=VSS | 4.5-6.0 | -1 | | |
| | IIL(3) | XT1,XT2 | When configured as an input port VIN=VSS | 4.5-6.0 | -1 | | |
| | IIL(4) | CF1 | VIN=VSS | 4.5-6.0 | -15 | | |
| | IIL(5) | P87/AN7/MICIN weak signal input | VIN=VBIS-0.5V (VBIS : Bias voltage) | 4.5-6.0 | -15 | -8.5 | -4.2 |
| Output high voltage | VOH(1) | Port 0,1,3: CMOS output option | IOH=-1.0mA | 4.5-6.0 | VDD-1 | | V |
| | VOH(2) | | IOH=-0.1mA | 4.5-6.0 | VDD-0.5 | | |
| | VOH(3) | Port 7 | IOH=-0.4mA | 4.5-6.0 | VDD-1 | | |
| | VOH(4) | S0/T0-S15/T15 | IOH=-20.0mA | 4.5-6.0 | VDD-1.8 | | |
| | VOH(5) | | IOH=-1.0mA IOH at any single pin is not over 1mA. | 4.5-6.0 | VDD-1 | | |
| | VOH(6) | S2+ to S51 | IOH=-5.0mA | 4.5-6.0 | VDD-1.8 | | |
| | VOH(7) | | IOH=-1.0mA IOH at any single pin is not over 1mA. | 4.5-6.0 | VDD-1 | | |
| Output low voltage | VOL(1) | Port 02, 03 | IOL=30mA | 4.5-6.0 | | | 1.5 |
| | VOL(2) | Port 0,1,3 | IOL=10mA | 4.5-6.0 | | | 1.5 |
| | VOL(3) | | IOL=1.6mA | 4.5-6.0 | | | 0.4 |
| Pull-up resistor | Rpu | Port 0,1,3,7 | VOH=0.9VDD | 4.5-6.0 | 15 | 40 | 0 |

Continued/

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|--------------------------------------|---------|---|--|---------|---------|--------|------|------------------|
| | | | | VDD[V] | min. | typ. | max. | |
| Output off-leak current | IOFF(1) | S0/T0 to S15/T15, S16 to S51 without pull-down resistor | •Output P-ch Tr. OFF •VOUT=VSS | 4.5–6.0 | -1 | | | μA |
| | IOFF(2) | | •Output P-ch Tr. OFF •VOUT=VDD-40V | 4.5–6.0 | -30 | | | |
| Resistance of the low level hold Tr. | Rinpd | S16 to S51 | •Output P-ch Tr. OFF | 4.5–6.0 | | 200 | | $\text{K}\Omega$ |
| High voltage pull-down resistor | Rpd | S0/T0 to S15/T15, S16 to S51 with pull-down resistor | •Output P-ch Tr. OFF •VOUT=3V •Vp=-30V | 5.0 | 60 | 100 | 200 | |
| Hysteresis voltage | VHIS(1) | •Port 1,7 •RES | | 4.5–6.0 | | 0.1VDD | | V |
| | VHIS(2) | Port 87 weak signal input | | 4.5–6.0 | | 0.1VDD | | |
| Pin capacitance | CP | All pins | •All other terminals connected to VSS. •f=1MHz •T _a =25°C | 4.5–6.0 | | 10 | | pF |
| Input sensitivity | Vsen | Port 87 weak signal input | | 4.5–6.0 | 0.12VDD | | | V _{pp} |

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | | Symbol | Pins | Conditions | VDD[V] | Ratings | | | unit |
|---------------|-------------------|------------------------|---|--|---|---------|------|----------------------|------|
| | | | | | | min. | typ. | max. | |
| Serial clock | Input clock | Cycle Time | tSCK(1) | SCK0(P12) | Refer to figure 6 | 4.5–6.0 | 4/3 | | tCYC |
| | | Low Level pulse width | tSCKL(1) | | | 2/3 | | | |
| | | | tSCKLA(1) | | | 2/3 | | | |
| | | High Level pulse width | tSCKH(1) | | | 2/3 | | | |
| | | | tSCKHA(1) | | | 3 | | | |
| | | Cycle Time | tSCK(2) | SCK1(P15) | Refer to figure 6 | 4.5–6.0 | 2 | | |
| | Output clock | Low Level pulse width | tSCKL(2) | | | 1 | | | tSCK |
| | | | tSCKLA(2) | | | 3/4 | | | |
| | | High Level pulse width | tSCKH(3) | | | 1/2 | | | |
| | | | tSCKHA(2) | | | 2 | | | |
| | | Cycle Time | tSCK(3) | SCK0(P12) | •CMOS output option •Refer to figure 6 | 4.5–6.0 | 4/3 | | |
| | | Low Level pulse width | tSCKL(3) | | | | 1/2 | | |
| | | | tSCKLA(2) | | | | 3/4 | | |
| | | High Level pulse width | tSCKH(3) | | | | 1/2 | | |
| | | | tSCKHA(2) | | | | 2 | | |
| | | Cycle Time | tSCK(4) | SCK1(P15) | •CMOS output option •Refer to figure 6 | 4.5–6.0 | 2 | | tCYC |
| | | Low Level pulse width | tSCKL(4) | | | | 1/2 | | tSCK |
| | | | tSCKH(4) | | | | 1/2 | | |
| Serial input | Data set-up time | tsDI | SI0(P10), SI1(P13), SB0(P11), SB1(P14) | •Measured with respect to SI0CLK leading edge. •Refer to figure 6 | 4.5–6.0 | 0.03 | | | μs |
| | Data hold time | thDI | | | | 0.03 | | | |
| Serial output | Output delay time | tdDO | SO0(P12), SO1(P15), SB0(011), SB1(P14) | •Measured with respect to SI0CLK trailing edge. •When port is open drain: Time delay from SI0CLK trailing edge to the SO data change. •Refer to figure 6 | 4.5–6.0 | | | 1/3 tCYC +0.05 | |

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings | | | unit |
|----------------------------|--------------------|--|---|---------|---------|------|------|------|
| | | | | | min. | typ. | max. | |
| High/low level pulse width | tPIH(1) tPIL(1) | INT0(P70), INT1(P71), INT2(P72) | •Interrupt acceptable •Events to timer 0 can be input. | 4.5–6.0 | 1 | | | tCYC |
| | tPIH(2) tPIL(2) | INT3(P73) (Noise rejection ratio set to 1/1.) | •Interrupt acceptable •Events to timer 0 can be input. | 4.5–6.0 | 2 | | | |
| | tPIH(3) tPIL(3) | INT3(P73) (Noise rejection ratio set to 1/32.) | •Interrupt acceptable •Events to timer 0 can be input. | 4.5–6.0 | 64 | | | |
| | tPIH(4) tPIL(4) | INT3(P73) (Noise rejection ratio set to 1/128.) | •Interrupt acceptable •Events to timer 0 can be input. | 4.5–6.0 | 256 | | | |
| | tPIL(5) | MICIN(P87) | •Weak signal detection counter enabled | 4.5–6.0 | 1 | | | |
| | tPIL(6) | RES# | Reset possible | 4.5–6.0 | 200 | | | μs |

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings | | | unit |
|----------------------------|--------|--|--|---------|-----------------------------|------|----------------------------|------|
| | | | | | min. | typ. | max. | |
| Resolution | N | AN0(P80) to | | 4.5–6.0 | | 8 | | bit |
| Absolute precision | ET | AN7(P87) | (Note2) | 4.5–6.0 | | | ±1.5 | LSB |
| Conversion time | TCAD | AN8(P70), AN9(P71) AN10(XT1), AN11(XT2) | AD conversion time = 32 × tCYC (ADCR2=0) (Note 3) | 4.5–6.0 | 15.62 (tCYC= 0.488μs) | | 97.92 (tCYC= 3.06μs) | μs |
| | | | AD conversion time = 64 × tCYC (ADCR2=1) (Note 3) | | 18.82 (tCYC= 0.294μs) | | 97.92 (tCYC= 1.53μs) | |
| Analog input voltage range | VAIN | | | 4.5–6.0 | VSS | | VDD | V |
| Analog port input current | IAINH | | VAIN=VDD | 4.5–6.0 | | | 1 | μA |
| | IAINL | | VAIN=VSS | 4.5–6.0 | -1 | | | |

(Note 2) Absolute precision not including quantizing error (±1/2 LSB).

(Note 3) Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings | | | unit |
|---|----------|---------------------------------|--|---------|---------|------|------|------|
| | | | | | min. | typ. | max | |
| Current dissipation during basic operation (Note 4) | IDDOP(1) | VDD1= VDD2= VDD3= VDD4 | •FmCF=10MHz for Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Divider set to 1/1 | 4.5–6.0 | | 12.5 | 30.0 | mA |
| | IDDOP(2) | | •CF1=20MHz for external clock •FsX'tal=32.768kHz for crystal oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Divider set to 1/2 | 4.5–6.0 | | 14.0 | 31.0 | |
| | IDDOP(3) | | •FmCF=4MHz Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Divider set to 1/1 | 4.5–6.0 | | 5.8 | 17.0 | |
| | IDDOP(4) | | •FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz for crystal oscillation •System clock: RC oscillation •Divider set to 1/2 | 4.5–6.0 | | 1.0 | 10.0 | |
| | IDDOP(5) | | •FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz for crystal oscillation •System clock: 32.768kHz •Internal RC oscillation stopped. •Divider set to 1/2 | 4.5–6.0 | | 70 | 160 | μA |

Continued/

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|--|------------|---------------------------------|---|------------|------|------|------|------|
| | | | | VDD[V] | min. | typ. | max. | |
| Current dissipation HALT mode (Note 4) | IDDHALT(1) | VDD1= VDD2= VDD3= VDD4 | HALT mode •FmCF=10MHz for Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Divider: 1/1 | 4.5 to 6.0 | | 5.0 | 12.0 | mA |
| | IDDHALT(2) | | HALT mode •CF1=20MHz for external clock •FsX'tal=32.768kHz for crystal oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Divider 1/2 | 4.5 to 6.0 | | 6.0 | 13.0 | |
| | IDDHALT(3) | | HALT mode •FmCF=4MHz for Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Divider: 1/2 | 4.5 to 6.0 | | 2.2 | 6.0 | |
| | IDDHALT(4) | | HALT mode •FmCF=0Hz (When oscillation stops.) •FsX'tal=32.768kHz for crystal oscillation •System clock : RC oscillation •Divider: 1/2 | 4.5 to 6.0 | | 500 | 1600 | μA |
| | IDDHALT(5) | | HALT mode •FmCF=0Hz (When oscillation stops.) •FsX'tal=32.768kHz for crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stopped. •Divider: 1/2 | 4.5 to 6.0 | | 60 | 150 | |

Continued/

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|---|------------|------|---|------------|------|--------|------|------|
| | | | | VDD[V] | min. | typ. | max. | |
| Current dissipation HOLD mode | IDDHOLD(1) | VDD1 | HOLD mode •CF1=VDD or open circuit (when using external clock) | 4.5 to 6.0 | | 0.0015 | 25 | μA |
| Current dissipation Date/time clock HOLD mode | IDDHOLD(2) | VDD1 | Date/time clock HOLD mode •CF1=VDD or open circuit (when using external clock) •FmX'tal=32.768kHz for crystal oscillation | 4.5 to 6.0 | | 50 | 140 | |

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Main system clock oscillation circuit characteristics

The characteristics in the table below is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer

Table 1. Main system clock oscillation circuit characteristics using ceramic resonator

| Frequency | Manufacturer | Oscillator | Circuit parameters | | | Operating supply voltage range | Oscillation stabilizing time | | Notes |
|-----------|--------------|---------------|--------------------|--------|-------|--------------------------------|------------------------------|-------|----------------|
| | | | C1 | C2 | Rd1 | | typ | max | |
| 10MHz | Murata | CSA10.0MTZ | 33pF | 33pF | 470Ω | 4.5-6.0V | 0.05ms | 0.2ms | |
| | | CST10.0MTW | (30pF) | (30pF) | 470Ω | 4.5-6.0V | 0.05ms | 0.2ms | Built in C1,C2 |
| | Kyocera | PBRC10.00BR-A | (10pF) | (10pF) | 1.0kΩ | 4.5-6.0V | 0.10ms | 0.2ms | Built in C1,C2 |
| 4MHz | Murata | CSA4.00MG | 33pF | 33pF | 1.5kΩ | 4.5-6.0V | 0.05ms | 0.2ms | |
| | | CST4.00MGW | (30pF) | (30pF) | 1.5kΩ | 4.5-6.0V | 0.05ms | 0.2ms | Built in C1,C2 |

The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure4)

Subsystem clock oscillation circuit characteristics

The characteristics in the table below is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer

Table 2. Subsystem clock oscillation circuit characteristics using crystal oscillator

| Frequency | Manufacturer | Oscillator | Circuit parameters | | | | Operating supply voltage range | Oscillation stabilizing time | | Notes |
|-----------|--------------|------------|--------------------|------|------|-------|--------------------------------|------------------------------|------|-------|
| | | | C3 | C4 | Rf | Rd2 | | typ | max | |
| 32.768MHz | Seiko EPSON | C-002Rx | 12pF | 15pF | 10MΩ | 680kΩ | 4.5-6.0V | 0.8s | 2.0s | |

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (Refer to Figure4)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

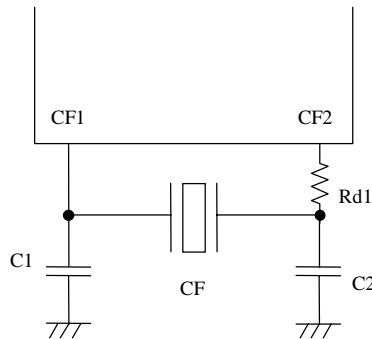


Figure 1 Ceramic oscillation circuit

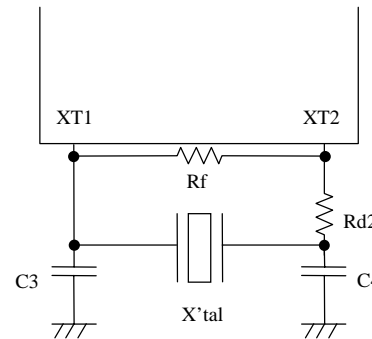


Figure 2 Crystal oscillation circuit

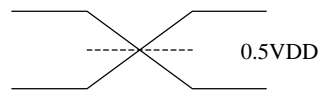


Figure 3 AC timing measurement point

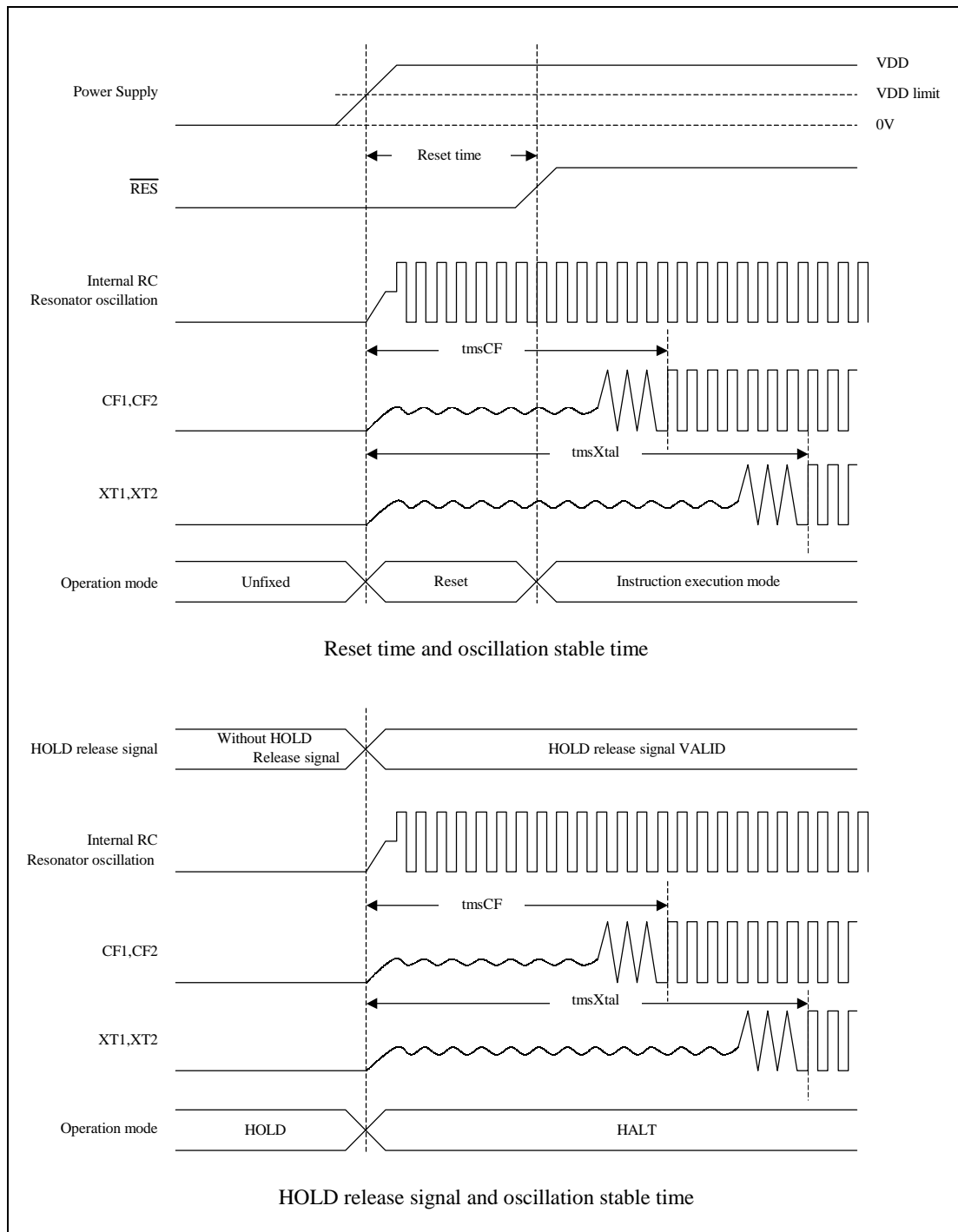
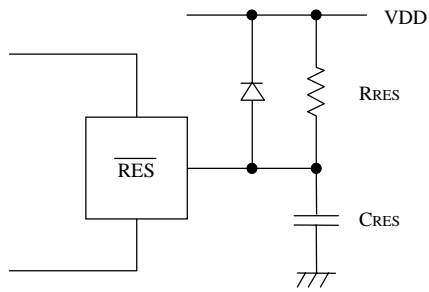


Figure 4 Oscillation stablization time



(Note) Set C_{RES} , R_{RES} values such that reset time exceeds $200\mu\text{s}$.

Figure 5 Reset circuit

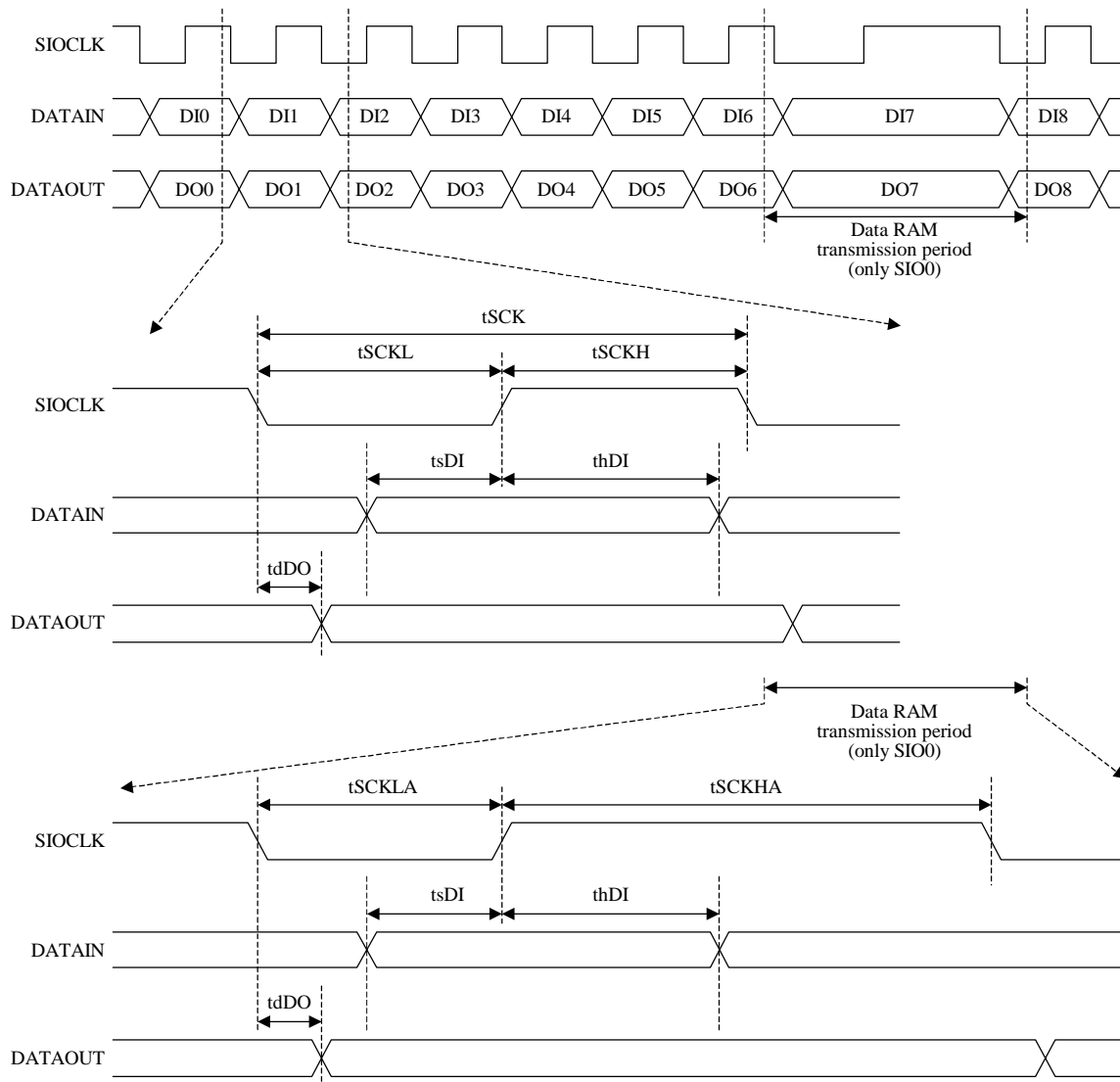


Figure 6 Serial input / output test condition

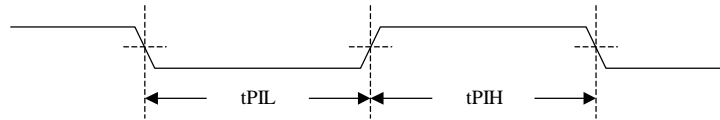


Figure 7 Pulse input timing condition

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