

**LC895196K****ATA-PI Compatible CD-ROM Decoder IC****Preliminary****Overview**

The LC895196K is a large scale integrated circuit equipped with CD-ROM functions and an internal ATA-PI (IDE) interface.

**Functions**

- CD-ROM ECC functions, SUB-CODE read function, ATA-PI (IDE) interface (Registers, etc.).

**Features**

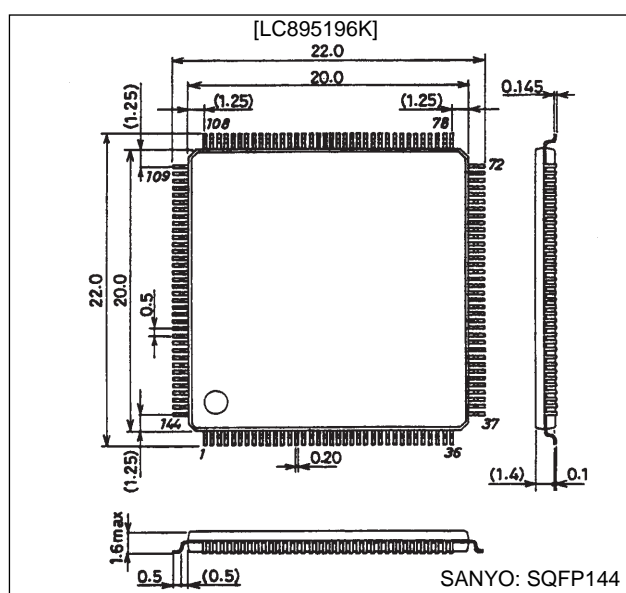
- Built-in ATA-PI (IDE) interface.
- 32× speed supported  
Uses the EDO-DRAM (× 16, 50 ns)  
16.6 Mbyte/s (with IORDY)  
Operating frequency: 33.8688 MHz
- 24× speed supported  
Uses the EDO-DRAM (× 16, 60 ns)  
16.6 Mbyte/s (without IORDY)  
Operating frequency: 33.8688 MHz
- Supports between 1 Mbit and 4 Mbit of buffer RAM when DRAM is used
- The user can flexibly set the CD main channel, the C2 flags, and the subcode regions in the buffer RAM
- Built-in batch transfer function. (Where the batch transfer function is a function that transmit the CD main channel, C2 flags, subcodes, etc. all at once.)
- Built-in multitransmit function. (Where the multitransmit function is a function that automatically transmits multiple blocks at once.)
- Built-in intelligent functions (auto buffering, auto

decoding, CD-R compatibility)

- Built in subcode P-W buffering function (NO-ECC) and CD-TEXT compatibility

**Package Dimensions**

unit: mm

**3214-SQFP144****Specifications****Absolute Maximum Ratings at  $V_{SS} = 0$  V**

Parameter	Symbol	Condition	Ratings	Unit
Maximum power supply voltage	$V_{DD}$ max	$T_a = 25^\circ\text{C}$	-0.3 to +7.0	V
I/O voltage	$V_I, V_O$	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d$ max	$T_a \leq 70^\circ\text{C}$	550	mW
Operating temperatures	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage temperatures	$T_{stg}$		-55 to +125	$^\circ\text{C}$
Soldering temperature (terminals only)		For 10 seconds	235	$^\circ\text{C}$
I/O current	$I_I, I_O$ max		$\pm 20^*$	mA

Note: \* Per basic I/O cell

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## LC895196K

### Allowable Operating Ranges at $T_a = -30$ to $+70^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		4.5	5.0	5.5	V
Input voltage range	$V_{IN}$		0		$V_{DD}$	V

### DC Characteristics at $V_{SS} = 0\text{ V}$ , $V_{DD} = 4.5$ to $5.5\text{ V}$ , $T_a = -30$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions Applicable pins (see below)	Ratings			Unit
			min	typ	max	
Input high level voltage	$V_{IH1}$	TTL compatible (1)	2.2			V
Input low level input	$V_{IL1}$	TTL compatible (1)			0.8	V
Input high level voltage	$V_{IH2}$	TTL compatible with pull-up resistor: (10)	2.2			V
Input low level input	$V_{IL2}$	TTL compatible with pull-up resistor: (10)			0.8	V
Input high level voltage	$V_{IH3}$	TTL compatible Schmitt: (2), (3), (11)	2.2			V
Input low level input	$V_{IL3}$	TTL compatible Schmitt: (2), (3), (11)			0.8	V
Output high level voltage	$V_{OH1}$	$I_{OH} = -2\text{ mA}$ : (4), (10)	$V_{DD} - 2.1$			V
Output low level voltage	$V_{OL1}$	$I_{OL} = 2\text{ mA}$ : (4), (10)			0.4	V
Output high level voltage	$V_{OH2}$	$I_{OH} = -8\text{ mA}$ : (5)	$V_{DD} - 2.1$			V
Output low level voltage	$V_{OL2}$	$I_{OL} = 8\text{ mA}$ : (5)			0.4	V
Output high level voltage	$V_{OH3}$	$I_{OH} = -4\text{ mA}$ : (8), (11)	$V_{DD} - 2.1$			V
Output low level voltage	$V_{OL3}$	$I_{OL} = 24\text{ mA}$ : (8), (11)			0.4	V
Output low level voltage	$V_{OL4}$	$I_{OL} = 24\text{ mA}$ : (9)			0.4	V
Output low level voltage	$V_{OL5}$	$I_{OL} = 8\text{ mA}$ : (6), (7)			0.4	V
Input leakage current	$I_{IL}$	$V_I = V_{SS}$ , $V_{DD}$ : (1), (2), (3), (11)	-10		+10	$\mu\text{A}$
Output leakage current	$I_{OZ}$	When high impedance output: (6), (8), (9), (11)	-10		+10	$\mu\text{A}$
Pull-up resistor	$R_{UP}$	(7), (10)	40	80	160	$\text{k}\Omega$

Note: The applicable pins correspond to the following names.

[INPUT]

(1) .....ATPINSEL, CSCCTRL, SUA0 to SUA6, BCK, C2PO, LRCK, SDATA, SBSO, SCOR, WFCK, TEST0 to TEST1

(2) .....ZRESET, ZCS, ZRD, ZWR, CSEL

(3) .....DA0 to DA2, ZCS1FX, ZCS3FX, ZDIOR, ZDIOW, ZDMACK, ZHRST

[OUTPUT]

(4) .....RA0 to RA8, ZCAS0, ZCAS1, ZUWE, ZLWE, ZOE, ZRAS0, EXCK

(5) .....MCK, MCK2, MCK3

(6) .....ZRSTCPU, ZRSTIC

(7) .....ZINT, ZINT1, ZSWAIT

(8) .....DMARQ, HINTRQ

(9) .....IORDY, ZIOCS16

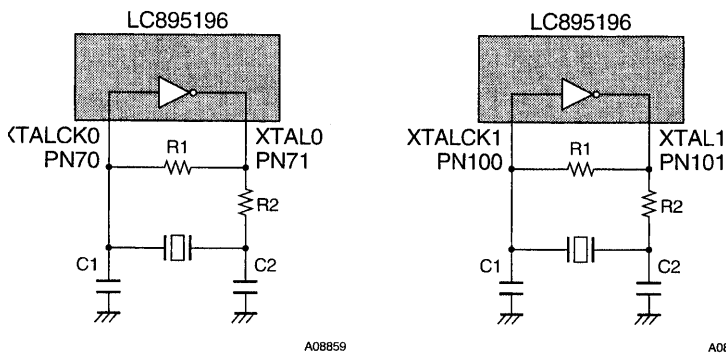
[INPUT]

(10) .....D0 to D7, IO0 to IO15

(11) .....DD0 to DD15, ZDASP, ZPDIAG

\* The XTAL0, XTALCK0, XTAL1, XTALCK1 pins are not included in the CD characteristics.

### Recommended Example of Oscillator Circuit



$R1 = 1\text{ M}\Omega$

$R2 = 47\text{ }\Omega$

$C1 = 0$

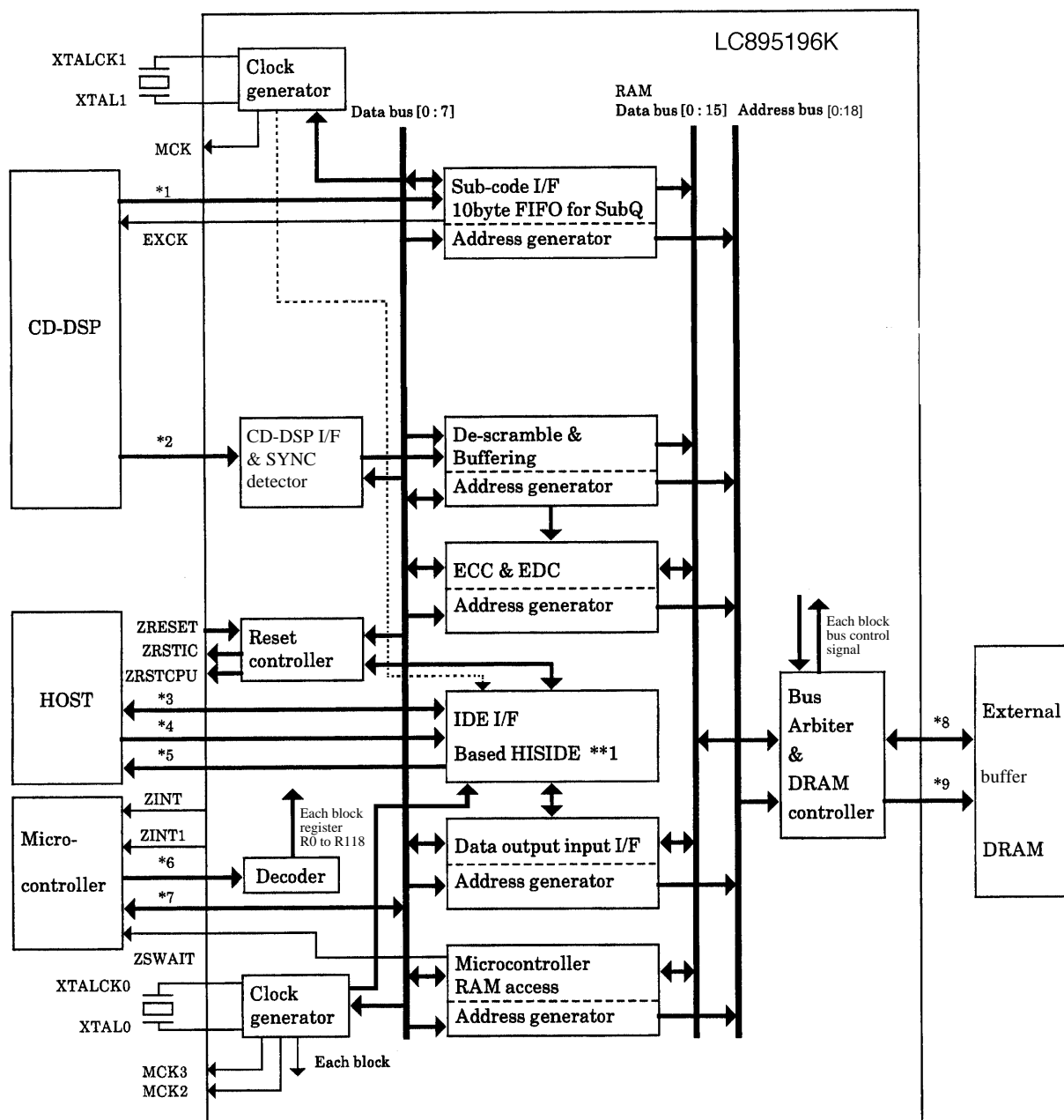
$C2 = 47\text{ pF}$

Ceramic oscillator frequency = 33.8688 MHz.

The 33.8688 MHz recommended example is for a 3× overtone.

Because the specific values are influenced by the circuit board, confer with the oscillator manufacturer.

## Block Diagram



- \*1 WFCK, SBSO, SCOR
- \*2 BCK, SDATA, LRCK, C2PO
- \*3 DD0 to DD15, ZDASP, ZPDIAG
- \*4 ZCS1FX, ZCS3FX, DA0 to DA2, ZDIOR, ZDIOW, ZDMACK, CSEL
- \*5 DMARQ, HINTRQ, ZIOCS16, IORDY, ZHRST
- \*6 ZRD, ZWR, SUA0 to SUA6, ZCS, CSCTRL
- \*7 D0 to D7
- \*8 IO0 to IO15
- \*9 RA0 to RA8, ZRAS0, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE
- \*\*1 HISIDE (WD25C32) is made by WESTERN DIGITAL

## Pin Functions

The LC895196K can be set to the opposite of the ATAPI pin layout using the setting of pin 19.

### Pin 29 ATPINSEL = 0

I: Input pin B: Bi-directional pin NC: Not connected O: Output pin P: Power supply pin

Pin No.	Symbol	Type	Function
1	V <sub>SS0</sub>	P	
2	ZRAS0	O	RAS signal output pin 0 to the buffer DRAM (Normally uses 0).
3		NC	
4	ZCAS0	O	CAS signal output pin 0 to the buffer DRAM (Normally uses 0).
5	ZCAS1	O	CAS signal output pin 1 to the buffer DRAM
6	ZOE	O	Buffer DRAM output enable
7	ZUWE	O	Buffer DRAM upper write enable
8	ZLWE	O	Buffer DRAM lower write enable
9	V <sub>SS0</sub>	P	
10	RA0	O	Address signal output pins to the data buffer DRAM
11	RA1	O	
12	RA2	O	
13	RA3	O	
14	RA4	O	
15	RA5	O	
16	RA6	O	
17	RA7	O	
18	V <sub>DD</sub>	P	
19	V <sub>SS0</sub>	P	
20	RA8	O	Address signal output pins to the data buffer DRAM
21		NC	
22	IO0	B	Data I/O pin to the data buffer DRAM. Built-in pull-up resistor.
23	IO1	B	
24	IO2	B	
25	IO3	B	
26	IO4	B	
27	IO5	B	
28	IO6	B	
29	ATPINSEL	I	ATAPI pin assignment select pin. Connect to V <sub>SS0</sub> .
30	IO7	B	Data I/O pin to the data buffer DRAM. Built-in pull-up resistor.
31	IO8	B	
32	IO9	B	
33	IO10	B	
34	IO11	B	
35	IO12	B	
36	V <sub>SS0</sub>	P	
37	V <sub>DD</sub>	P	
38	IO13	B	Data I/O pin to the data buffer DRAM. Built-in pull-up resistor.
39	IO14	B	
40	IO15	B	
41		NC	
42	V <sub>SS0</sub>	P	
43	V <sub>SS0</sub>	P	
44	V <sub>SS0</sub>	P	
45		NC	
46		NC	

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Pin No.	Symbol	Type	Function
47	C2PO	I	CD-DSP interface
48	SDATA	I	
49	BCK	I	
50	LRCK	I	
51	EXCK	O	Subcode I/O
52	WFCK	I	
53	SBSO	I	
54	V <sub>DD</sub>	P	
55	V <sub>SS0</sub>	P	
56	SCOR	I	Subcode I/O
57		NC	
58		NC	
59		NC	
60	MCK	O	XTALCK1 1/1, 1/2 and STOP output
61	TEST0	I	Test input pin. Connect to V <sub>SS</sub> .
62	TEST1	I	
63	CSEL	I	ATAPI control signal
64	ZRSTIC	O	Reset signal to the drive reset IC
65	CSCTRL	I	Microcontroller-side CS active low/high select pin
66	MCK2	O	XTALCK0 1/1, 1/2, 1/5, 1/512 and STOP output
67	MCK3	O	XTALCK0 1/1, 1/5, 2/5, 1/512 and STOP output
68	V <sub>SS0</sub>	P	
69		NC	
70	XTALCK0	I	X'tal oscillator circuit input
71	XTAL0	O	X'tal oscillator circuit input
72	V <sub>SS0</sub>	P	
73	V <sub>DD</sub>	P	
74	ZRESET	I	LSI reset
75	ZRD	I	Microcontroller data read signal input
76	ZWR	I	Microcontroller data write signal input
77	ZCS	I	Input pin for the register chip select signal from the microcontroller
78	V <sub>SS0</sub>	P	
79	SUA0	I	Microcontroller register select signals
80	SUA1	I	
81	SUA2	I	
82	SUA3	I	
83	SUA4	I	
84	SUA5	I	
85	SUA6	I	
86	D0	B	Microcontroller data signals. Built-in pull-up resistors.
87	D1	B	
88	D2	B	
89	D3	B	
90	V <sub>DD</sub>	P	
91	V <sub>SS0</sub>	P	
92	D4	B	Microcontroller data signals. Built-in pull-up resistors.
93	D5	B	
94	D6	B	
95	D7	B	
96	ZINT0	O	Output pin for interrupt request signal to the microcontroller (set by the ECC-side registers)
97	ZINT1	O	Output pin for interrupt request signal to the microcontroller (set by the ATAPI-side registers)
98	ZSWAIT	O	Wait signal to the microcontroller
99	ZRSTCPU	O	Reset signal to the CPU
100	XTAL1	I	X'tal oscillator circuit input

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Pin No.	Symbol	Type	Function
101	XTAL1	O	X'tal oscillator circuit output
102	V <sub>SS0</sub>	P	
103	ZHRST	I	ATAPI control signals
104	ZDASP	B	
105	ZCS3FX	I	
106	ZCS1FX	I	
107	DA2	I	
108	V <sub>SS0</sub>	P	
109	V <sub>DD</sub>	P	
110	DA0	I	
111	ZPDIAG	B	ATAPI control signals
112	DA1	I	
113	ZIOCS16	O	
114	INTRQ	O	
115	ZDMACK	I	
116	V <sub>SS1</sub>	P	
117	IORDY	O	ATAPI control signals
118	ZDIOR	I	
119	ZDIOW	I	
120	DMARQ	O	
121	DD15	B	ATAPI data bus
122	V <sub>SS1</sub>	P	
123	DD0	B	ATAPI data bus
124	DD14	B	
125	DD1	B	
126	V <sub>DD</sub>	P	
127	V <sub>SS1</sub>	P	
128	DD13	B	ATAPI data bus
129	DD2	B	
130	DD12	B	
131	DD3	B	
132	V <sub>SS1</sub>	P	
133	DD11	B	ATAPI data bus
134	DD4	B	
135	DD10	B	
136	V <sub>SS1</sub>	P	
137	V <sub>DD</sub>	P	
138	DD5	B	ATAPI data bus
139	DD9	B	
140	DD6	B	
141	V <sub>SS1</sub>	P	
142	DD8	B	ATAPI data bus
143	DD7	B	
144	V <sub>DD</sub>	P	

Leave the NC pins OPEN.

Those pin names starting with the letter "Z" indicate negative logic.

V<sub>SS0</sub> is the logic system ground, and V<sub>SS1</sub> is the ID interface driver ground.

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## Pin 29 ATPINSEL = 1

I: Input pin B: Bi-directional pin NC: Not connected O: Output pin P: Power supply pin

Pin No.	Symbol	Type	Function
1	V <sub>SS0</sub>	P	
2	ZRAS0	O	RAS signal output pin 0 to the buffer DRAM (Normally uses 0).
3		NC	
4	ZCAS0	O	CAS signal output pin 0 to the buffer DRAM (Normally uses 0).
5	ZCAS1	O	CAS signal output pin 1 to the buffer DRAM
6	ZOE	O	Buffer DRAM output enable
7	ZUWE	O	Buffer DRAM upper write enable
8	ZLWE	O	Buffer DRAM lower write enable
9	V <sub>SS0</sub>	P	
10	RA0	O	Address signal output pin to the data buffer DRAM
11	RA1	O	
12	RA2	O	
13	RA3	O	
14	RA4	O	
15	RA5	O	
16	RA6	O	
17	RA7	O	
18	V <sub>DD</sub>	P	
19	V <sub>SS0</sub>	P	
20	RA8	O	Address signal output pin to the data buffer DRAM
21		NC	
22	IO0	B	Data I/O pin to the data buffer DRAM. Built-in pull-up resistor.
23	IO1	B	
24	IO2	B	
25	IO3	B	
26	IO4	B	
27	IO5	B	
28	IO6	B	
29	ATPINSEL	I	ATAPI pin assignment select pin. Connect to V <sub>SS0</sub> .
30	IO7	B	Data I/O pin to the data buffer DRAM. Built-in pull-up resistor
31	IO8	B	
32	IO9	B	
33	IO10	B	
34	IO11	B	
35	IO12	B	
36	V <sub>SS0</sub>	P	
37	V <sub>DD</sub>	P	
38	IO13	B	Data I/O pin to the data buffer DRAM. Built-in pull-up resistor.
39	IO14	B	
40	IO15	B	
41		NC	
42	V <sub>SS0</sub>	P	
43	V <sub>SS0</sub>	P	
44	V <sub>SS0</sub>	P	
45		NC	
46		NC	

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Pin No.	Symbol	Type	Function
47	C2PO	I	CD-DSP interface
48	SDATA	I	
49	BCK	I	
50	LRCK	I	
51	EXCK	O	Subcode I/O
52	WFCK	I	
53	SBSO	I	
54	V <sub>DD</sub>	P	
55	V <sub>SS0</sub>	P	
56	SCOR	I	Subcode I/O
57		NC	
58		NC	
59		NC	
60	MCK	O	XTALCK1 1/1, 1/2 and STOP output
61	TEST0	I	Test input pin. Connect to V <sub>SS</sub> .
62	TEST1	I	
63	CSEL	I	ATAPI control signal
64	ZRSTIC	O	Reset signal to the drive reset IC
65	CSCTRL	I	Microcontroller-side CS active low/high select pin
66	MCK2	O	XTAKCK0 1/1, 1/2, 1/5, 1/512 and STOP output
67	MCK3	O	XTAKCK0 1/1, 1/5, 2/5, 1/512 and STOP output
68	V <sub>SS0</sub>	P	
69		NC	
70	XTALCK0	I	X'tal oscillator circuit input
71	XTAL0	O	X'tal oscillator circuit input
72	V <sub>SS0</sub>	P	
73	V <sub>DD</sub>	P	
74	ZRESET	I	LSI reset
75	ZRD	I	Microcontroller data read signal input
76	ZWR	I	Microcontroller data write signal input
77	ZCS	I	Input pin for the register chip select signal from the microcontroller
78	V <sub>SS0</sub>	P	
79	SUA0	I	Microcontroller register select signals
80	SUA1	I	
81	SUA2	I	
82	SUA3	I	
83	SUA4	I	
84	SUA5	I	
85	SUA6	I	
86	D0	B	Microcontroller data signals. Built-in pull-up resistors.
87	D1	B	
88	D2	B	
89	D3	B	
90	V <sub>DD</sub>	P	
91	V <sub>SS0</sub>	P	
92	D4	B	Microcontroller data signals Built-in pull-up resistors.
93	D5	B	
94	D6	B	
95	D7	B	
96	ZINT0	O	Output pin for interrupt request signal to the microcontroller (set by the ECC-side registers)
97	ZINT1	O	Output pin for interrupt request signal to the microcontroller (set by the ATAPI-side registers)
98	ZSWAIT	O	Wait signal to the microcontroller
99	ZRSTCPU	O	Reset signal to the CPU
100	XTAL1	I	X'tal oscillator circuit input

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Pin No.	Symbol	Type	Function
101	XTAL1	O	X'tal oscillator circuit output
102	V <sub>SS0</sub>	P	
103	DD7	B	ATAPI data bus
104	DD8	B	
105	DD6	B	
106	DD9	B	
107	DD5	B	
108	V <sub>SS1</sub>	P	
109	V <sub>DD</sub>	P	
110	DD10	B	ATAPI data bus
111	DD4	B	
112	DD11	B	
113	DD3	B	
114	DD12	B	
115	DD2	B	
116	V <sub>SS1</sub>	P	
117	DD13	B	ATAPI data bus
118	DD1	B	
119	DD14	B	
120	DD0	B	
121	DD15	B	
122	V <sub>SS1</sub>	P	
123	DMARQ	O	ATAPI control signals
124	ZDIOW	I	
125	ZDIOR	I	
126	V <sub>DD</sub>	P	
127	V <sub>SS1</sub>	P	
128	IORDY	O	ATAPI control signals
129	ZDMACK	I	
130	INTRQ	O	
131	ZIOCS16	O	
132	V <sub>SS1</sub>	P	
133	DA1	I	ATAPI control signals
134	ZPDIAG	B	
135	DA0	I	
136	V <sub>SS1</sub>	P	
137	V <sub>DD</sub>	P	
138	DA2	I	ATAPI control signals
139	ZCS1FX	I	
140	ZCS3FX	I	
141	V <sub>SS1</sub>	P	
142	ZDASP	B	ATAPI control signals
143	ZHRST	I	
144	V <sub>DD</sub>	P	

Leave the NC pins OPEN.

Those pin names starting with the letter "Z" indicate negative logic.

V<sub>SS0</sub> is the logic system ground, and V<sub>SS1</sub> is the ID interface driver ground.

## Pin Descriptions

### 1. ATAPI

#### ZCS1FX (input)

Chip select signal for selecting the command block register.

#### ZCS3FX (input)

Chip select signal for selecting the control block register.

#### DA0 to 2 (input)

Addresses for accessing the various ATAPI addresses.

#### ZDASP (input/output)

Drive 1 is output and drive 0 is input.

Signal for indicating the existence of drive 1 to drive 0. Attach external pull-up resistors.

#### DD0 to DD15 (input/output)

16-bit data bus. Can be used for transferring 8 bit and 16 bit data.

#### ZDIOR (input)

Read strobe signal from the host.

#### ZDIOW (input)

Write strobe signal from the host.

#### ZDMACK (input)

During DMA transmission, this is the acknowledged signal from the host responding to the DMARQ drive request signal. There is no built-in pull-up resistor.

#### DMARQ (output)

This is the drive request signal during DMA transmission.

#### HINTRQ (output)

Drive interrupt signal to the host.

#### ZIOCS16 (output)

This signal is asserted depending on the drive when the drive can support 16-bit transfers. This signal is not asserted during DMA transfers.

#### IORDY (output)

This signal indicates that the drive is ready to respond during data transfer. This signal is low if the drive is not ready. Attach an external pull-up resistor.

#### ZPDIAG (input/output)

This signal is asserted by drive 1 to inform drive 0 that the diagnostics are complete. Attach an external pull-up resistor.

#### ZHRST (input)

This is the reset signal from the host. Applying a low signal to this pin causes ZRSTIC to go low and resets the drive. There is no built-in pull-up resistor.

#### ZINT1 (output)

This is the interrupt request signal from the IDE block to the MC.

#### CSEL (input)

This is the cable select signal that determines master/slave. Attach an external pull-up resistor.

### 2. Microcontroller Interface

#### ZCS (input)

This is the MC-side chip select.

#### CSCTRL (input)

This signal selects the MC-side chip select logic.

High: ZCS is active low

Low: ZCS is active high

#### ZRD, ZWR, SUA0 to SUA6 (inputs)

These are the MC interface control signals. Addressing uses SUA0 to SUA6.

#### ZSWAIT (output)

When the microcontroller accesses the RAM, the SUB-CPU must wait while this pin is low.

D7 to D0 (input/output)

This is the MC-side data bus. Built-in pull-up resistor.

ZINT (output)

This is the interrupt signal to the microcontroller.

### 3. The Buffer RAM

IO0 to IO15 (input/output)

This is the buffer DRAM data bus. Built-in pull-up resistors.

RA0 to RA8 (output)

These are the address pins for the buffer RAM.

ZRAS0 (output)

These are the RAS output pins for the buffer DRAM.

ZCAS0 and ZCAS1 (output)

This is the CAS output pin for the buffer DRAM. Normally ZCAS0 is used. When two 1M (64K × 16 bit) DRAMS are used, connect the ZCAS0 output to the CAS pin of each DRAM. When the 2CAS type is used, connect ZCAS0 to UCAS and connect ZCAS1 to LCAS.

ZOE (output)

The read output signal for the buffer DRAM.

ZUWE, ZLWE (output)

This is the write output signal for the buffer DRAM. This connects to various DRAM pins. When the 2CAS type is used, connect ZLWE to the write enable signal.

### 4. Subcode Interface

EXCK, WFCK, SBSO, SCOR (input or output)

These are the subcode interface pins. By connecting these to the CD-DSP the subcode data is accepted by the LC895196K and transferred to the host.

### 5. The CD-DSP Data

BCK, SDATA, LRCK, C2PO (input)

When connected to CD-DSP, CD-ROM data is acquired. C2PO is a pin for use by the C2 flag.

### 6. Other Pins

ZRESET (input)

This is the LC895196K reset pin. The LC895196K is reset when this signal is low. This signal must be kept low for at least a period of 1 μs after power on.

XTALCK0, XTAL0

These cause oscillation at 33.8688 MHz. Frequencies from the outside may also be input into XTALCK0.

XTALCK1, XTAL1

Basically, these pins cannot oscillate. If these pins are not used, connect XTALCK1 (pin 100) to ground.

MCK (output)

This outputs the XTALCK1 and XTALCK1/2 frequencies. The output can also be turned off.

**MCK2 (output)**

This outputs the XTALCK0, XTALCK0/2, XTALCK0/5 and XTALCK0/512 frequencies. The output can also be turned off.

**MCK3 (output)**

This outputs the XTALCK0, XTALCK\*0/2, XTALCK0/5 and XTALCK0/512 frequencies. The output can also be turned off.

**ZRSTIC (output)**

The ZRSTIC output goes low when the microcontroller register R46-bit7 (ZSYSRET) or the ZHRST pin is put low. When both the ZSYSRET and ZHRST pins are high, ZRSTIC enters a high impedance state. Attach an external pull-up resistor.

**ZRSTCPU (output)**

When an ATAPI soft reset command (08h) is received, a low pulse is generated for approximately 1 ms (when XTALCK1 = 34 MHz). When this happens, an interrupt is sent to the microcontroller. When the ZRESET pin has become active, the ZRESET signal is output directly at the ZRSTCPU. Attach an external pull-up resistor.

**ATPINSEL (input)**

By changing the input to this pin, the ATAPI-side pin layout can be reversed.

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