



LC895925

Signal Processing LSI for CD-R Drives

Preliminary

Overview

The LC895925 provides the following signal processing functions for CD-R drives: CD-ROM decoding/encoding (complete with ECC processing for the former), subcode decoding/encoding, CD encoding, ATIP decoding, CLV servo, and SCSI interface registers.

Features

- CD-ROM decoding/encoding complete with error detection and error correction
- Subcode decoding/encoding complete with error correction
- ATIP decoding and CRC checking for both encoding and decoding
- CLV servo control using ATIP data during encoding
- CIRC code insertion and EFM modulation during encoding
- Support for PCA random EFM output during encoding
- Support for CD-ReWritable (CD-RW) Write Strategy signal output
- Access to buffer RAM from microcontroller via LC895925
- Built-in SCSI interface
- Speeds of 12× for decoding and 4× for encoding
 - Frequencies
 - Decoding: 17.2872 MHz
 - Encoding: 17.2872 MHz without Write Strategy support
 - 69.1488 MHz with Write Strategy support
- Transfers speeds of 10 megabytes/s (synchronous) and 5 megabytes/s (asynchronous) with 16 80-ns DRAMs *1

- Buffer RAM sizes between 1 and 32 megabits (using 16-bit DRAMs)
- User control over sizes of CD main channel, C2 flag, and subcode areas in buffer RAM
- Built-in batch transfer function for transferring entire CD main channel, C2 flag, or subcode area in a single operation
- Built-in multiblock transfer function for transferring multiple blocks in a single operation

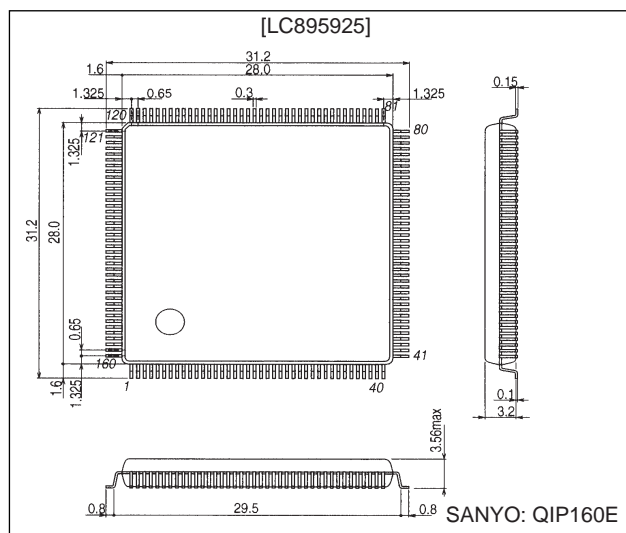
Notes:

1. Using a SCSI master clock of 20 MHz with speeds up to 8x.
2. Using a SCSI master clock of 17.2872 MHz with speeds up to 4x.

Package Dimensions

unit: mm

3153A-QFP160E



SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-0005 JAPAN

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V
I/O voltage	V_I, V_O		-0.3 to $V_{DD}+0.3$	V
Maximum power dissipation	$P_d\text{ max}$	$T_a \leq 70^\circ\text{C}$	600	mW
Operating temperature	T_{opr}		-30 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$
Solder resistance		10 seconds	260	$^\circ\text{C}$

Permissible Operating Range at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V_{IH}	TTL levels, for pin types 1 and 6	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input high level voltage	V_{IH}	TTL levels, for pin type 4, with pull-up resistors	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input high* level voltage	V_{IH}	TTL levels, for pin 0 and 7, with Schmitt inputs	2.5			V
Input low level voltage	V_{IL}				0.6	V
Output high level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$, for pin type 3	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin type 3			0.4	V
Output high level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$, for pin types 2, 4, and 6	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin types 2, 4, and 6			0.4	V
Output high level voltage	V_{OH}	$I_{OH} = -48\text{ mA}$, for pin type 7	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 48\text{ mA}$, for pin type 7			0.4	V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin type 5			0.4	V
Input leak current	I_{IL}	$V_I = V_{SS}, V_{DD}$, for pin types 0, 1, 6, and 7	-10		+10	μA
Pull-up resistance	R_{UP}	For pin types 4 and 5	40	80	160	$\text{k}\Omega$

The pin types above refer to the following groups.

Input

(0) BCK, BICKIN, BIDATAI, C2PO, LOCKIN, LRCK, PLLOUTIN, ROUGH, SBSO, SCOR, SDATA, WFCK, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$

(1) SUA0 to SUA6, TEST0 to TEST6, X1EN, $\overline{\text{RESET}}$

Output

(2) CLV^+ , CLV^- , FSW

(3) DATAKO, EFM, EFMG, EFMGATE0 to EFMGATE6, EXCK, LOCK, MCK, MON, PSUBSYNC, RA0 to RA9, SUBSYNC, CAS0 to CAS1, RAS0 to RAS1, ERROR, EXTACK, FRCK, LWE, UWE, OE

Input/Output

(4) D0 to D7, IO0 to IO15

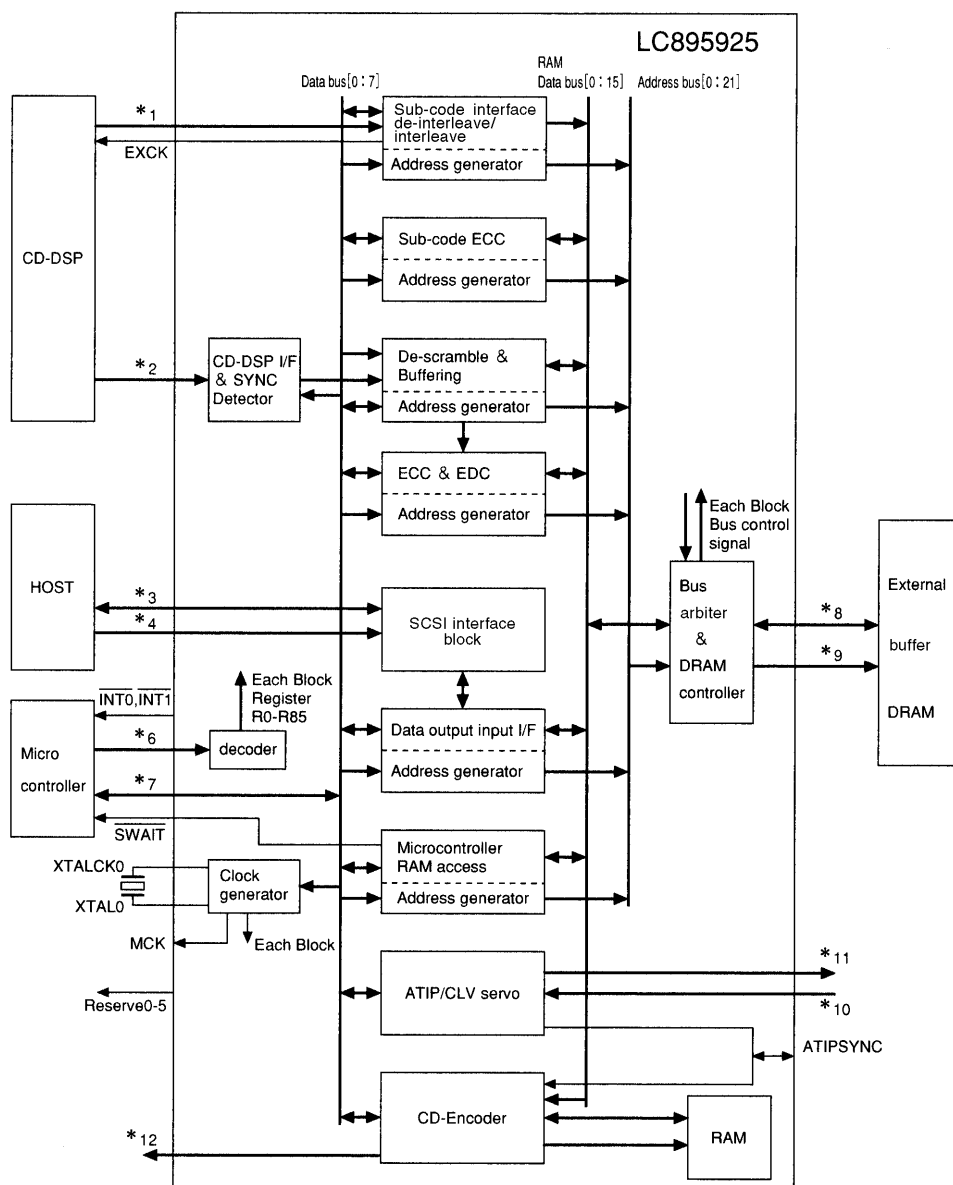
(5) INT0 to INT1, $\overline{\text{SWAIT}}$

(6) ATIPSYNC, Reserve0 to Reserve5

(7) $\overline{\text{ACK}}$, $\overline{\text{ATN}}$, $\overline{\text{BSY}}$, C/D, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, I/O, $\overline{\text{MSG}}$, $\overline{\text{REQ}}$, $\overline{\text{RST}}$, $\overline{\text{SEL}}$

Note: The XTAL0, XTAL1, XTALCK0, and XTALCK1 pins fall outside of these DC characteristic specifications.

Block Diagram



A09977

- *1 WFCK, SBSO, SCOR
- *2 BCK, SDATA, LRCK, C2PO
- *3 DB0 to DB7, DBP, BSY, MSG, SEL, RST, REQ, I/O, C/D
- *4 ACK, ATN
- *6 RD, WR, SUA0 to SUA6, CS
- *7 D0 to D7
- *8 IO0 to IO15
- *9 RA0 to RA9, RAS0, RAS1, CAS0, CAS1, OE, UWE, LWE
- *10 PLLOUTIN, ROUGH, LOCKIN, BICKIN, BIDATAIN
- *11 ERROR, LOCK, CLV⁺ (MDP), CLV⁻ (MDS), MON, FSW
- *12 SUBSYNC, PSUBSYNC, FRCK, EFM, EFMG, EFMGATE3 to EFMGATE0, EXTACK, DATAK0

Pin Descriptions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
1	V _{SS}	P	
2	Reserve0	B	Reserved for future expansion (leave open)
3	Reserve1	B	Reserved for future expansion (connect to ground)
4	Reserve2	B	Reserved for future expansion (connect to ground)
5	TEST1	I	Test pin (connect to V _{SS})
6	XTALCK0	I	Crystal oscillator circuit input pin (17.2872 to 69.1488 MHz)
7	XTAL0	O	Crystal oscillator circuit output pin
8	TEST2	I	Test pin (connect to V _{SS})
9	MCK	O	Master Clock output pin
10	TEST3	I	Test pin (connect to V _{SS})
11	XTALCK1	I	Crystal oscillator circuit input pin (20 MHz)
12	XTAL1	O	Crystal oscillator circuit output pin
13	TEST4	I	Test pin (connect to V _{SS})
14	V _{DD}	P	
15	V _{SS}	P	
16	CLV+ (MDP)	O	CLV servo signal output pins
17	CLV- (MDS)	O	
18	MON	O	
19	FSW	O	
20	V _{DD}	P	
21	V _{SS}	P	
22	PLLOUTIN	I	Wobble signal carrier clock input pin
23	ROUGH	I	Rough CLV servo wobble signal input pin
24	LOCKIN	I	CD decoder lock signal input pin
25	LOCK	O	CLV servo lock monitor pin
26	ERROR	O	ATIP parity error detection pin
27	ATIPSYNC	B	ATIP synchronization signal I/O pin
28	BIDATAI	I	Biphase data input pin
29	BICLKIN	I	Biphase data transfer clock input pin
30	V _{DD}	P	
31	IO0	B	Data signal pins for ROM encoder/decoder buffer RAM, with pull-up resistors
32	IO1	B	
33	IO2	B	
34	IO3	B	
35	IO4	B	
36	IO5	B	
37	IO6	B	
38	IO7	B	
39	IO8	B	
40	V _{DD}	P	
41	V _{SS}	P	

Continued on next page.

LC895925

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
42	IO9	B	Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors
43	IO10	B	
44	IO11	B	
45	IO12	B	
46	IO13	B	
47	IO14	B	
48	IO15	B	
49	V _{SS}	P	Address signal pins for ROM encoder/decoder DRAM
50	RA0	O	
51	RA1	O	
52	RA2	O	
53	RA3	O	
54	RA4	O	
55	RA5	O	
56	RA6	O	
57	RA7	O	
58	RA8	O	
59	RA9	O	
60	V _{DD}	P	DRAM $\overline{\text{RAS}}$ signal output pins
61	V _{SS}	P	
62	$\overline{\text{RAS0}}$	O	DRAM $\overline{\text{CAS}}$ signal output pins
63	$\overline{\text{RAS1}}$	O	
64	$\overline{\text{CAS0}}$	O	DRAM Output Enable signal output pin
65	$\overline{\text{CAS1}}$	O	
66	$\overline{\text{OE}}$	O	DRAM Output Upper Write Enable signal output pin
67	$\overline{\text{UWE}}$	O	
68	$\overline{\text{LWE}}$	O	DRAM Output Lower Write Enable signal output pin
69	TEST0	I	Test pin (connect to V _{SS})
70	V _{DD}	P	Subcode data read shift clock output pin
71	EXCK	O	
72	WFCK	I	Subcode frame synchronization input pin
73	SBSO	I	Subcode serial data input pin
74	SCOR	I	Subcode block synchronization input pin
75	V _{SS}	P	Serial data input clock input pin
76	BCK	I	
77	SDATA	I	Serial data input pin
78	LRCK	I	44.1-kHz strobe signal input pin
79	C2PO	I	C2 pointer input pin
80	V _{DD}	P	SCSI pins
81	V _{SS}	P	
82	$\overline{\text{DB0}}$	B	SCSI pins
83	$\overline{\text{DB1}}$	B	
84	V _{DD}	P	SCSI pins
85	$\overline{\text{DB2}}$	B	
86	$\overline{\text{DB3}}$	B	SCSI pins
87	V _{SS}	P	
88	$\overline{\text{DB4}}$	B	SCSI pins
89	$\overline{\text{DB5}}$	B	

Continued on next page.

LC895925

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
90	V _{DD}	P	
91	$\overline{\text{DB6}}$	B	SCSI pins
92	V _{DD}	P	
93	V _{SS}	P	
94	$\overline{\text{DB7}}$	B	SCSI pins
95	$\overline{\text{DBP}}$	B	
96	V _{DD}	P	
97	V _{SS}	P	
98	$\overline{\text{ATN}}$	B	SCSI pins
99	$\overline{\text{BSY}}$	B	
100	V _{DD}	P	
101	V _{SS}	P	
102	$\overline{\text{ACK}}$	B	SCSI pins
103	$\overline{\text{RST}}$	B	
104	V _{DD}	P	
105	V _{SS}	P	
106	$\overline{\text{MSG}}$	B	SCSI pins
107	$\overline{\text{SEL}}$	B	
108	V _{DD}	P	
109	C/D	B	SCSI pins
110	V _{DD}	P	
111	$\overline{\text{REQ}}$	B	SCSI pins
112	I/O	B	
113	V _{SS}	P	
114	X1EN	I	Pin for selecting SCSI interface clock (XTALCK0 or XTALCK1)
115	$\overline{\text{RESET}}$	I	RESET pin
116	V _{DD}	P	
117	DATACKO	O	4.3218-MHz (Normal Speed) oscillator output pin
118	PSUBSYNC	O	Pseudo subcode synchronization output pin
119	$\overline{\text{EXTACK}}$	O	ATIP synchronization interval acknowledgment output pin
120	V _{DD}	P	
121	V _{SS}	P	
122	SUBSYNC	O	Subcode synchronization signal output pin
123	$\overline{\text{FRCK}}$	O	EFM frame synchronization signal output pin
124	FRCK	O	EFM output gate signal output pin
125	EFM	O	EFM signal output pin
126	EFMGATE0	O	EFM pulse width detection gate signals
127	EFMGATE1	O	
128	EFMGATE2	O	
129	EFMGATE3	O	
130	TEST5	I	Test pin (connect to V _{SS})
131	V _{SS}	P	
132	TEST6	I	Test pin (connect to V _{SS})

Continued on next page.

LC895925

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
133	SUA0	I	Command register selection address input pins
134	SUA1	I	
135	SUA2	I	
136	SUA3	I	
137	SUA4	I	
138	SUA5	I	
139	SUA6	I	
140	V _{DD}	P	Microcontroller data signal pins, with pull-up resistors
141	V _{SS}	P	
142	D0	B	
143	D1	B	
144	D2	B	
145	D3	B	
146	D4	B	
147	D5	B	Interrupt request signals to microcontroller. Open drain outputs with built-in pull-up resistors
148	D6	B	
149	D7	B	
150	V _{DD}	P	
151	\overline{CS}	I	
152	\overline{RD}	I	
153	\overline{WR}	I	
154	\overline{WAIT}	O	Reserved for future expansion (leave open)
155	$\overline{INT0}$	O	
156	$\overline{INT1}$	O	
157	Reserve3	B	
158	Reserve4	B	Reserved for future expansion (leave open)
159	Reserve5	B	
160	V _{DD}	P	

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of December, 1997. Specifications and information herein are subject to change without notice.