

**LC895926****CD-R Encoder/Decoder IC with Built-in SCSI Interface****Overview**

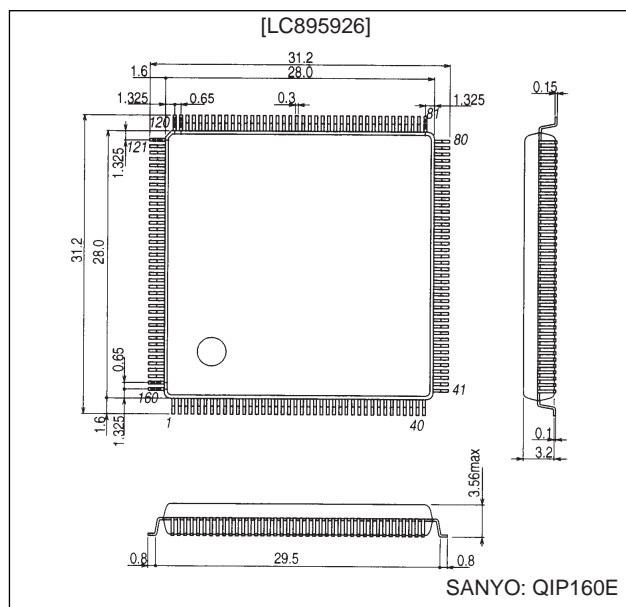
The LC895926 is a CD-R IC that provides a wide range of functions including CD-ROM decoding (including ECC) and encoding, subcode encoding and decoding, CD encoding, ATIP decoding and CLV servo, and a SCSI interface that includes the register block.

**Features**

- ECC and EDC correction/addition for CD-ROM data (during decoding and encoding)
- Subcode decoding/encoding complete with error detection and error correction
- ATIP decoding and CRC checking for both encoding and decoding
- CLV servo control using ATIP data during encoding
- CIRC code insertion and EFM modulation during encoding
- Access to buffer RAM from microcontroller via LC895926
- Built-in SCSI interface
- Speeds of 24× for decoding and 12× for encoding
- Transfers speeds of 10 megabytes/s (synchronous) and 5 megabytes/s (asynchronous) with 16-bit 50-ns EDO-DRAMs
- Buffer RAM sizes between 1 and 32 megabits (using 16-bit EDO-DRAMs)
- User control over sizes of CD main channel, C2 flag, and subcode areas in buffer RAM
- Built-in batch transfer function for transferring entire CD main channel, C2 flag, or subcode area in a single operation.
- Built-in multiblock transfer function for transferring multiple blocks in a single operation.
- Automatic sequencing of encoding and decoding processing for a reduced processing load on the system microcontroller.

**Package Dimensions**

unit: mm

**3153A-QFP160E**

## Specifications

**Absdute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V**

| Parameter                     | Symbol                          | Conditions | Ratings                      | Unit |
|-------------------------------|---------------------------------|------------|------------------------------|------|
| Maximum power supply voltage  | V <sub>DD</sub> max             |            | −0.3 to +7.0                 | V    |
| I/O voltage                   | V <sub>I</sub> , V <sub>O</sub> |            | −0.3 to V <sub>DD</sub> +0.3 | V    |
| Allowable power dissipation   | Pd max                          | Ta ≤ 70°C  | 600                          | mW   |
| Operating temperature         | Topr                            |            | −30 to +70                   | °C   |
| Storage temperature           | Tstg                            |            | −55 to +125                  | °C   |
| Solder resistance (Pins only) |                                 | 10 seconds | 260                          | °C   |

**Allowable Operating Ranges at Ta = −30 to +70°C, V<sub>SS</sub> = 0 V**

| Parameter            | Symbol          | 3.3V |     |                 | 5V  |     |                 | Unit |
|----------------------|-----------------|------|-----|-----------------|-----|-----|-----------------|------|
|                      |                 | min  | typ | max             | min | typ | max             |      |
| Power supply voltage | V <sub>DD</sub> | 3.0  | 3.3 | 3.6             | 4.5 | 5.0 | 5.5             | V    |
| Input voltage range  | V <sub>IN</sub> | 0    |     | V <sub>DD</sub> | 0   |     | V <sub>DD</sub> | V    |

**DC Characteristics at Ta = −30 to +70°C, V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 5.5 V**

| Parameter                 | Symbol          | Conditions   | Ratings               |     |     | Unit |
|---------------------------|-----------------|--|-----------------------|-----|-----|------|
|                           |                 |  | min                   | typ | max |      |
| Input high level voltage  | V <sub>IH</sub> | TTL levels, for pins (1) and (6)   | 2.2                   |     |     | V    |
| Input low level voltage   | V <sub>IL</sub> |  |                       |     | 0.8 | V    |
| Input high level voltage  | V <sub>IH</sub> | TTL levels, for pin (4), with pull-up resistors                                      | 2.2                   |     |     | V    |
| Input low level voltage   | V <sub>IL</sub> |  |                       |     | 0.8 | V    |
| Input high level voltage  | V <sub>IH</sub> | TTL levels, for pins (0) and (7), with Schmitt inputs                                | 2.5                   |     |     | V    |
| Input low level voltage   | V <sub>IL</sub> |  |                       |     | 0.6 | V    |
| Output high level voltage | V <sub>OH</sub> | I <sub>OH</sub> = −2 mA, for pin (3)   | V <sub>DD</sub> − 2.1 |     |     | V    |
| Output low level voltage  | V <sub>OL</sub> | I <sub>OL</sub> = 2 mA, for pin (3)  |                       |     | 0.4 | V    |
| Output high level voltage | V <sub>OH</sub> | I <sub>OH</sub> = −2 mA, for pins (2), (4), and (6)                                  | V <sub>DD</sub> − 2.1 |     |     | V    |
| Output low level voltage  | V <sub>OL</sub> | I <sub>OL</sub> = 2 mA, for pins (2), (4), and (6)                                   |                       |     | 0.4 | V    |
| Output high level voltage | V <sub>OH</sub> | I <sub>OH</sub> = −48 mA, for pin (7)  | V <sub>DD</sub> − 2.1 |     |     | V    |
| Output low level voltage  | V <sub>OL</sub> | I <sub>OL</sub> = 48 mA, for pin (7)   |                       |     | 0.4 | V    |
| Output low level voltage  | V <sub>OL</sub> | I <sub>OL</sub> = 2 mA, for pin (5)  |                       |     | 0.4 | V    |
| Input leak current        | I <sub>IL</sub> | V <sub>I</sub> = V <sub>SS</sub> , V <sub>DD</sub> , for pins (0), (1), (6), and (7) | −10                   |     | +10 | μA   |
| Pull-up resistance        | R <sub>UP</sub> | For pins (4) and (5)   | 40                    | 80  | 160 | kΩ   |

The pins above refer to the following groups.

### Input

- (0) BCK, BICKIN, BIDATAI, C2PO, LOCKIN, LRCK, PLLOUTIN, ROUGH, SBSO, SCOR, SDATA, WFCK,  $\overline{\text{CS}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$   
 (1) SUA0 to SUA7, TEST0 to TEST6,  $\overline{\text{RESET}}$

### Output

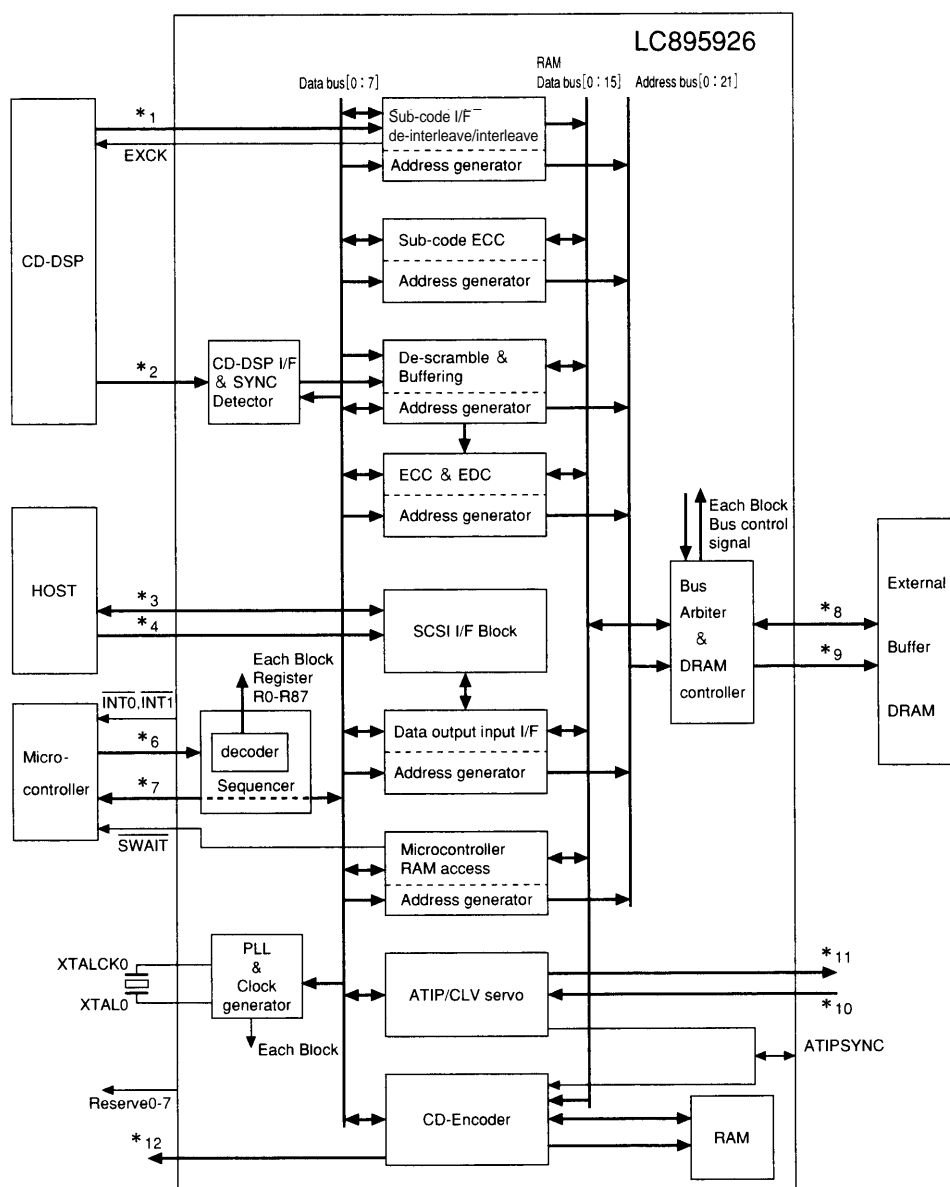
- (2) CLV<sup>+</sup>, CLV<sup>−</sup>, FSW  
 (3) EFM, EFMG, EFMGATE0 to EFMGATE3, EXCK, LOCK, MON, RA0 to RA9, SUBSYNC,  $\overline{\text{CAS0}}$  to  $\overline{\text{CAS1}}$ ,  $\overline{\text{RAS0}}$  to  $\overline{\text{RAS1}}$ ,  $\overline{\text{LWE}}$ ,  $\overline{\text{UWE}}$ ,  $\overline{\text{OE}}$

### Input

- (4) D0 to D7, IO0 to IO15  
 (5)  $\overline{\text{INT0}}$  to  $\overline{\text{INT1}}$ ,  $\overline{\text{SWAIT}}$   
 (6)  $\overline{\text{ATIPSYNC}}$ ,  $\overline{\text{Reserve0}}$  to  $\overline{\text{Reserve7}}$   
 (7)  $\overline{\text{ACK}}$ ,  $\overline{\text{ATN}}$ ,  $\overline{\text{BSY}}$ ,  $\overline{\text{C/D}}$ ,  $\overline{\text{DB0}}$  to  $\overline{\text{DB7}}$ ,  $\overline{\text{DBP}}$ ,  $\overline{\text{I/O}}$ ,  $\overline{\text{MSG}}$ ,  $\overline{\text{REQ}}$ ,  $\overline{\text{RST}}$ ,  $\overline{\text{SEL}}$

Note: The XTAL0, XTAL1, XTALCK0, and XTALCK1 pins are not included in these DC characteristic specifications.

## Block Diagram



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- \*1 WFCK, SBSO, SCOR
- \*2 BCK, SDATA, LRCK, C2PO
- \*3 DB0 to DB7, DBP, BSY, MSG, SEL, RST, REQ, I/O, C/D
- \*4 ACK, ATN
- \*6 RD, WR, SUA0 to SUA7, CS
- \*7 D0 to D7
- \*8 IO0 to IO15
- \*9 RA0 to RA9, RAS0, RAS1, CAS0, CAS1, OE, UWE, LWE
- \*10 PLLOUTIN, ROUGH, LOCKIN, BICLKIN, BIDATAIN
- \*11 LOCK, CLV<sup>+</sup> (MDP), CLV<sup>-</sup> (MDS), MON, FSW
- \*12 SUBSYNC, EFM, EFMG, EFMGATE0 to EFMGATE3

## Pin Descriptions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

| Pin Number | Pin Name               | Type | Description   |
|------------|------------------------|------|---|
| 1          | V <sub>SS</sub>        | P    |   |
| 2          | XTALCK0                | I    | Xtal oscillator circuit input pin (17.2872 MHz)                       |
| 3          | XTAL0                  | O    | Xtal oscillator circuit output pin                                    |
| 4          | TEST0                  | I    | Test pin (connect to V <sub>SS</sub> )                                |
| 5          | RESET                  | I    | Reset pin   |
| 6          | V <sub>DD</sub>        | P    | 5V  |
| 7          | SUBSYNC                | O    | Subcode synchronization signal output pin                             |
| 8          | EFMG                   | O    | EFM output gate signal output pin                                     |
| 9          | EFM                    | O    | EFM signal output pin   |
| 10         | EFMGATE0               | O    | EFM pulse width detection gate signals                                |
| 11         | EFMGATE1               | O    |   |
| 12         | EFMGATE2               | O    |   |
| 13         | EFMGATE3               | O    |   |
| 14         | TEST1                  | I    | Test pin (connect to V <sub>SS</sub> )                                |
| 15         | Reserve0               | B    | Reserved for future expansion (connect to V <sub>SS</sub> if unused.) |
| 16         | Reserve1               | B    |   |
| 17         | Reserve2               | B    |   |
| 18         | Reserve3               | B    |   |
| 19         | Reserve4               | B    |   |
| 20         | V <sub>DD</sub>        | P    | 3.3V  |
| 21         | V <sub>SS</sub>        | P    |   |
| 22         | Reserve5               | B    | Reserved for future expansion (connect to V <sub>SS</sub> if unused.) |
| 23         | Reserve6               | B    |   |
| 24         | Reserve7               | B    |   |
| 25         | TEST2                  | I    | Test pin (connect to V <sub>SS</sub> )                                |
| 26         | LOCKIN                 | I    | CD decoder lock signal input pin                                      |
| 27         | LOCK                   | O    | CLV servo lock monitor pin  |
| 28         | PLL0UTIN               | I    | Wobble signal carrier clock input pin                                 |
| 29         | V <sub>SS</sub>        | P    |   |
| 30         | ROUGH                  | I    | Rough CLV servo wobble signal input pin                               |
| 31         | ATIPSYNC               | B    | ATIP synchronization signal I/O pin                                   |
| 32         | BICKIN                 | I    | Biphase data transfer clock input pin                                 |
| 33         | BIDATAI                | I    | Biphase data input pin  |
| 34         | V <sub>DD</sub>        | P    | 3.3V  |
| 35         | V <sub>SS</sub>        | P    |   |
| 36         | CLV <sup>+</sup> (MDP) | O    | CLV servo signal output pin   |
| 37         | CLV <sup>-</sup> (MDS) | O    |   |
| 38         | MON                    | O    |   |
| 39         | FSW                    | O    |   |
| 40         | V <sub>DD</sub>        | P    | 5V  |
| 41         | V <sub>SS</sub>        | P    |   |

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# LC895926

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

| Pin Number | Pin Name                 | Type | Description   |
|------------|--------------------------|------|---|
| 42         | IO0                      | B    | Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors |
| 43         | IO1                      | B    |   |
| 44         | IO2                      | B    |   |
| 45         | IO3                      | B    |   |
| 46         | IO4                      | B    |   |
| 47         | IO5                      | B    |   |
| 48         | V <sub>DD</sub>          | P    | 5V  |
| 49         | IO6                      | B    | Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors |
| 50         | IO7                      | B    |   |
| 51         | IO8                      | B    |   |
| 52         | IO9                      | B    |   |
| 53         | V <sub>SS</sub>          | P    |   |
| 54         | IO10                     | B    | Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors |
| 55         | IO11                     | B    |   |
| 56         | IO12                     | B    |   |
| 57         | IO13                     | B    |   |
| 58         | IO14                     | B    |   |
| 59         | IO15                     | B    |   |
| 60         | V <sub>DD</sub>          | P    | 3.3V  |
| 61         | V <sub>SS</sub>          | P    |   |
| 62         | RA0                      | O    | Address signal pins for ROM encoder/decoder DRAM                      |
| 63         | RA1                      | O    |   |
| 64         | RA2                      | O    |   |
| 65         | RA3                      | O    |   |
| 66         | RA4                      | O    |   |
| 67         | RA5                      | O    |   |
| 68         | RA6                      | O    |   |
| 69         | V <sub>SS</sub>          | P    |   |
| 70         | RA7                      | O    | Address signal pins for ROM encoder/decoder DRAM                      |
| 71         | RA8                      | O    |   |
| 72         | RA9                      | O    |   |
| 73         | $\overline{\text{RAS}}0$ | O    | $\overline{\text{RAS}}$ signal pins for ROM encoder/decoder DRAM      |
| 74         | $\overline{\text{RAS}}1$ | O    |   |
| 75         | $\overline{\text{CAS}}0$ | O    | $\overline{\text{CAS}}$ signal pins for ROM encoder/decoder DRAM      |
| 76         | $\overline{\text{CAS}}1$ | O    |   |
| 77         | $\overline{\text{OE}}$   | O    | Output enable signal pin for ROM encoder/decoder DRAM                 |
| 78         | $\overline{\text{UWE}}$  | O    | Upper write enable signal pin for ROM encoder/decoder DRAM            |
| 79         | $\overline{\text{LWE}}$  | O    | Lower write enable signal pin for ROM encoder/decoder DRAM            |
| 80         | V <sub>DD</sub>          | P    | 5V  |
| 81         | V <sub>SS</sub>          | P    |   |
| 82         | $\overline{\text{DB}}0$  | B    | SCSI pins   |
| 83         | $\overline{\text{DB}}1$  | B    |   |
| 84         | V <sub>DD</sub>          | P    | 3.3V  |
| 85         | $\overline{\text{DB}}2$  | B    | SCSI pins   |
| 86         | $\overline{\text{DB}}3$  | B    |   |
| 87         | V <sub>SS</sub>          | P    |   |
| 88         | $\overline{\text{DB}}4$  | B    | SCSI pins   |
| 89         | $\overline{\text{DB}}5$  | B    |   |

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## LC895926

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power Supply pin, N: No connection pin

| Pin Number | Pin Name         | Type | Description   |
|------------|------------------|------|---|
| 90         | V <sub>DD</sub>  | P    | 3.3V  |
| 91         | $\overline{DB6}$ | B    | SCSI pin  |
| 92         | V <sub>DD</sub>  | P    | 5V  |
| 93         | V <sub>SS</sub>  | P    |   |
| 94         | $\overline{DB7}$ | B    | SCSI pins   |
| 95         | $\overline{DBP}$ | B    |   |
| 96         | V <sub>DD</sub>  | P    | 5V  |
| 97         | V <sub>SS</sub>  | P    |   |
| 98         | $\overline{ATN}$ | B    | SCSI pin  |
| 99         | $\overline{BSY}$ | B    | SCSI pin  |
| 100        | V <sub>DD</sub>  | P    | 5V  |
| 101        | V <sub>SS</sub>  | P    |   |
| 102        | $\overline{ACK}$ | B    | SCSI pins   |
| 103        | $\overline{RST}$ | B    |   |
| 104        | V <sub>DD</sub>  | P    | 5V  |
| 105        | V <sub>SS</sub>  | P    |   |
| 106        | $\overline{MSG}$ | B    | SCSI pins   |
| 107        | $\overline{SEL}$ | B    |   |
| 108        | V <sub>DD</sub>  | P    | 3.3V  |
| 109        | C/D              | B    | SCSI pin  |
| 110        | V <sub>DD</sub>  | P    | 5V  |
| 111        | $\overline{REQ}$ | B    | SCSI pins   |
| 112        | I/O              | B    |   |
| 113        | V <sub>SS</sub>  | P    |   |
| 114        | XTALCK1          | I    | Xtal oscillator circuit input pin for SCSI interface (20 MHz) |
| 115        | XTAL1            | O    | Xtal oscillator circuit output pin for SCSI interface         |
| 116        | TEST3            | I    | Test pin (connect to V <sub>SS</sub> )                        |
| 117        | TEST4            | I    | Test pin (connect to V <sub>SS</sub> )                        |
| 118        | TEST5            | I    | Test pin (connect to V <sub>SS</sub> )                        |
| 119        | BCK              | I    | Serial data input clock input pin                             |
| 120        | V <sub>DD</sub>  | P    | 5V  |
| 121        | V <sub>SS</sub>  | P    |   |
| 122        | SDATA            | I    | Serial data input pin   |
| 123        | LRCK             | I    | 44.1 kHz strobe signal input pin                              |
| 124        | C2PO             | I    | C2 pointer input pin  |
| 125        | EXCK             | O    | Subcode data read shift clock output pin                      |
| 126        | WFCK             | I    | Subcode frame synchronization input pin                       |
| 127        | SBSO             | I    | Subcode serial data input pin                                 |
| 128        | SCOR             | I    | Subcode block synchronization input pin                       |
| 129        | V <sub>SS</sub>  | P    |   |
| 130        | SUA0             | I    | Commande register selection address input pins                |
| 131        | SUA1             | I    |   |
| 132        | SUA2             | I    |   |
| 133        | SUA3             | I    |   |
| 134        | SUA4             | I    |   |
| 135        | SUA5             | I    |   |
| 136        | SUA6             | I    |   |
| 137        | SUA7             | I    |   |

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power Supply pin, N: No connection pin

| Pin Number | Pin Name           | Type | Description  |
|------------|--------------------|------|--|
| 138        | $\overline{WR}$    | I    | Data write signal from microcontroller   |
| 139        | $\overline{RD}$    | I    | Data read signal from microcontroller  |
| 140        | $V_{DD}$           | P    | 3.3V   |
| 141        | $V_{SS}$           | P    |  |
| 142        | $\overline{CS}$    | I    | Chip select signal from microcontroller  |
| 143        | D0                 | B    | Microcontroller data signal pins, with pull-up resistors   |
| 144        | D1                 | B    |  |
| 145        | D2                 | B    |  |
| 146        | D3                 | B    |  |
| 147        | D4                 | B    |  |
| 148        | D5                 | B    |  |
| 149        | D6                 | B    |  |
| 150        | D7                 | B    |  |
| 151        | $\overline{SWAIT}$ | O    | Wait signal to microcontroller   |
| 152        | $V_{DD}$           | P    | 5V   |
| 153        | $\overline{INT0}$  | O    | Interrupt request signals to microcontroller. Open drain outputs with built-in pull-up resistors |
| 154        | $\overline{INT1}$  | O    |  |
| 155        | TEST6              | I    | Test pin (connect to $V_{SS}$ )  |
| 156        | PD                 | O    | Charge pump output pin   |
| 157        | VCNT               | I    | VCO control voltage pin  |
| 158        | R                  | I    | VCO bias resistor pin  |
| 159        | $V_{SS}$           | P    |  |
| 160        | $V_{DD}$           | P    | 3.3V   |

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