

**LC895994**

CD-R Encoder/Decoder LSI with Built-in ATAPI (IDE) Interface

Preliminary

Overview

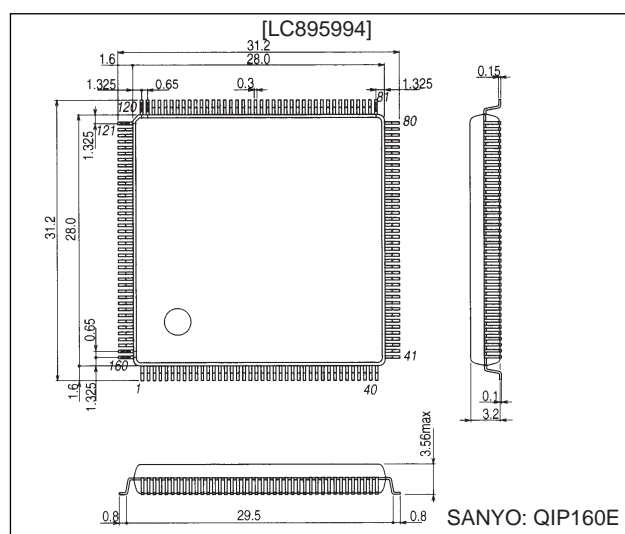
The LC895994 is a CD-R LSI that provides a wide range of functions including CD-ROM decoding (including ECC) and encoding, subcode Q encoding (CRC addition) and decoding, CD encoding, ATIP decoding and CLV servo, and an IDE interface that includes the register block.

Features

- ECC and EDC correction/addition for the CD-ROM data (during decoding and encoding)
- ATIP decoding and CRC checking for both encoding and decoding
- CLV servo control using ATIP data during encoding
- CIRC code insertion and EFM modulation during encoding
- Support for PCA random EFM output during encoding
- Support for CD-ReWritable (CD-RW) Write Strategy signal output
- Access to buffer RAM from microcontroller via LC895994
- Built-in ATAPI (IDE) interface
- Speeds of 12× for decoding and 4× for encoding
 - Frequencies
 - Decoding: 17.2872 MHz
 - Encoding: 17.2872 MHz without Write Strategy support
69.1488 MHz with Write Strategy support
- IDE Transfer rate: 13.3 MB/s when using 16-bit data path 80-ns DRAM chips
- Buffer RAM sizes between 1 and 32 megabits (using 16-bit DRAMs)
- User control over sizes of CD main channel, C2 flag areas in buffer RAM
- Built-in batch transfer function for transferring entire CD main channel, C2 flag, or subcode area in a single operation
- Built-in multiblock transfer function for transferring multiple blocks in a single operation

Package Dimensions

unit: mm

3153A-QFP160E

Specifications

Maximum Ratings at $T_a = 25^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V
I/O voltage	V_I, V_O		-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 70^{\circ}\text{C}$	600	mW
Operating temperature	T_{opr}		-30 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$
Solder resistance (Pins only)		10 seconds	260	$^{\circ}\text{C}$

Allowable Operating Range at $T_a = -30\text{ to }+70^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at $T_a = -30\text{ to }+70^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}	TTL levels, for pin types 1 and 7	2.2			V
Input low-level voltage	V_{IL}				0.8	V
Input high-level voltage	V_{IH}	TTL levels, for pin types 8 and 9, with pull-up resistors	2.2			V
Input low-level voltage	V_{IL}				0.8	V
Input high-level voltage	V_{IH}	TTL levels, for pin types 2 and 10, with Schmitt inputs	2.5			V
Input low-level voltage	V_{IL}				0.6	V
Output high-level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$, for pin type 6	$V_{DD} - 2.1$			V
Output low-level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin type 6			0.4	V
Output high-level voltage	V_{OH}	$I_{OH} = -24\text{ mA}$, for pin type 3	$V_{DD} - 2.1$			V
Output low-level voltage	V_{OL}	$I_{OL} = 24\text{ mA}$, for pin type 3			0.4	V
Output high-level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$, for pin types 4, 7, and 8	$V_{DD} - 2.1$			V
Output low-level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin types 4, 7, and 8			0.4	V
Output high-level voltage	V_{OH}	$I_{OH} = -24\text{ mA}$, for pin types 5 and 10	$V_{DD} - 2.1$			V
Output low-level voltage	V_{OL}	$I_{OL} = 24\text{ mA}$, for pin types 5 and 10			0.4	V
Output low-level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin type 9.			0.4	V
Input leakage current	I_{IL}	$V_I = V_{SS}, V_{DD}$, for pin types 1, 2, 7, and 10	-10		+10	μA
Output leakage current		When set to high-impedance output: For pin types 4, 5, 7, and 10.	-10		+10	μA
Pull-up resistance	R_{UP}	For pin types 8 and 9	40	80	160	$\text{k}\Omega$

The pin types above refer to the following groups.

Input

(1) SUA0 to SUA7, TEST0 to TEST6, $\overline{\text{RESET}}$

(2) BCK, BICKIN, BIDATAI, C2PO, DA0 to DA2, LOCKIN, LRCK, PLLOUTIN, ROUGH, SBSO, SCOR, SDATA, WFCCK, $\overline{\text{CS}}$, $\overline{\text{CS1FX}}$, $\overline{\text{CS3FX}}$, DIOR, DIOW, DMACK, HRST, RD, WR

Output

(3) EFM

(4) CLVMDP, CLVMDS, FSW

(5) DMARQ, HINTRQ, IORDY, $\overline{\text{IOCS16}}$

(6) DATAACKO, EFMG, EFMGATE0 to EFMGATE3, EXCK, LOCK, MCK, MON, PSUBSYNC, RA0 to RA9, SUBSYNC, CAS0, CAS1, ERROR, EXTACK, FRCK, LOWE, OE, RAS0, RAS1, UWE

Input

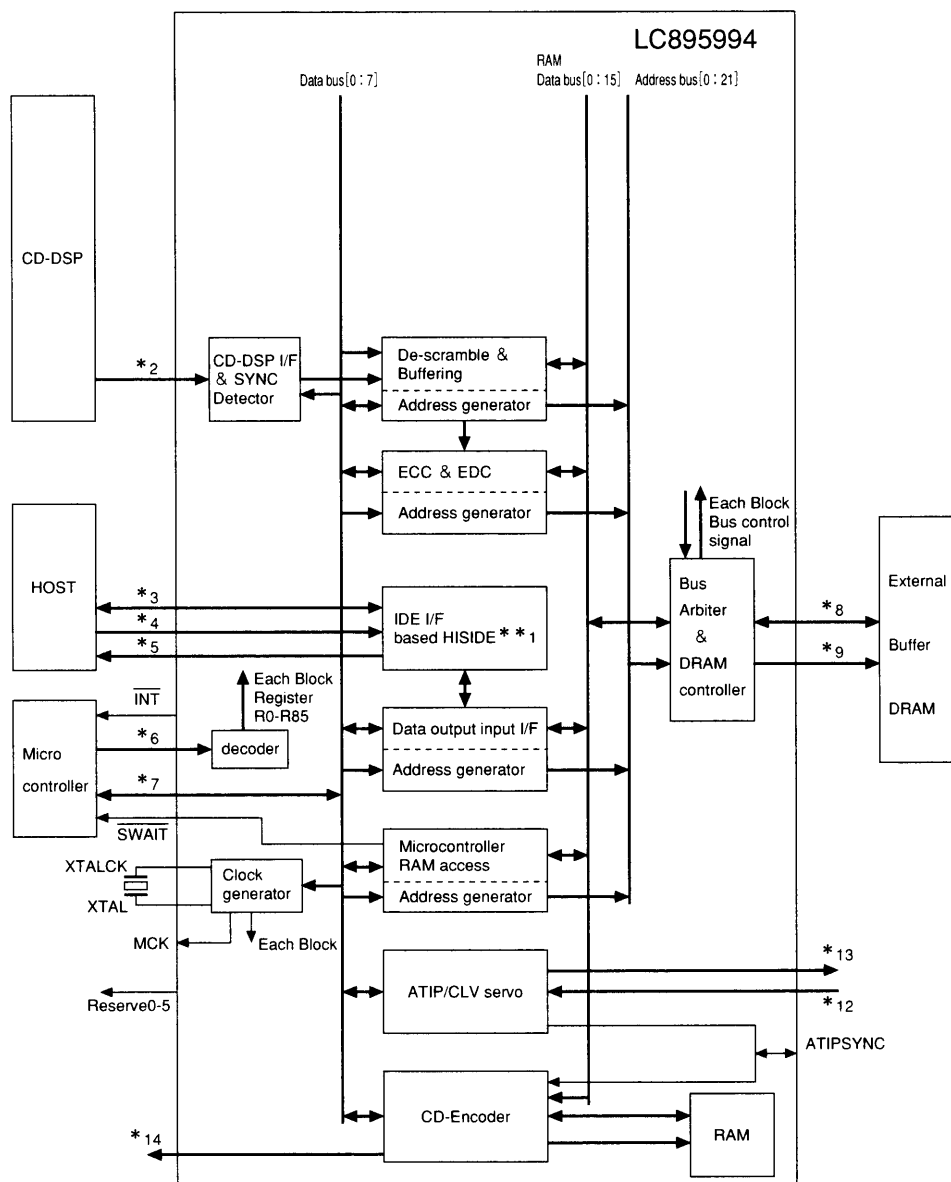
(7) ATIPSYNC, Reserve0 to Reserve5

(8) D0 to D7, IO0 to IO15

(9) $\overline{\text{INT0}}$ to $\overline{\text{INT1}}$, $\overline{\text{SWAIT}}$

(10) DD0 to DD15, $\overline{\text{DASP}}$, $\overline{\text{PDIAG}}$

Block Diagram



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- *2 BCK, SDATA, LRCK, C2PO
- *3 DD0 to DD15, $\overline{\text{DASP}}$, $\overline{\text{PDIAG}}$
- *4 $\overline{\text{CS1FX}}$, $\overline{\text{CS3FX}}$, DA0 to DA2, $\overline{\text{DIOR}}$, $\overline{\text{DIOW}}$, $\overline{\text{DMACK}}$
- *5 $\overline{\text{DMARQ}}$, $\overline{\text{HINTRQ}}$, $\overline{\text{IOCS16}}$, $\overline{\text{IORDY}}$
- *6 $\overline{\text{RD}}$, $\overline{\text{WR}}$, SUA0 to SUA6, $\overline{\text{CS}}$
- *7 D0 to D7
- *8 IO0 to IO15
- *9 RA0 to RA9, $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$, $\overline{\text{OE}}$, $\overline{\text{UWE}}$, $\overline{\text{LWE}}$
- *10 PLLOUTIN, ROUGH, LOCKIN, BICLKIN, BIDATAIN
- *11 $\overline{\text{ERROR}}$, LOCK, CLV^+ (MDP), CLV^- (MDS), MON, FSW
- *12 SUBSYNC, PSUBSYNC, FRCK, EFM, EFMG, EFMGATE3 to EFMGATE0, EXTACK, DATAACKO
- **1 HISIDE (WD25C32) is made by WESTERN DIGITAL.

Pin Descriptions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin No.	Pin Name	Type	Description
1	V _{SS}	P	
2	Reserve0	O	Reserved for future expansion (Must be left open if unused.)
3	Reserve1	I	Reserved for future expansion (Must be tied to ground if unused.)
4	Reserve2	I	Reserved for future expansion (Must be tied to ground if unused.)
5	TEST1	I	Test pin (connect to V _{SS})
6	XTALCK	I	Crystal oscillator circuit input pin (17.2872 to 69.1488 MHz)
7	XTAL	O	Crystal oscillator circuit output pin
8	TEST2	I	Test pin (connect to V _{SS})
9	MCK	O	Master Clock output pin
10	TEST3	I	Test pin (connect to V _{SS})
11	PSUBSYNC	O	Pseudo-subcode synchronization output
12	EXTACK	O	ATIP synchronization acknowledge signal output
13	TEST4	I	Test pin (connect to V _{SS})
14	V _{DD}	P	
15	V _{SS}	P	
16	CLV+ (MDP)	O	CLV servo signal output pins
17	CLV- (MDS)	O	
18	MON	O	
19	FSW	O	
20	V _{DD}	P	
21	V _{SS}	P	
22	PLLOUTIN	I	Wobble signal carrier clock input pin
23	ROUGH	I	Rough CLV servo wobble signal input pin
24	LOCKIN	I	CD decoder lock signal input pin
25	LOCK	O	CLV servo lock monitor pin
26	ERROR	O	ATIP parity error detection pin
27	ATIPSYNC	B	ATIP synchronization signal I/O pin
28	BIDATAI	I	Biphase data input pin
29	BICLKIN	I	Biphase data transfer clock input pin
30	DATAACKO	O	4.3218 MHz (normal speed) oscillator output
31	IO0	B	Data signal pins for ROM encoder/decoder buffer RAM, with pull-up resistors
32	IO1	B	
33	IO2	B	
34	IO3	B	
35	IO4	B	
36	IO5	B	
37	IO6	B	
38	IO7	B	
39	IO8	B	
40	V _{DD}	P	
41	V _{SS}	P	

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Pin No.	Pin Name	Type	Description
42	IO9	B	Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors
43	IO10	B	
44	IO11	B	
45	IO12	B	
46	IO13	B	
47	IO14	B	
48	IO15	B	
49	V _{SS}	P	Address signal pins for ROM encoder/decoder DRAM
50	RA0	O	
51	RA1	O	
52	RA2	O	
53	RA3	O	
54	RA4	O	
55	RA5	O	
56	RA6	O	
57	RA7	O	
58	RA8	O	
59	RA9	O	
60	V _{DD}	P	DRAM $\overline{\text{RAS}}$ signal output pins
61	V _{SS}	P	
62	$\overline{\text{RAS0}}$	O	DRAM $\overline{\text{CAS}}$ signal output pins
63	$\overline{\text{RAS1}}$	O	
64	$\overline{\text{CAS0}}$	O	DRAM output enable signal output pin
65	$\overline{\text{CAS1}}$	O	
66	$\overline{\text{OE}}$	O	DRAM upper write enable signal output pin
67	$\overline{\text{UWE}}$	O	
68	$\overline{\text{LWE}}$	O	DRAM lower write enable signal output pin
69	TEST0	I	
70	V _{DD}	P	Test pin (connect to V _{SS})
71	EXCK	O	
72	WFCK	I	Subcode data read shift clock output pin
73	SBSO	I	Subcode frame synchronization input pin
74	SCOR	I	Subcode serial data input pin
75	V _{SS}	P	Subcode block synchronization input pin
76	BCK	I	Serial data input clock input pin
77	SDATA	I	
78	LRCK	I	Serial data input pin
79	C2PO	I	
80	V _{DD}	P	44.1-kHz strobe signal input pin
81	V _{SS}	P	
82	$\overline{\text{HRST}}$	I	C2 pointer input pin
83	$\overline{\text{DASP}}$	B	
84	$\overline{\text{CS3FX}}$	I	
85	$\overline{\text{CS1FX}}$	I	IDE pins
86	V _{DD}	P	
87	DA2	I	
88	DA0	I	
89	$\overline{\text{PDIAG}}$	B	IDE pins

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power Supply pin, N: No connection pin

Pin No.	Pin Name	Type	Description
90	DA1	I	IDE pins
91	$\overline{\text{IOCS16}}$	O	
92	INTRQ	O	
93	V _{SS}	P	
94	$\overline{\text{DMACK}}$	I	IDE pins
95	$\overline{\text{IORDY}}$	O	
96	$\overline{\text{DIOR}}$	I	
97	$\overline{\text{DIOW}}$	I	
98	DMARQ	O	
99	DD15	B	
100	V _{DD}	P	
101	V _{SS}	P	
102	DD0	B	IDE pins
103	DD14	B	
104	DD1	B	
105	DD13	B	
106	DD2	B	
107	V _{SS}	P	
108	DD12	B	IDE pins
109	DD3	B	
110	DD11	B	
111	V _{SS}	P	
112	DD4	B	IDE pins
113	DD10	B	
114	DD5	B	
115	V _{SS}	P	
116	DD9	B	IDE pins
117	DD6	B	
118	DD8	B	
119	DD7	B	
120	V _{DD}	P	
121	V _{SS}	P	
122	SUBSYNC	O	Subcode synchronization signal output pin
123	FRCK	O	EFM frame synchronization signal output pin
124	EFMG	O	EFM output gate signal output pin
125	EFM	O	EFM signal output pin
126	EFMGATE0	O	EFM pulse width detection gate signals
127	EFMGATE1	O	
128	EFMGATE2	O	
129	EFMGATE3	O	
130	TEST5	I	Test pin (connect to V _{SS})
131	V _{SS}	P	
132	TEST6	I	Test pin (connect to V _{SS})

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Pin No.	Pin Name	Type	Description
133	SUA0	I	Command register selection address input pins
134	SUA1	I	
135	SUA2	I	
136	SUA3	I	
137	SUA4	I	
138	SUA5	I	
139	SUA6	I	
140	V _{DD}	P	
141	V _{SS}	P	
142	D0	B	Microcontroller data signal pins, with pull-up resistors
143	D1	B	
144	D2	B	
145	D3	B	
146	D4	B	
147	D5	B	
148	D6	B	
149	D7	B	
150	RESET	I	Reset pin
151	CS	I	Chip select signal from microcontroller
152	RD	I	Data read signal from microcontroller
153	WR	I	Data write signal from microcontroller
154	SWAIT	O	Wait signal to microcontroller
155	INT0	O	Interrupt request signals to microcontroller. Open drain outputs with built-in pull-up resistors.
156	INT1	O	
157	Reserve3	O	Reserved for future expansion (Must be left open if unused.)
158	Reserve4	O	
159	Reserve5	O	
160	V _{DD}	P	

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