	No. 5111	LC89970, 89970M
		PAL CCD Delay Line

## Overview

The LC89970 and LC89970M are CCD delay lines for PAL television systems. It incorporates a comb filter for chrominance signal and a 1 H delay line for luminance signal.

## Structure

- NMOS + CCD

## Functions

- Two CCD shift registers (for chrominance and luminance signals)
- CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- Sample-and-hold circuit
- PLL 3 × frequency multiplier
- fsc clock output circuit
- RD voltage generator

## Features

- 5 V single-voltage power supply
- Built-in PLL 3 × frequency multiplier circuit allows 3 fsc operation from an fsc (4.43 MHz) input.
- Control pin switchable to handle PAL/GBI and 4.43 MHz NTSC systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

## Specifications

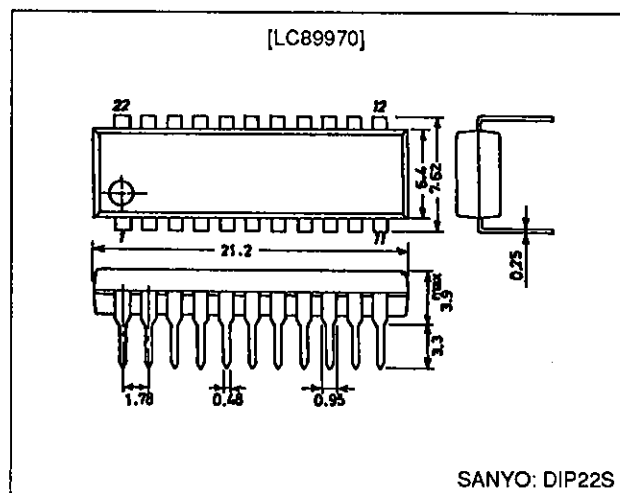
Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max		-0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89970	1200	mW
		LC89970M	600	mW
Operating temperature	T <sub>opr</sub>		-10 to +70	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

## Package Dimensions

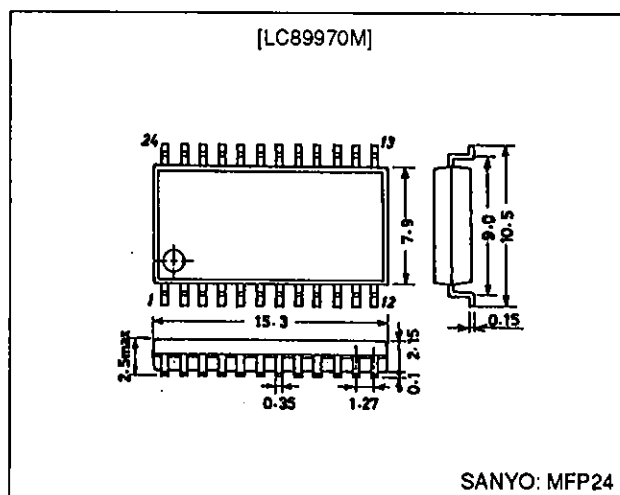
unit: mm

### 3059-DIP22S



unit: mm

### 3045B-MFP24



Allowable Operating Ranges at  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$		4.75	5.00	5.25	V
Clock input amplitude	$V_{CLK}$		300	500	1000	mVp-p
Clock frequency	$F_{CLK}$	Sine wave	—	4.43361875	—	MHz
Clock signal input amplitude	$V_{IN-C}$		—	350	500	mVp-p
Luminance signal input amplitude	$V_{IN-Y}$		—	400	572	mVp-p

Electrical Characteristics at  $V_{DD} = 5.0\text{ V}$ ,  $T_a = 25^\circ\text{C}$ ,  $F_{CLK} = 4.43361875\text{ MHz}$ ,  $V_{CLK} = 500\text{ mVp-p}$ 

Parameter	Symbol	Switch states			Conditions	min	typ	max	Unit
		SW1	SW2	SW3					
Supply current	I <sub>DD-1</sub>	a	a	b	1	40	50	60	mA
	I <sub>DD-2</sub>	b	a	b					
Chrominance System Characteristics (with no Y-IN input)									
Pin voltage (input)	V <sub>INC-1</sub>	a	a	b	2	2.0	2.4	2.8	V
	V <sub>INC-2</sub>	b	a	b					
Pin voltage (output)	V <sub>OUVC-1</sub>	a	a	b		1.2	1.6	2.0	V
	V <sub>OUTC-2</sub>	b	a	b					
Voltage gain	G <sub>VC-1</sub>	a	a	b	3	−2	0	+2	dB
	G <sub>VC-2</sub>	b	a	b					
Comb depth	C <sub>D-1</sub>	a	a	b	4	—	−40	−35	dB
	C <sub>D-2</sub>	b	a	b					
Linearity	L <sub>NC-1</sub>	a	a	b	5	−0.3	0.0	+0.3	dB
	L <sub>NC-2</sub>	b	a	b					
Clock leakage (3 fsc)	L <sub>CK3C-1</sub>	a	a	b	6	—	10	50	mVrms
	L <sub>CK3C-2</sub>	b	a	b					
Clock leakage (fsc)	L <sub>CK1C-1</sub>	a	a	b		—	0.8	1.5	mVrms
	L <sub>CK1C-2</sub>	b	a	b					
Noise	N <sub>C-1</sub>	a	a	b	7	—	0.5	2.0	mVrms
	N <sub>C-2</sub>	b	a	b					
Output impedance	Z <sub>OC-1</sub>	a	a	a, b	8	200	350	500	Ω
	Z <sub>OC-2</sub>	b	a	a, b					
OH delay time	T <sub>DC-1</sub>	a	a	b	9	—	245	—	ns
	T <sub>DC-2</sub>	b	a	b					

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Parameter	Symbol	Switch states			Conditions	min	typ	max	Unit
		SW1	SW2	SW3					
Luminance System Characteristics (with no C-IN1 or C-IN2 input)									
Pin voltage (input)	V <sub>INY-1</sub>	a	a	b	10	1.7	2.1	2.5	V
	V <sub>INY-2</sub>	b	a	b					
Pin voltage (output)	V <sub>OUTY-1</sub>	a	a	b		0.8	1.2	1.6	V
	V <sub>OUTY-2</sub>	b	a	b					
Voltage gain	G <sub>VY-1</sub>	a	a	b	11	−2	0	+2	dB
	G <sub>VY-2</sub>	b	a	b					
Frequency response	G <sub>FY-1</sub>	a	b	b	12	−2	0	+2	dB
	G <sub>FY-2</sub>	b	b	b					
Differential gain	D <sub>GY-1</sub>	a	a	b	13	0	5	7	%
	D <sub>GY-2</sub>	b	a	b					
Differential phase	D <sub>PY-1</sub>	a	a	b		0	5	7	deg
	D <sub>PY-2</sub>	b	a	b					
Linearity	L <sub>SY-1</sub>	a	a	b	14	37	40	43	%
	L <sub>SY-2</sub>	b	a	b					
Clock leakage (3 fsc)	L <sub>CK3Y-1</sub>	a	a	b	15	—	10	50	mVrms
	L <sub>CK3Y-2</sub>	b	a	b					
Clock leakage (fsc)	L <sub>CK1Y-1</sub>	a	a	b		—	0.8	1.5	mVrms
	L <sub>CK1Y-2</sub>	b	a	b					
Noise	N <sub>Y-1</sub>	a	a	b	16	—	0.5	2.0	mVrms
	N <sub>Y-2</sub>	b	a	b					
Output impedance	Z <sub>OY-1</sub>	a	a	c, b	17	250	400	550	Ω
	Z <sub>OY-2</sub>	b	a	c, b					
Delay time	T <sub>DY-1</sub>	a	a	b	18	—	63.92	—	μs
	T <sub>DY-2</sub>	b	a	b					

### Test Conditions

1. Supply current with no signal input.
2. C-OUT voltage (center bias voltage) with no signal input.
3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$GVC = 20 \log \frac{\text{C-OUT output [mVp-p]}}{350 \text{ [mVp-p]}} \text{ [dB]}$$

Test frequencies

GVC-1 4.429662 MHz (PAL/GBI)

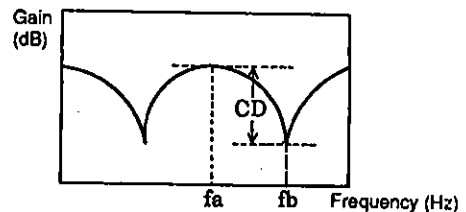
GVC-2 4.425694 MHz (4.43 NTSC)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

$$CD = 20 \log \frac{\text{C-OUT output with fb input [mVp-p]}}{\text{C-OUT output with fa input [mVp-p]}} \text{ [dB]}$$

Test frequencies

	fa	fb
CD-1	4.429662 MHz	4.425756 MHz (PAL/GBI)
CD-2	4.425694 MHz	4.417819 MHz (4.43 NTSC)



5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

$$\text{LNC} = 20 \log \left( \frac{\text{Output for a 500 mVp-p input [mVp-p]}}{500 \text{ [mVp-p]}} / \frac{\text{Output for a 200 mVp-p input [mVp-p]}}{200 \text{ [mVp-p]}} \right) \text{ [dB]}$$

Test frequencies

- LNC-1 4.429662 MHz (PAL/GBI)  
LNC-2 4.425694 MHz (4.43 NTSC)

6. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input.
7. Measure the noise in the C-OUT output with no input.  
Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.
8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$\text{ZOC} = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [}\Omega\text{]}$$

Test frequencies

- ZOC-1 4.429662 MHz (PAL/GBI)  
ZOC-2 4.425694 MHz (4.43 NTSC)

9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)
10. Y-OUT voltage (clamp voltage) with no signal input.
11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

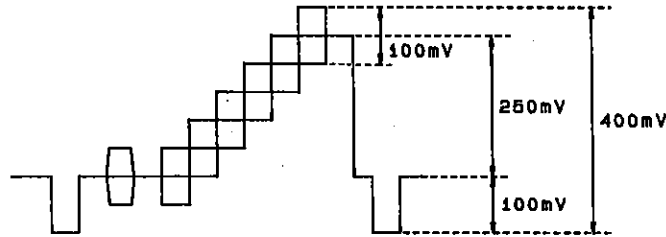
$$\text{GVY} = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{400 \text{ [mVp-p]}} \text{ [dB]}$$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

$$\text{GFY} = 20 \log \frac{\text{Y-OUT output with a 3.3 MHz input [mVp-p]}}{\text{Y-OUT output with a 200 kHz input [mVp-p]}} \text{ [dB]}$$

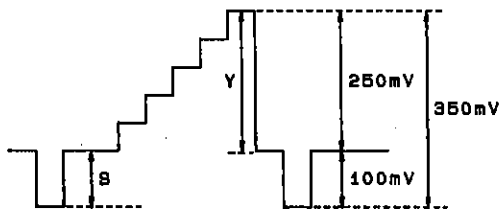
Note that  $V_{\text{bias}}$  should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



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14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



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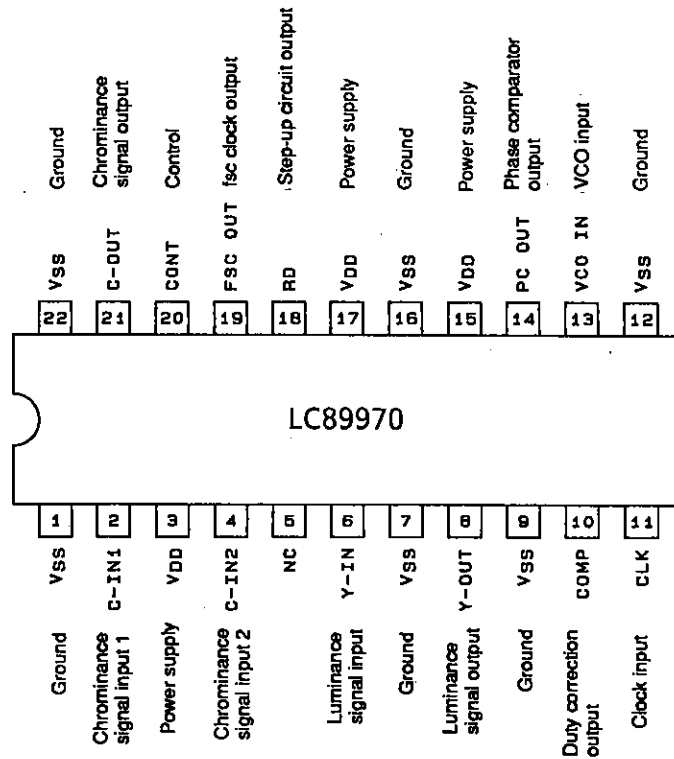
$$LS = \frac{S \text{ [mV]}}{Y \text{ [mV]}} \times 100 \text{ [%]}$$

15. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input.
16. Measure the noise in the Y-OUT output with no input.  
Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 5 MHz low-pass filter, and a 4.43 MHz trap filter.
17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW3 set to c, and let V2 be the C-OUT output with SW3 set to b.

$$ZOY = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [\Omega]}$$

18. The Y-OUT delay time with respect to Y-IN

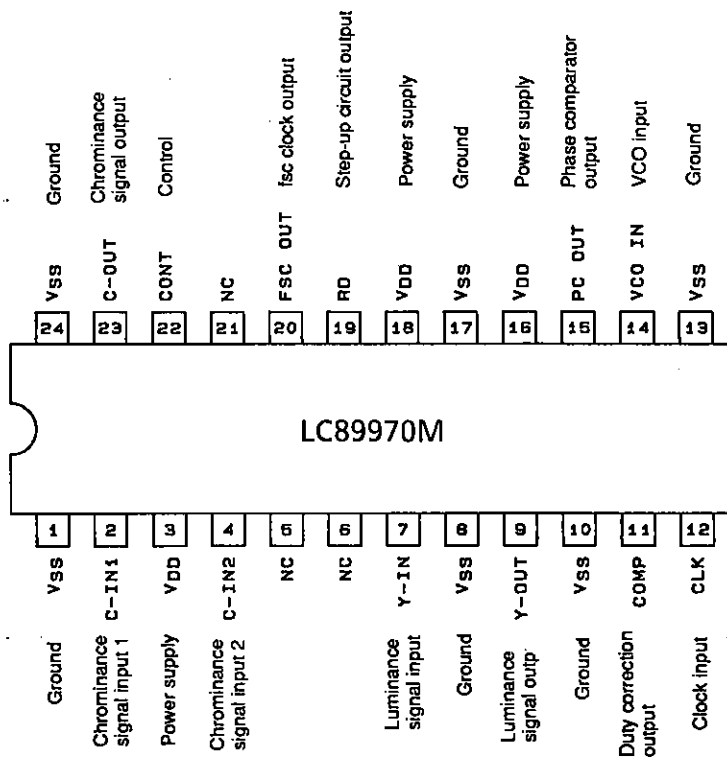
Pin Assignment [LC89970]



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Top view

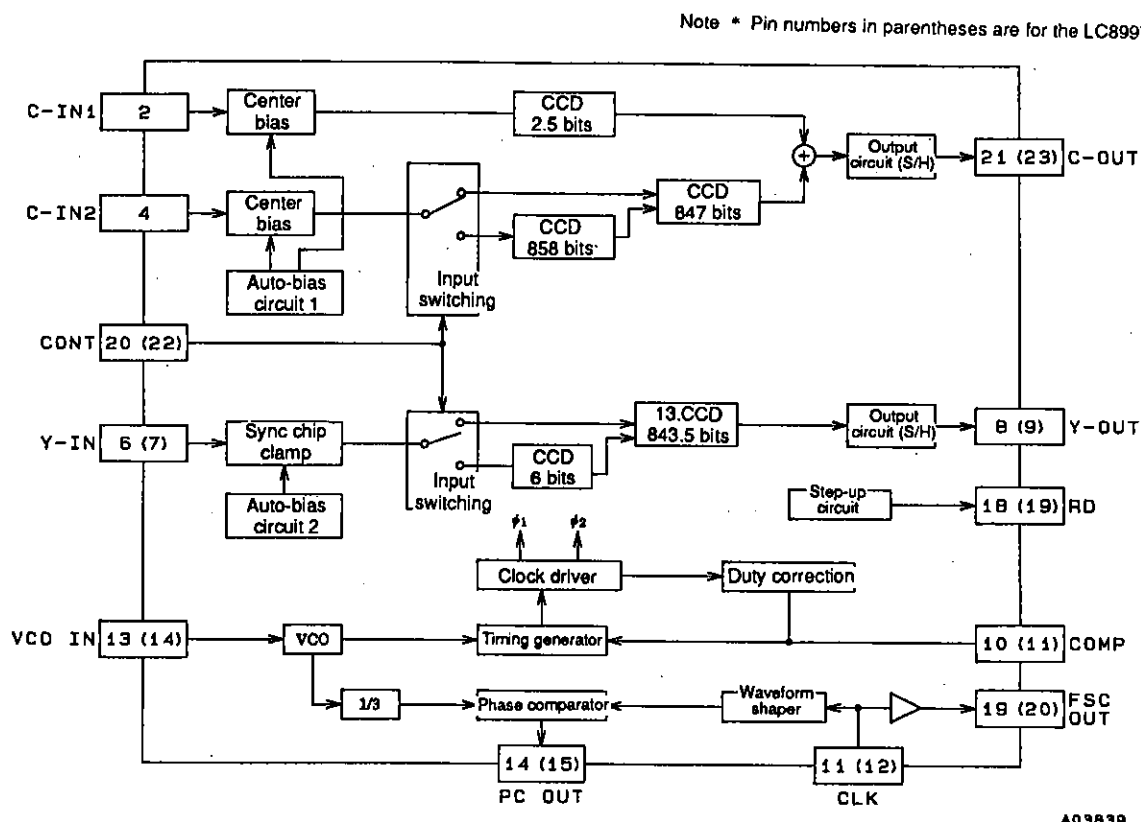
Pin Assignment [LC89970M]



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Top view

## Block Diagram



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## Control Pin Function

CONT	Mode (representative example)	Chrominance signal delay (CCD bits)	Luminance signal delay (CCD bits)
Low	PAL/GBI	2 H (1705) + 0 H (2.5)	1 H (849.5)
High	4.43 NTSC	1 H (847) + 0 H (2.5)	1 H (843.5)

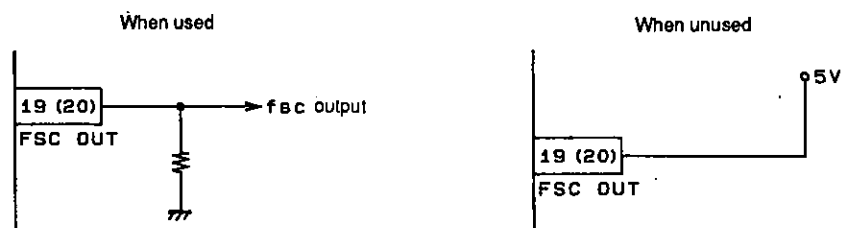
## Switching Voltage Levels

Low/high	Symbol	min	typ	max	Unit
Low	$V_L$	-0.3	0.0	0.5	V
High	$V_H$	2.0	5.0	6.0	V

Note: Since the control pin has a built-in pull-down resistor, the pin will be set to the low state if left open.

## FSC OUT Pin Function

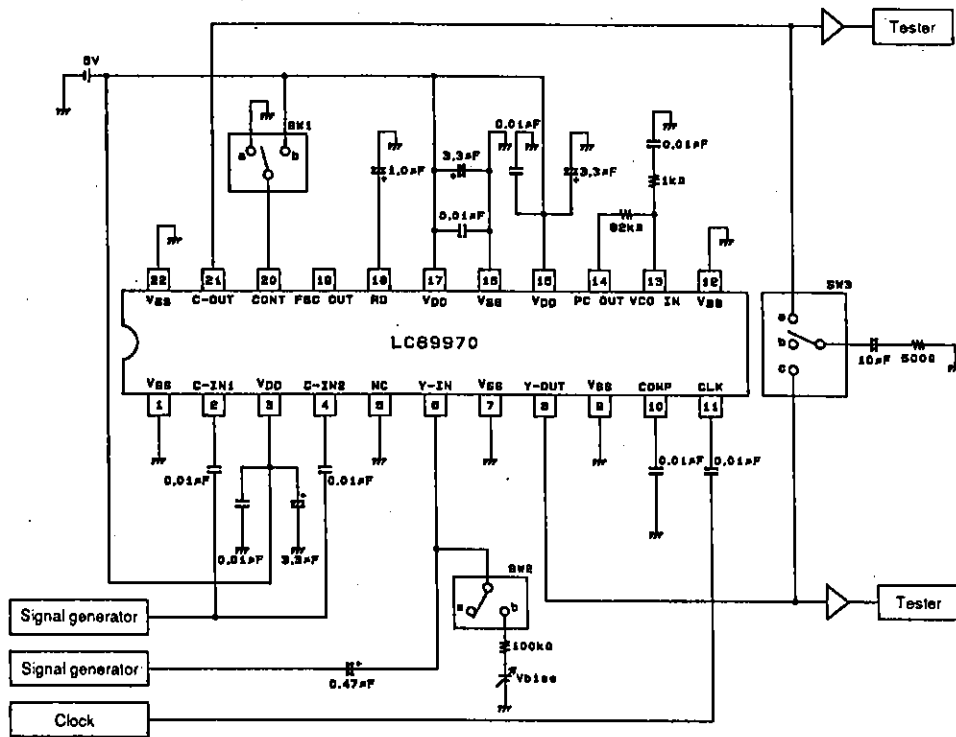
This pin provides a buffer output for the clock signal input to the CLK pin.



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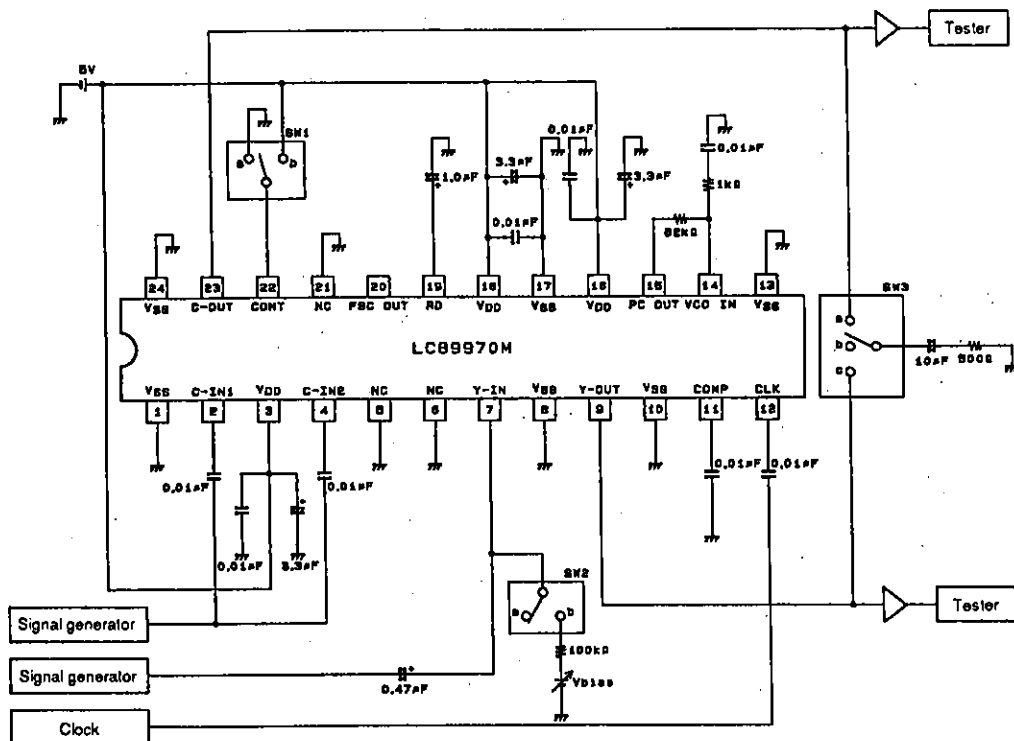
Note: Since this pin has a built-in pull-up resistor, the pin voltage will go to the supply voltage and output will cease if left open.

Test Circuit [LC89970]



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Test Circuit [LC89970M]



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