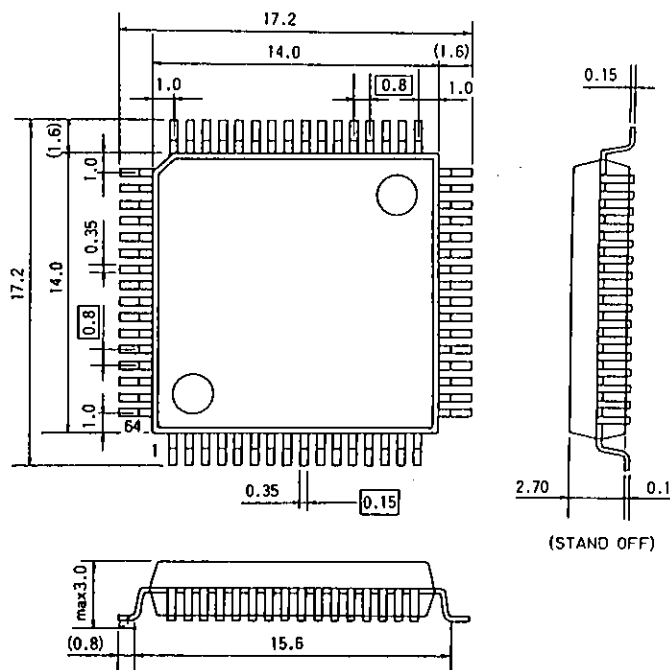


Timing Generator for Solid-State Imager

Features:

- Single +5V supply voltage
 - Low-power dissipation thanks to CMOS process technology
 - Output of all the pulses required for driving CCD Solid-State Imager and for signal processing
 - Two external synchronization functions: PLL synchronization using Horizontal SYNC. input, and Reset synchronization with V and H resets
 - Electronic automatic iris
- Automatic optical control is implemented based on the Sanyo original regulated stop-down technology. This shows excellent adaptability even in ultra-high bright environment thereby providing high-speed response. The magnification can be switched between 1/16 and 1/8. The shortest exposure is 1/15000 seconds.
- Center exposure/security optical control available
 - Long exposure of up to 4 times
- The automatic iris can be used even in the long exposure mode.

3150-Q64AVL



SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Absolute Maximum Ratings at $V_{SS} = 0V$

| Parameter | Symbol | Condition | Limits | Unit |
|---------------------------|---------------|------------------------------------|------------------------|------------|
| Maximum Supply Voltage | $V_{DD\ max}$ | $T_a = 25^\circ C$ | -0.3 to +7.0 | V |
| Input/Output Voltage | V_i, V_o | $T_a = 25^\circ C$ | -0.3 to $V_{DD} + 0.3$ | V |
| Maximum Power Dissipation | $P_d\ max$ | $T_a \leq 70^\circ C$ | 250 | mW |
| Operating Temperature | Topr | | -30 to +70 | $^\circ C$ |
| Storage Temperature | T_{stg} | | -55 to +125 | $^\circ C$ |
| Soldering Heat Resistance | | 10-sec. dip-soldering of pins only | 260 | $^\circ C$ |

Allowable operating Ratings at $T_a = -30^\circ C$ to $+70^\circ C$, $V_{SS} = 0V$

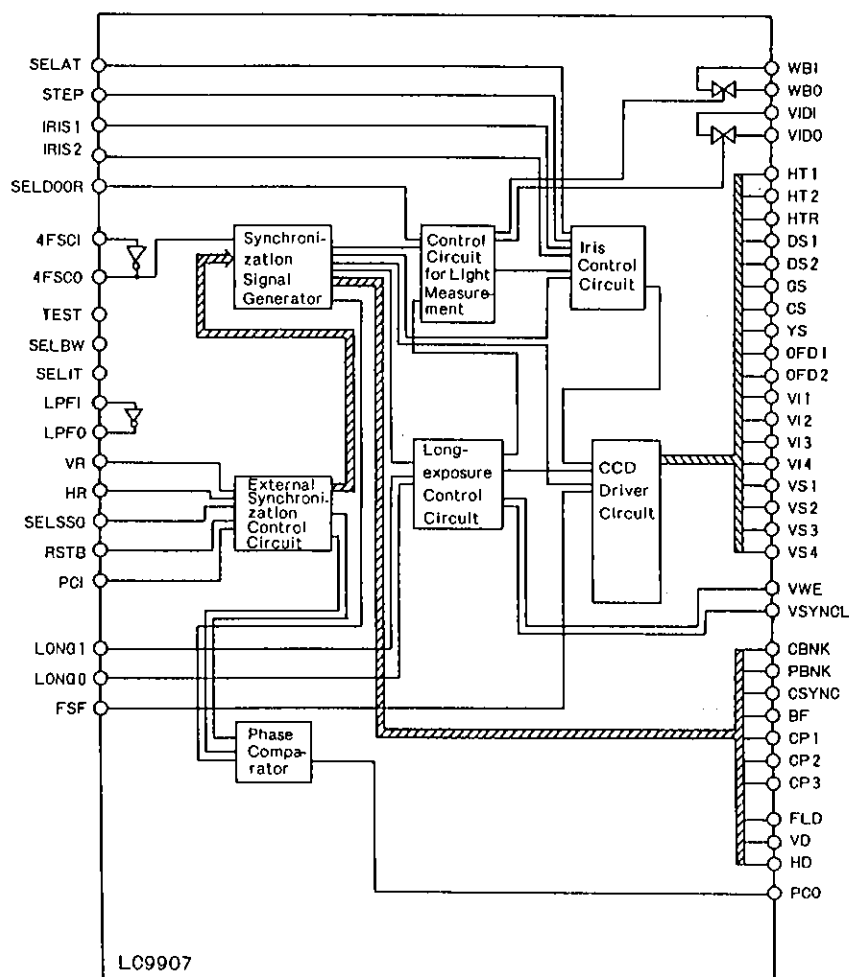
| Parameter | Symbol | min | typ | max | unit |
|---------------------|----------|-----|-----|----------|------|
| Supply Voltage | V_{DD} | 4.5 | 5.0 | 5.5 | V |
| Input Voltage Range | V_{IN} | 0 | | V_{DD} | V |

DC Characteristics at $V_{SS} = 0V$, $V_{pp} = 4.5V$ to $5.5V$, $T_a = -30^\circ C$ to $+70^\circ C$

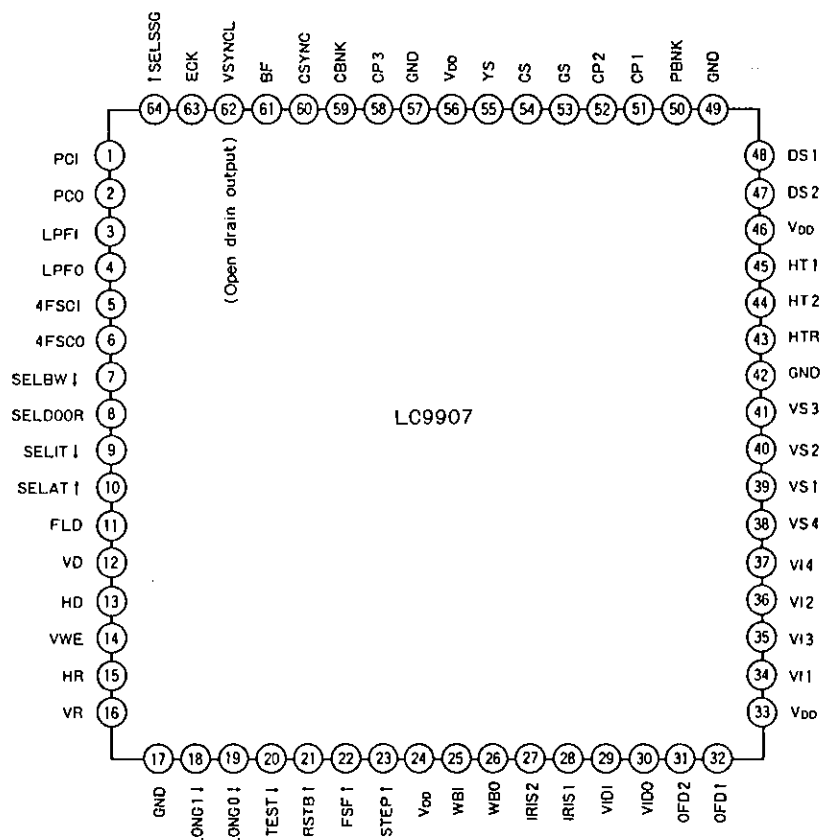
| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Applied Pins |
|--------------------------|----------|-------------------------------|-----------------|-----|-----------------|---------|--------------------------------|
| Input 'H'-level Voltage | V_{IH} | CMOS Level | $0.7V_{DD}$ | | | V | All input pins |
| Input 'L'-level Voltage | V_{IL} | CMOS Level | | | $0.3V_{DD}$ | V | All input pins |
| Output 'H'-level Voltage | V_{OH} | $I_{OH} = -3\ mA$ for TTL | 2.4 | | | V | All output pins except for (1) |
| Output 'L'-level Voltage | V_{OL} | $I_{OL} = 3\ mA$ for TTL | | | 0.4 | V | All output pins |
| Output 'H'-level Voltage | V_{OH} | $I_{OH} = -1\ \mu A$ for CMOS | $V_{DD} - 0.05$ | | | V | All output pins except for (1) |
| Output 'L'-level Voltage | V_{OL} | $I_{OL} = 1\ \mu A$ for CMOS | | | $V_{SS} + 0.05$ | V | All output pins |
| Output 'H'-level Voltage | V_{OH} | $I_{OH} = -30\ mA$ | | 2.5 | | V | PCO |
| Output 'L'-level Voltage | V_{OL} | $I_{OL} = 30\ mA$ | | 2.5 | | V | PCO |
| Input Leakage Current | I_L | $V_i = V_{SS}, V_{DD}$ | -1 | | +1 | μA | All output pins |
| Output Leakage Current | I_{OZ} | At the high impedance output | -10 | | +10 | μA | PCO VSYN CL ... (1) |

LC9907

Block Diagram



Pin Layout



↑ : Pull-up resistor output
↓ : Pull-down resistor output

LC9907

Pin Description

| Pin Number | Pin Name | I/O | Functional Description | | | | | | | | | | | | | | | |
|------------|----------------|--------------------------|--|-------|-------|--------------------------|---|---|------|---|---|------|---|---|------|---|---|------|
| 1 | PCI | I | Horizontal SYNC. input Synchronization signal input for PLL external synchronization | | | | | | | | | | | | | | | |
| 2 | PCO | O | Phase comparator Output of phase comparison of horizontal synchronization input with internal HSYNC. This is used for forming a horizontal PLL. | | | | | | | | | | | | | | | |
| 3 | LPFI | I | Inverter input for low-pass filter | | | | | | | | | | | | | | | |
| 4 | LPFO | O | Inverter output for low-pass filter | | | | | | | | | | | | | | | |
| 5 | 4FSCI | I | Inverter input for source oscillation : 14.318MHz | | | | | | | | | | | | | | | |
| 6 | 4FSCO | O | Inverter output for source oscillation | | | | | | | | | | | | | | | |
| 7 | SELBW | I | Color/monochrome switching pin NC or L: Color H: Monochrome (black and white) | | | | | | | | | | | | | | | |
| 8 | SELDOOR | I | Optical door select pin L: Full optical door/center optical door H: Security optical door | | | | | | | | | | | | | | | |
| 9 | SELIT | I | CCD interlace/non-interlace select 1. At 60Hz image pickup NC or L: Interlace H: Non-interlace (storage at $\phi 3$ and $\phi 4$) 2. Long-exposure is based on non-interlace image pickup with 3-picture element read-out (The storage gate is changed every 1/60 seconds). NC or L: Storage start at $\phi 1$ and $\phi 2$ H: Storage start at $\phi 3$ and $\phi 4$ | | | | | | | | | | | | | | | |
| 10 | SELAT | I | Automatic iris/manual iris switching L: Manual iris NC or H: Automatic iris | | | | | | | | | | | | | | | |
| 11 | FLD | O | Field identification signal | | | | | | | | | | | | | | | |
| 12 | VD | O | Vertical driver pulse | | | | | | | | | | | | | | | |
| 13 | HD | O | Horizontal drive pulse | | | | | | | | | | | | | | | |
| 14 | VWE | O | Vertical write enable | | | | | | | | | | | | | | | |
| 15 | HR | I | Horizontal reset pulse | | | | | | | | | | | | | | | |
| 16 | VR | I | Vertical reset pulse | | | | | | | | | | | | | | | |
| 18 19 | LONG1 LONG0 | I | Exposure cycle select pin <table><tr><td>LONG1</td><td>LONG0</td><td>Exposure cycle (seconds)</td></tr><tr><td>0</td><td>0</td><td>1/60</td></tr><tr><td>0</td><td>1</td><td>1/30</td></tr><tr><td>1</td><td>0</td><td>1/20</td></tr><tr><td>1</td><td>1</td><td>1/15</td></tr></table> | LONG1 | LONG0 | Exposure cycle (seconds) | 0 | 0 | 1/60 | 0 | 1 | 1/30 | 1 | 0 | 1/20 | 1 | 1 | 1/15 |
| LONG1 | LONG0 | Exposure cycle (seconds) | | | | | | | | | | | | | | | | |
| 0 | 0 | 1/60 | | | | | | | | | | | | | | | | |
| 0 | 1 | 1/30 | | | | | | | | | | | | | | | | |
| 1 | 0 | 1/20 | | | | | | | | | | | | | | | | |
| 1 | 1 | 1/15 | | | | | | | | | | | | | | | | |
| 20 | TEST | I | Test pin NC or L: Normal operation mode H: Test mode | | | | | | | | | | | | | | | |
| 21 | RSTB | I | Reset pin L: Internal initialization NC or L: No initialization | | | | | | | | | | | | | | | |
| 22 | FSF | I | Frame shift frequency select pin L: 3.58MHz NC or H: 1.79MHz | | | | | | | | | | | | | | | |
| 23 | STEP | I | Automatic iris magnification select pin L: 1/8 NC or H: 1/16 | | | | | | | | | | | | | | | |
| 25 | WBI | I | Analog switch for center-screen video signal isolation. Analog switch turns on during the output to the screen center location (1/4 size in area). | | | | | | | | | | | | | | | |
| 26 | WBO | O | | | | | | | | | | | | | | | | |

Continued on the next page.

Continued from the preceding page.

| Pin Number | Pin Name | I/O | Functional Description |
|----------------------|----------|--------------|---|
| 27 | IRIS2 | I | Optical data input pin for automatic Iris *: Refer to the optical method. |
| 28 | IRIS1 | I | |
| 29 | VIDI | I | Optical analog switch *: Refer to the optical method. |
| 30 | VIDO | O | |
| 31 | OFD2 | O | OFD pulse 2 OFD pulse for driving electronic shutter |
| 32 | OFD1 | O | OFD pulse 1 OFD pulse for frame shift |
| 34 | VI1 | O | Pulse for CCD ϕ 1 |
| 35 | VI3 | O | Pulse for CCD ϕ 3 |
| 36 | VI2 | O | Pulse for CCD ϕ 2 |
| 37 | VI4 | O | Pulse for CCD ϕ 4 |
| 38 | VS4 | O | Pulse for CCD ϕ S4 |
| 39 | VS1 | O | Pulse for CCD ϕ S1 |
| 40 | VS2 | O | Pulse for CCD ϕ S2 |
| 41 | VS3 | O | Pulse for CCD ϕ S3 |
| 43 | HTR | O | Pulse for CCD ϕ R |
| 44 | HT2 | O | Pulse for CCD ϕ H2 |
| 45 | HT1 | O | Pulse for CCD ϕ H1 |
| 47 | DS2 | O | Sampling precharge pulse |
| 48 | DS1 | O | Sampling data pulse |
| 50 | PBNK | O | Preblanking pulse |
| 51 | CP1 | O | Clamp pulse 1 |
| 52 | CP2 | O | Clamp pulse 2 |
| 53 | GS | O | Color sampling pulse Green |
| 54 | CS | O | Color sampling pulse Cyan |
| 55 | YS | O | Color sampling pulse Yellow |
| 58 | CP3 | O | Clamp pulse 3 |
| 59 | CBNK | O | Composite blanking pulse |
| 60 | CSYNC | O | Composite synchronization |
| 61 | BF | O | Burst flag |
| 62 | VSYNCL | O | Exposure cycle response type vertical synchronization pulse (open drain output) |
| 63 | ECK | O | Source oscillation output Connected with the 4FSC IN (pin 33) of the LA7266 |
| 64 | SELSSG | I | External synchronization mode select pin NC or L: internal synchronization, VR and HR reset synchronization H: PLL synchronization by horizontal synchronization signal input |
| 17 42 49 57 | GND | Power supply | Ground |
| 24 33 46 56 | VDD | Power supply | +5V |

External Synchronization

The LC9907 has two external synchronization modes: reset synchronization (H reset and V reset) and V reset-HPLL type synchronization.

1) Reset synchronization

The reset synchronization is based on the master clock synchronization of source oscillators. The reset circuit can be driven by setting the SELSSG to 'L'. The H reset circuit is controlled by pin 15 (HR) while the V reset circuit is controlled by pin 16 (VR). If a pin level changes from 'H' to 'L', the corresponding reset circuit will be activated. The H reset pulse will cause the HD to be set to 'L' and the V reset pulse will also cause the VD to be set to 'L'. If the V reset pulse changes from 'H' to 'L' with the HR = '0', the EVEN field will be selected. Otherwise, the ODD field will be selected.

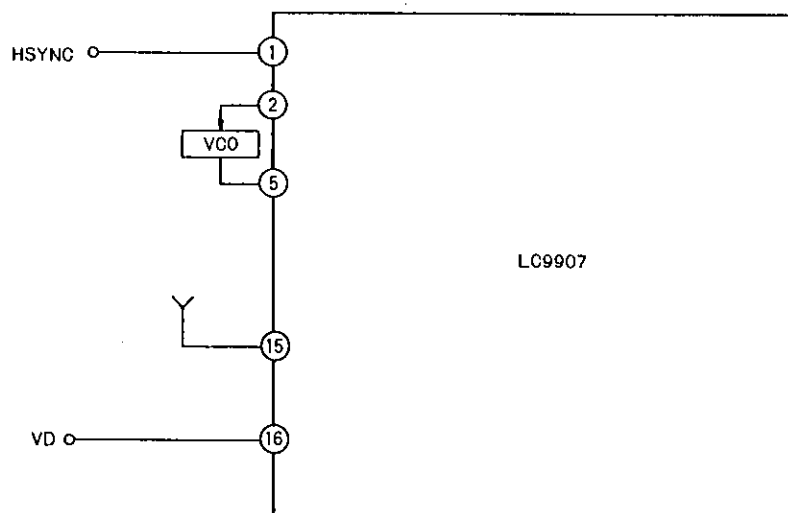
The reset synchronization timings are shown later in this catalog. The reset circuits are driven by the internal SYNC. generator if the HR and VR pin levels do not change to 'L'. This means that the LC9907 has the internal SYNC. generator which accepts outside interrupts.

2) External synchronization using HPLL and V reset

The LC9907 has an external synchronization that is implemented by HPLL and V reset. First, select the internal synchronization mode by setting the SELSSG to 'L' level or 'NC(not connected)' state.

Fix the HR pin at 'H' or 'L' level and then input vertical drive pulse VD (negative pulse) to the VR pin. The VCO can be configured by inputting HSYNC signals to the PCI (pin 1) and by using the PCO (pin 2) output.

The typical HPLL and V-reset external synchronization is shown below.



Long-time exposure

The LC9907 has a long-time exposure operation mode that can be selected by software. The maximum cycle of the long-time exposure is 15Hz that is followed by 20Hz, 30Hz and 60Hz (base cycle). Table 1 shows the relationship between software selection data and long-time exposure modes.

Table 1 Long-time exposure modes

| LONG1 | LONG0 | Exposure time (unit: seconds) |
|-------|-------|-------------------------------|
| 0 | 0 | 1/60 |
| 0 | 1 | 1/30 |
| 1 | 0 | 1/20 |
| 1 | 1 | 1/15 |

If a long-time exposure mode is selected and signals are processed normally, flickers may be produced on the screen. These flickers can be corrected by image storage area adjustment. However, if CCDs are interlaced like a normal exposure, the flickers moving up and down will be produced. As a result, if a long-time exposure mode is selected, the LC9907 automatically starts the non-interlace CCD drive that reads three pixels.

Even in the long-exposure mode, the automatic iris and manual iris functions are still effective. Note that the automatic iris response speed will be reduced according to exposure cycles.

In long-time exposure mode, the CCD sensitivity will be upgraded according to the exposure cycles. However, set temperature should be carefully handled because of the dark current increase.

Optical door modes

The optical control data for the automatic iris operation consists of two bits. As shown in Table 2, the three automatic iris operation modes can be selected by setting optical control data.

The optical control data is accepted on the rising edge of the pin 14 (VWE) input signal (near the tail of each field) to determine the iris point (electronic shutter position) of the next field.

The automatic iris function can be used by taking out the 2-bit data from video signal.

The operation mode that relates to optical area is discussed next.

The LC9907 has an internal analog switch that enables center screen isolation. This switch reduces the screen area into one fourth to give the highest priority to optical center door data.

Table 2 Optical control data and iris mode

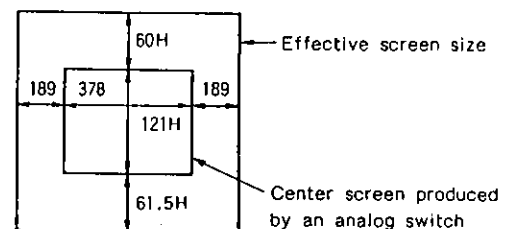
| IRIS1 | IRIS2 | Mode |
|-------|-------|-----------|
| 0 | 0 | Open |
| 0 | 1 | No change |
| 1 | 1 | Stop-down |

1) Center optical mode

There are two types of analog switch: WBI/WBO and VIDI/VIDO. The WBI/WBO switch is always available for center optical processing.

The VIDI/VIDO switch is used for this processing only if the SELDOOR is set to 'L'.

The center optical mode will be very effective for backlight adjustment in camera application systems where many of the subjects are located at the center screen.



2) Security optical mode

The camera locations in application systems such as door phones and monitor systems are fixed but the subjects do not always appear at the screen center. In such application systems, backlight is not fully adjusted in the center optical mode. To compensate for that drawback, the LC9907 provides fixed camera applications with security optical function.

If the SELDOOR pin is changed to 'H', analog switch pins 29 (VIDI), 30 (VIDO) and internal optical control data decision circuit are interrelated for joint operation. Optical control data is collected from the areas shown in the following four figures, evaluates each data ('0' = Open, '1' = Best, '2' = Stop-down), and adds all the area values. The decisions shown in Table 3 will be then made based on that sum and the number of areas with a value of '1' (best).

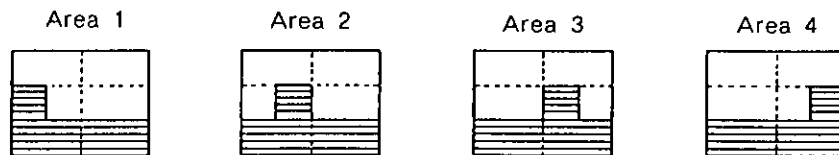


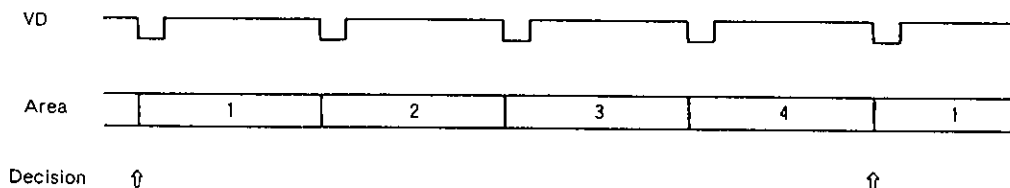
Table 3 Security optical mode decisions

| No. of 'best' areas | Evaluation total | | | ← Decisions |
|---------------------|------------------|-----------|-----------|-------------|
| | Open | No change | Stop-down | |
| 0 | 0, 2, 4 | — | 6, 8 | |
| 1 | 1, 3 | 5 | 7 | |
| 2 | 2 | 4, 6 | — | |
| 3 | — | 3, 5 | — | |
| 4 | — | 4 | — | |

According to the decision values shown in Table 3, at least one area out of the four areas has the optimum exposure. In short, the total evaluation value of the four areas is within the optimum exposure range.

Each area is selected in time sequence and its selection cycle is 4Vs.

This means that decisions are made every 4Vs. In short, decisions are made 15 times per seconds (at 60Hz image pickup).



If the camera locations in door phone systems are fixed so that low- brightness subjects appear at a bottom area (one fourth) of the screen, good backlight adjustment may be made.

Electronic auto iris

Electronic auto iris is to control exposure by the CCD electronic shutter (function to control image pickup time with the CCD drive).

The LC9907 allows the TTL type (through the lens) auto iris. The desired optical door mode can be selected from the Sanyo original two modes. For detailed information on the optical door modes, refer to the related item.

In this section, regulated stop-down mode will be discussed.

If a certain amount of photon is input to CCD, the CCD output is increased in proportion to shutter speed. The LC9907 provides the auto iris function using the field back loop. In the field back loop, the CCD output in proportion to a certain shutter speed is used to determine the shutter speed of the next field. The LC9907 auto iris function uses a optical control data (stop-down, no change, open), current shutter speed S (= exposure period) and stop-down rate A ($A = 1/8$ or $1/16$: selectable) to calculate shutter speed $S1$ of the next field as shown below.

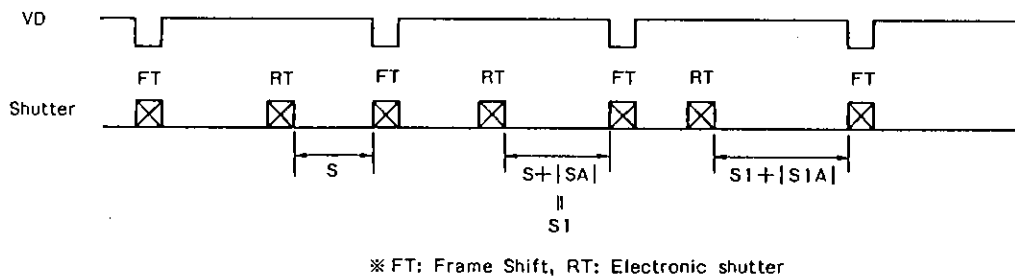
Stop-down : $S1 = S - |SA|$

No change : $S1 = S$

Open : $S1 = S + |SA|$

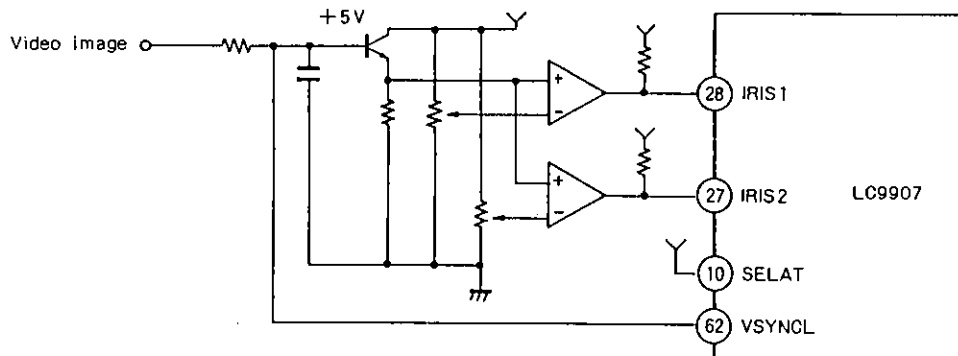
As a result, the change of the exposure time (stop-down rate) can be regulated.

- Iris open



The response in the center door mode at 60Hz image pickup will be about 0.8 seconds from 'release' (1/60 seconds) to the maximum stop-over (1/15000 seconds) (stop-down rate = 1/8) and about 1.3 seconds (stop-down rate = 1/16).

The auto iris function can be easily configured as shown below.



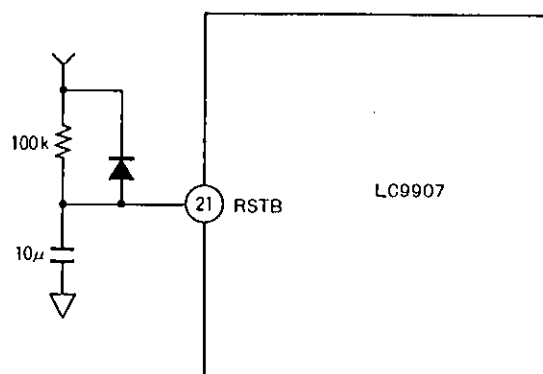
External add-on circuit

• Power-on reset circuit

The LC9907 requires a power-on reset circuit.

The circuit shown below can be configured with ease.

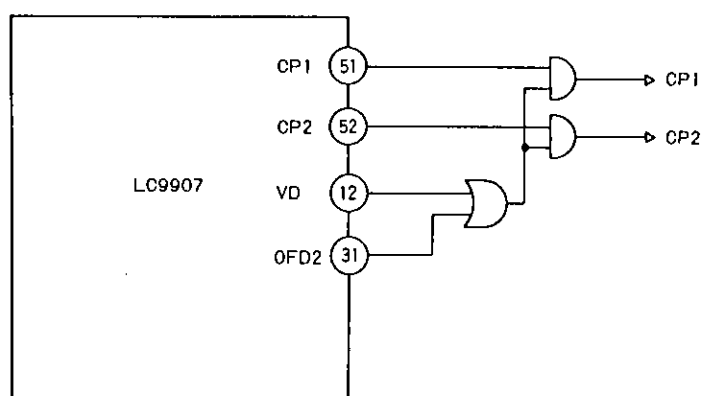
If the interface function with another control system such as camera control boards is needed, the reset pulse should be input to pin 21 (RSTB) after power is applied.



Unit (resistance: Ω , capacitance: F)

• Clamp pulse

The following circuit should be added to a user application product if the auto iris and the manual iris of up to 1/15000 seconds are used.



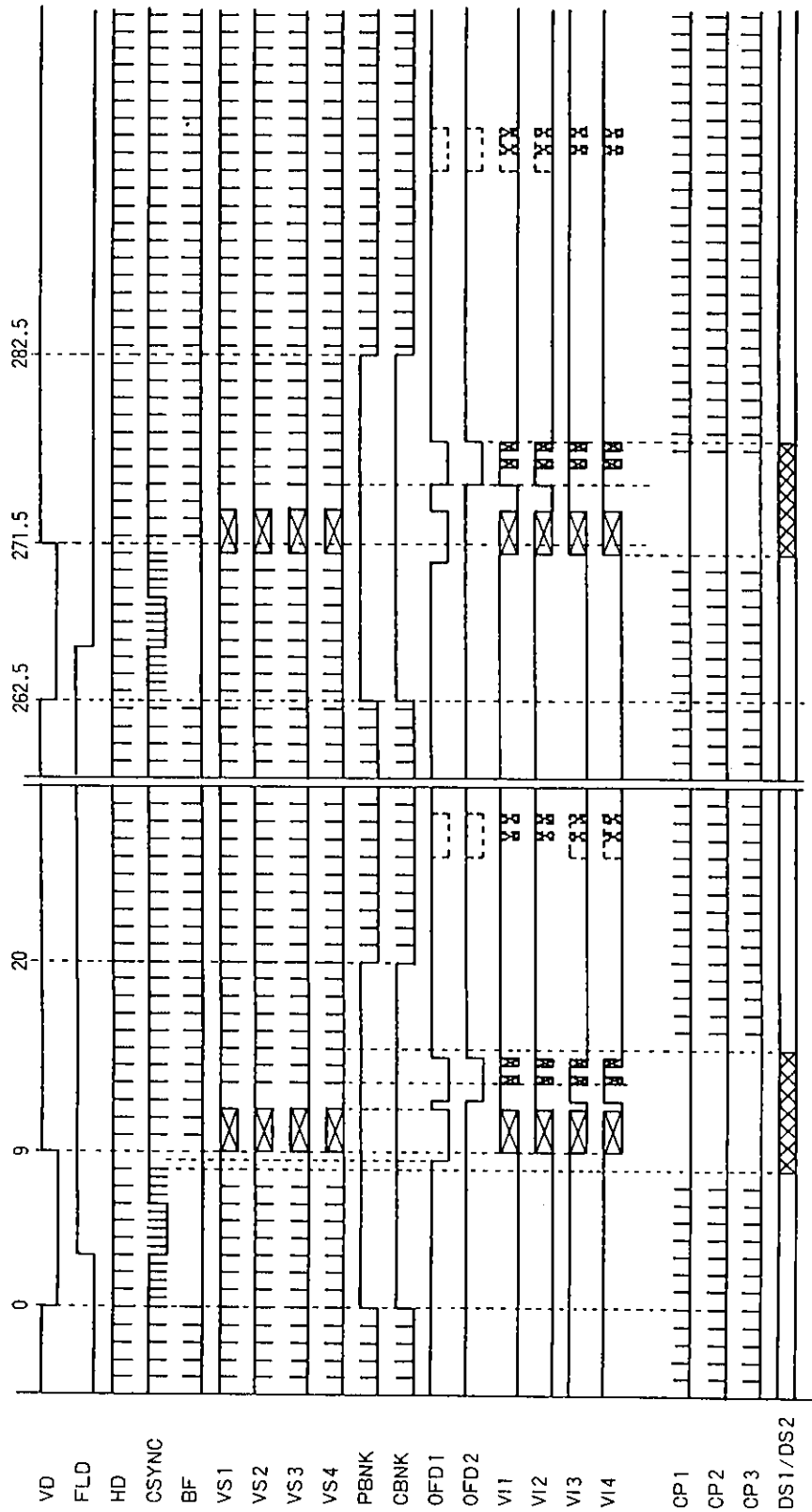
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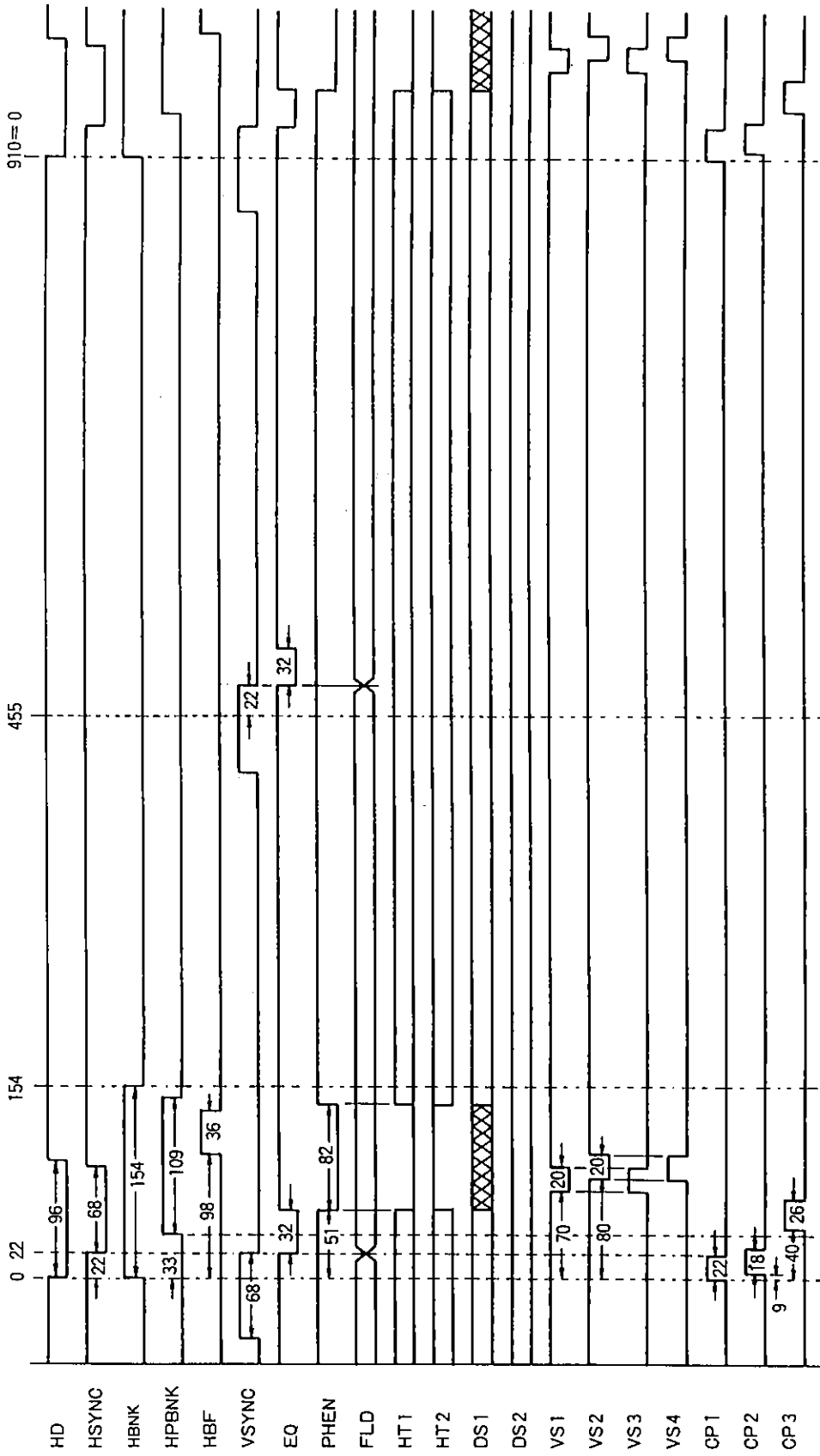
V-TIMING NTSC



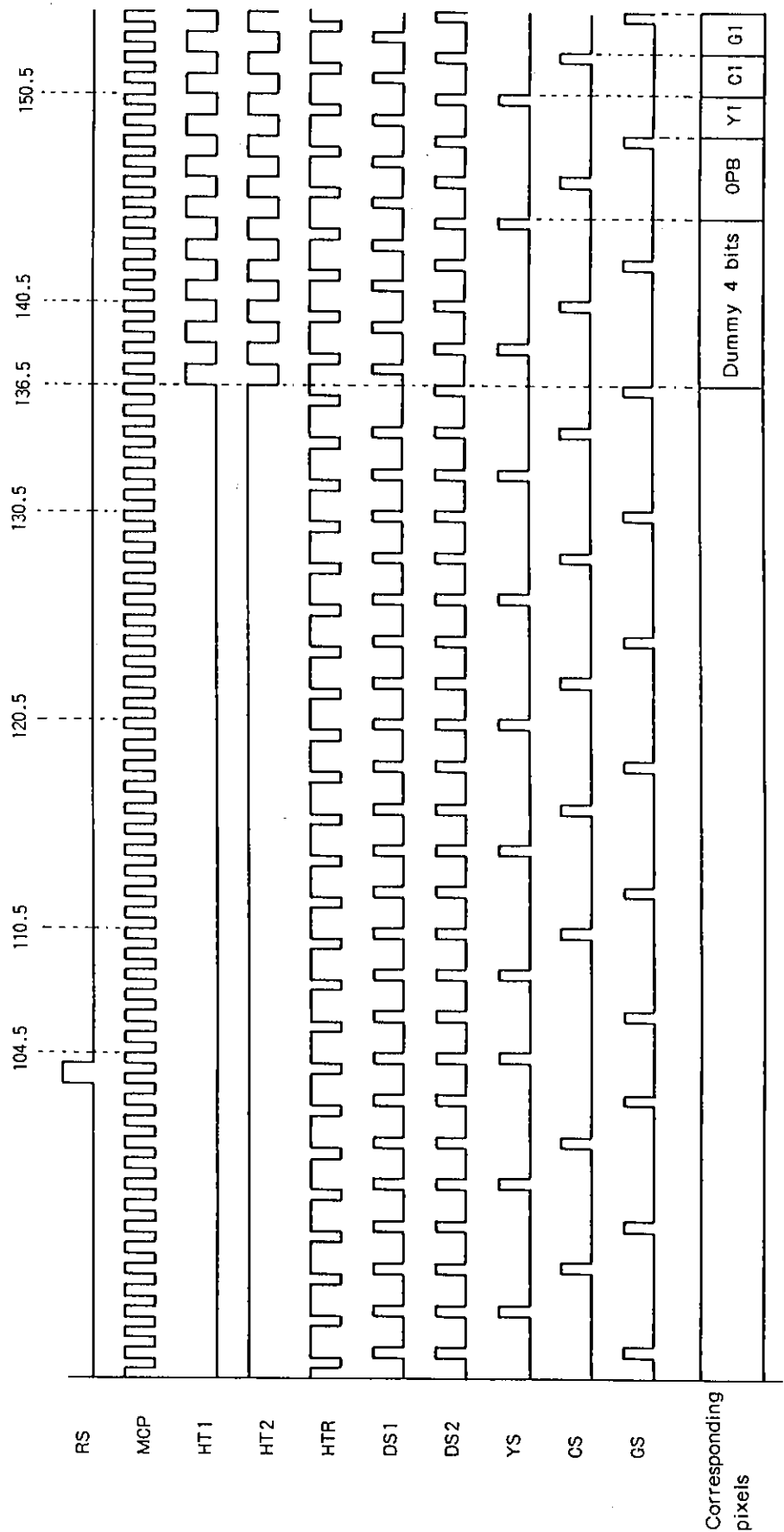
Notes

- The shaded DS1/DS2 means that the DS2 equals DS1.
- CBNK and PBNK will be inverted in the black-white mode.
- The frame shift frequency is 1.79MHz.
If the frame shift frequency is 3.58MHz, the number of pulses and the generation positions are the same as those in the 1.79MHz mode.
- For detailed information on frame shift and electronic shutter, refer to time chart VCCD.

H-TIMING

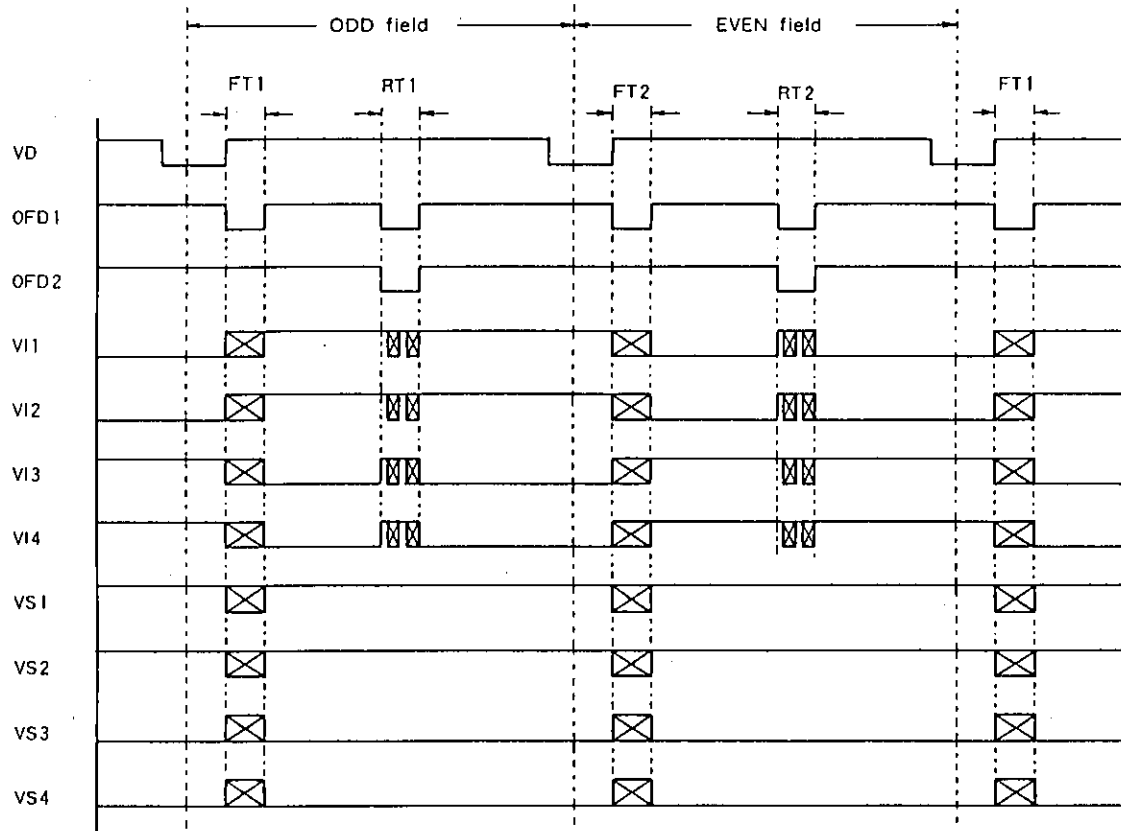


Sampling Timings



VCCD timings

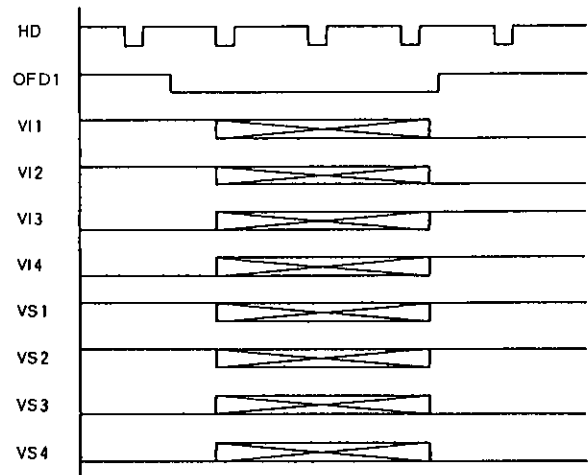
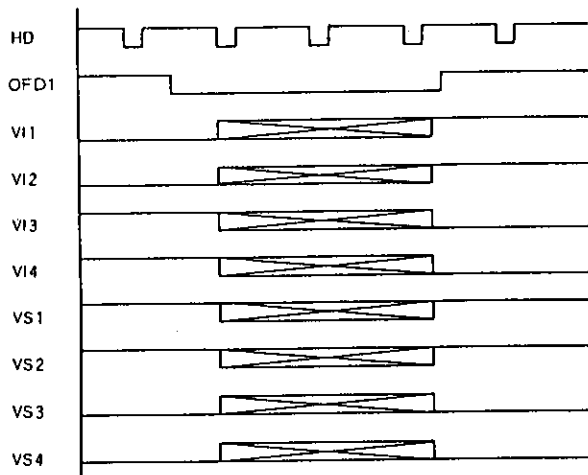
Frame shift and Electronic shutter



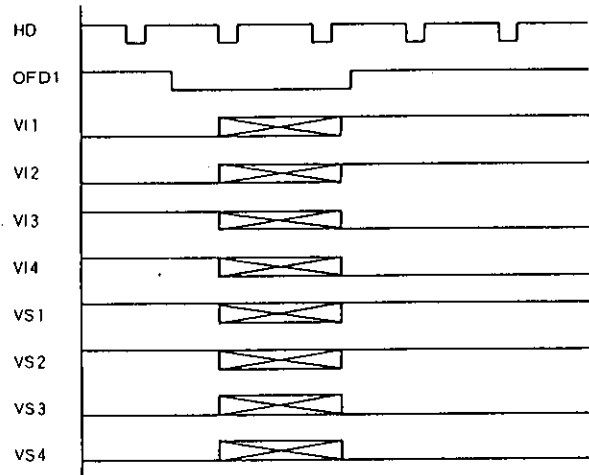
※FT: Frame shift period, RT: Discharge period

FT1 (ODD field frame shift)
FSF=1 (Frame shift frequency = 1.79MHz)

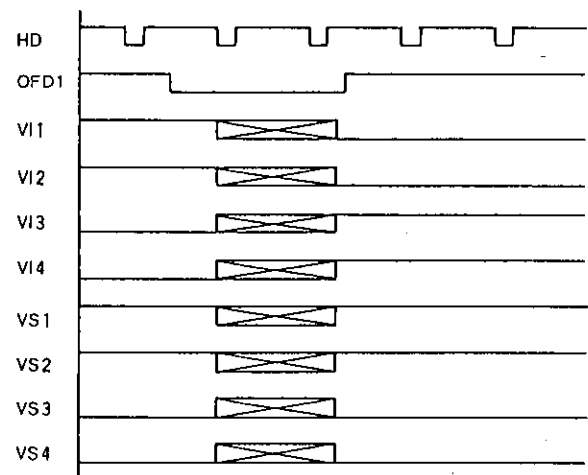
FT2 (EVEN field frame shift)
FSF=1 (Frame shift frequency = 1.79MHz)



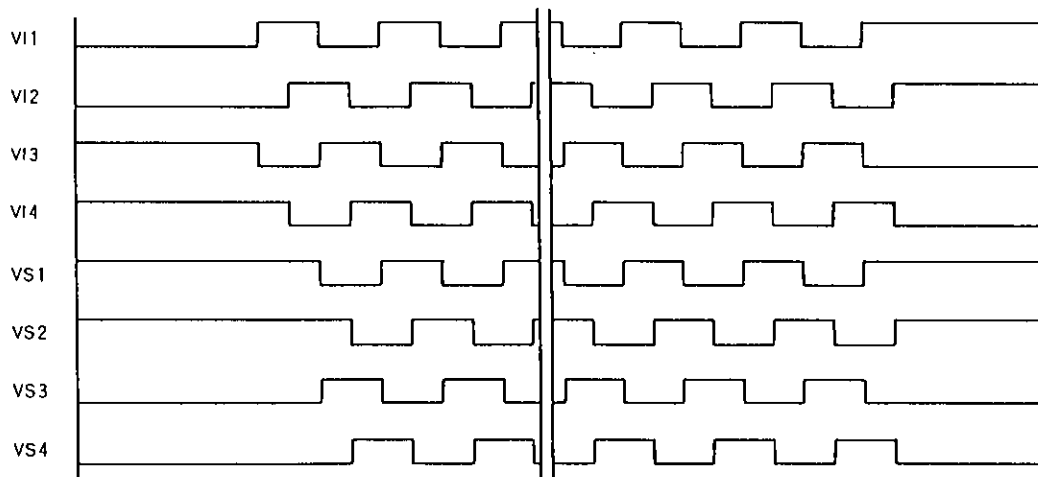
FT1 (ODD field frame shift)
FSF=0 (Frame shift frequency = 3.58MHz)



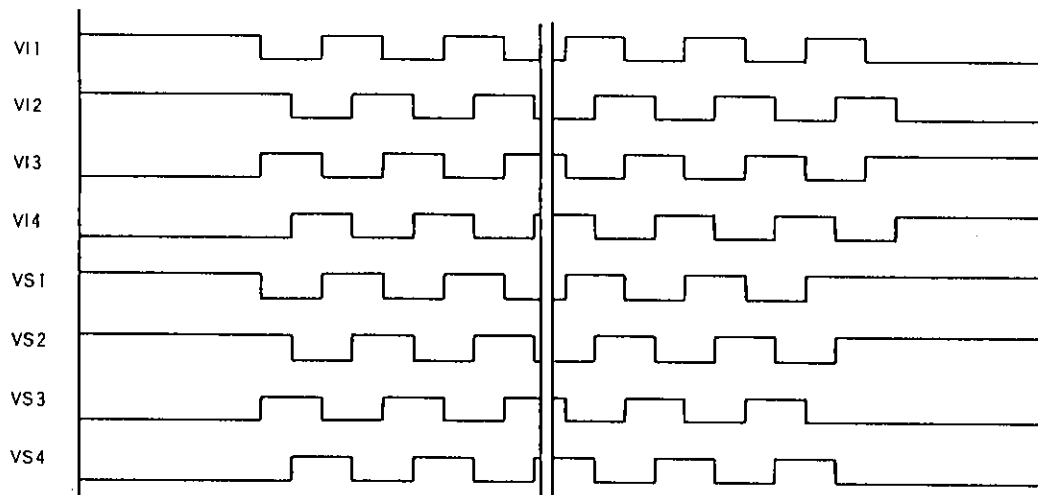
FT2 (EVEN field frame shift)
FSF=0 (Frame shift frequency = 3.58MHz)



FT1 (ODD field frame shift)

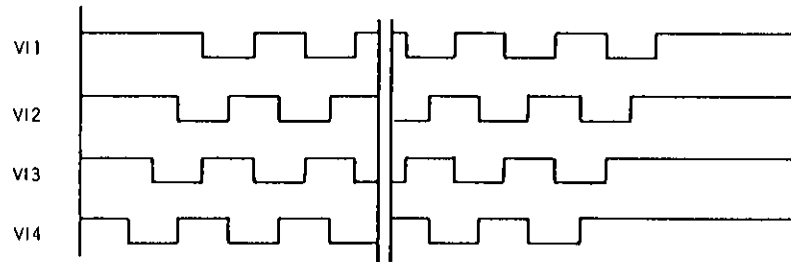


FT2 (EVEN field frame shift)

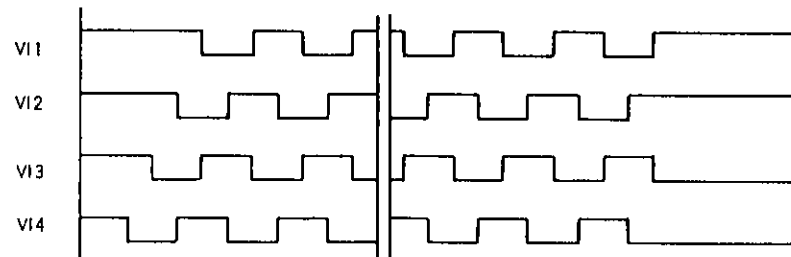


RT1 (ODD field discharge)

a. First transfer

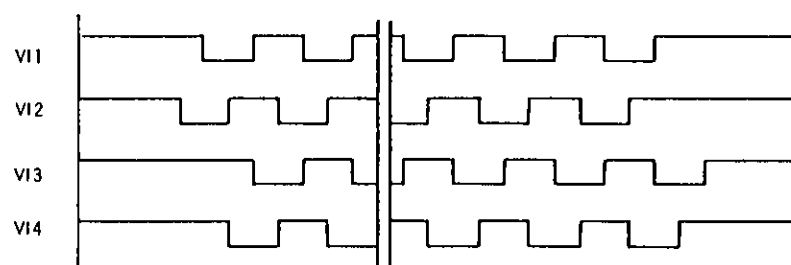


b. Second transfer

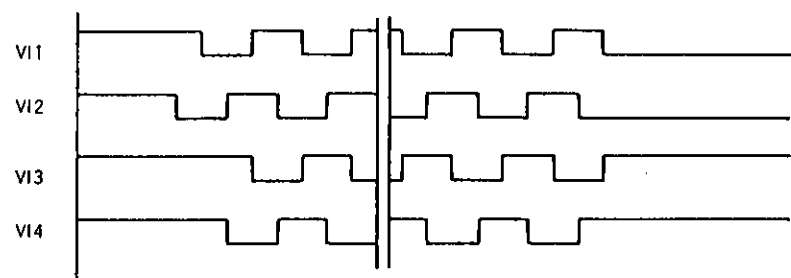


RT2 (EVEN field discharge)

a. First transfer



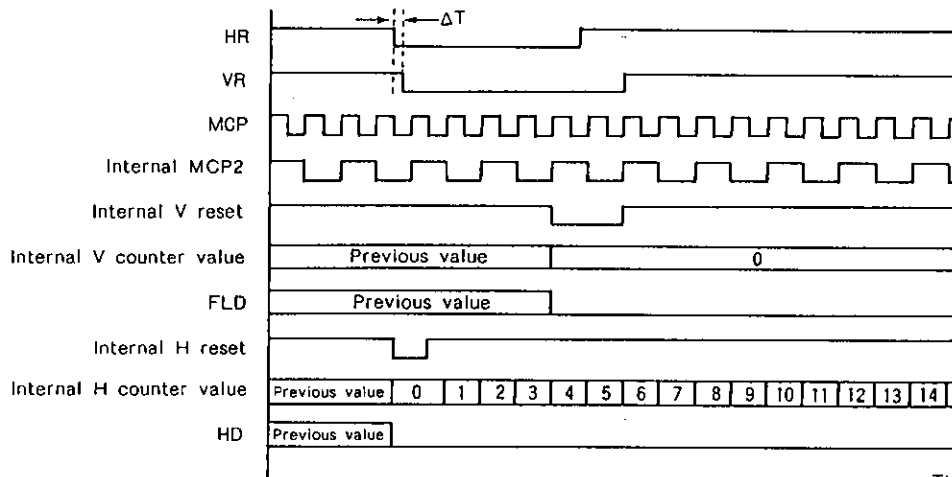
b. Second transfer



External synchronization

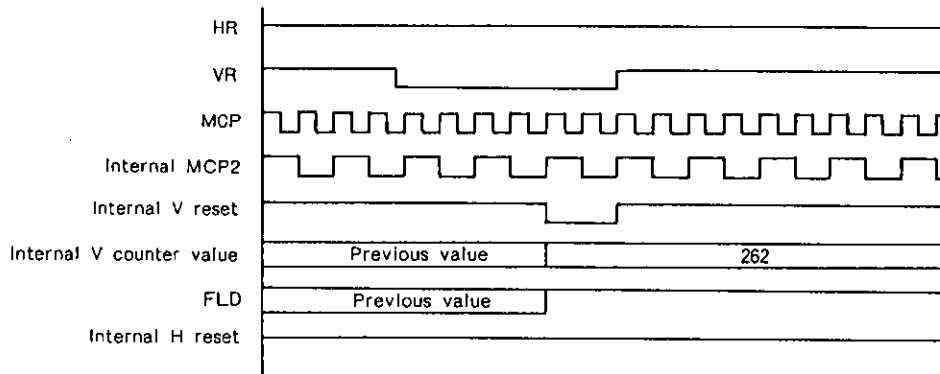
1. Reset synchronization

EVEN field

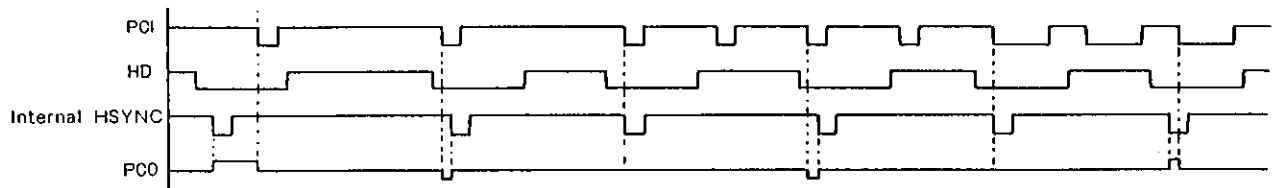


※ The delta T should be greater than 0 ns.

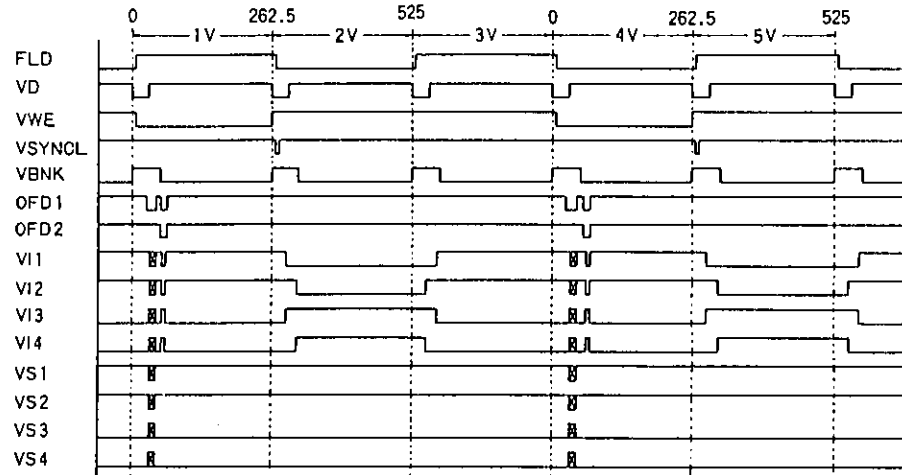
ODD field



2. H phase comparison



Long-time exposure timing (3-times exposure)



※ The VSYNCL is generated when the pull-up resistor is added to the open drain output circuit.