Ordering number : EN*5129A

CMOS LSI

LE28C1001M, T-90/12/15

1MEG (131072 words × 8 bits) Flash Memory

Preliminary

Overview

The LE28C1001M, T series ICs are 1 MEG flash memory products that feature a 131072-word × 8-bit organization and 5 V single-voltage power supply operation. CMOS peripheral circuits are adopted for high speed, low power dissipation, and ease of use. A 128-byte page rewrite function provides rapid data rewriting.

Features

- Highly reliable 2-layer polysilicon CMOS flash EEPROM process
- Read and write operations using a 5 V single-voltage power supply
- Fast access time: 90, 120, and 150 ns
- Low power dissipation
  - — Operating current (read): 30 mA (maximum)
  - — Standby current: 20 µA (maximum)
- Highly reliable read/write
  - — Erase/write cycles: $10^4/10^3$ cycles
  - — Data retention: 10 years
- Address and data latches
- Fast page rewrite operation
  - — 128 bytes per page
  - — Byte/page rewrite time: 5 ms (typical)
  - — Chip rewrite time: 5 s (typical)
- Automatic rewriting using internally generated Vpp
- Rewrite complete detection function
  - — Toggle bit
  - — $\overline{\text{Data}}$ polling
- Hardware and software data protection functions
- All inputs and outputs are TTL compatible.
- Pin assignment conforms to the JEDEC byte-wide EEPROM standard.
- Package

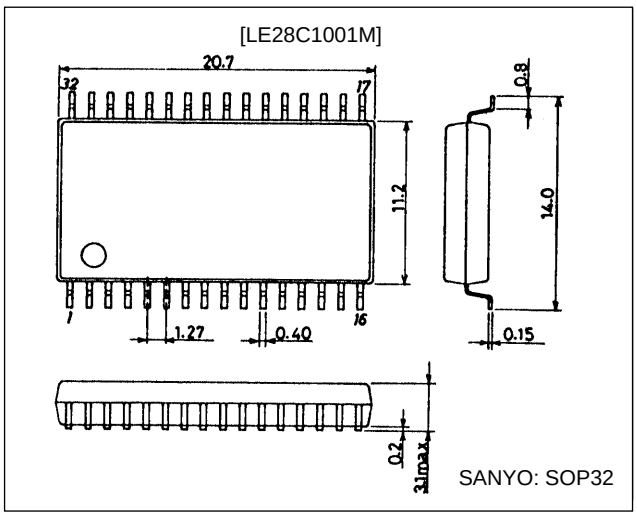
  SOP 32-pin (525 mil) plastic package : LE28C1001M

  TSOP 32-pin (8×20 mm) plastic package : LE28C1001T

Package Dimensions

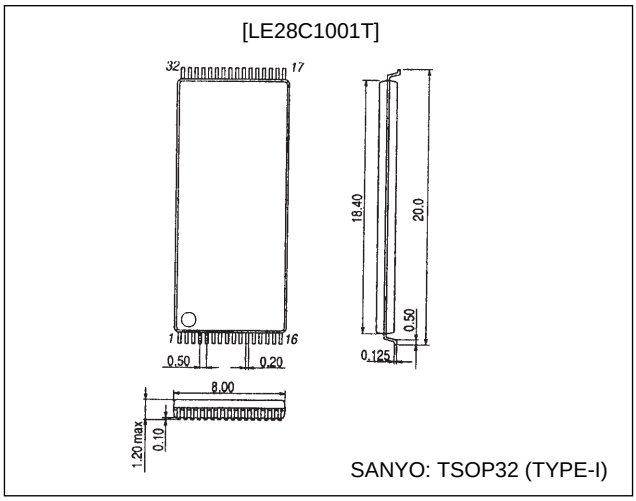
unit: mm

3205-SOP32



unit: mm

3224-TSOP32

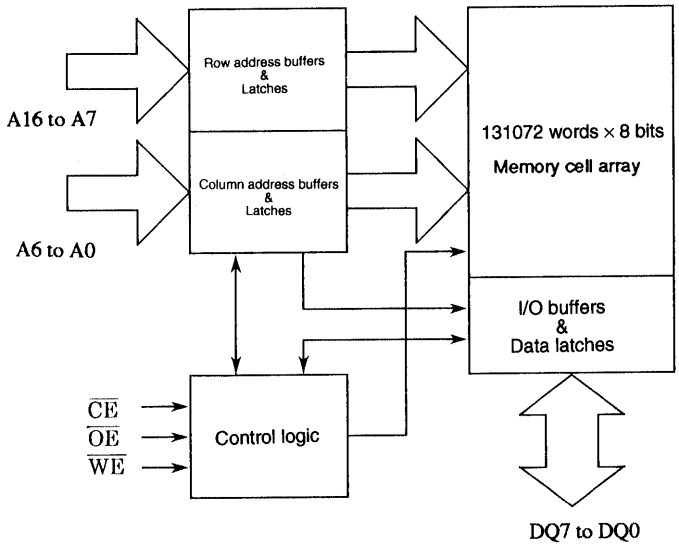


These FLASH MEMORY products incorporate technology licensed Silicon Storage Technology, Inc.

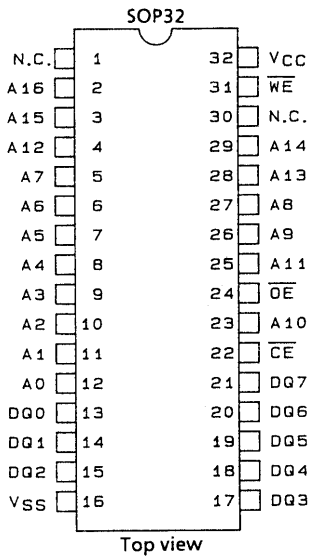
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

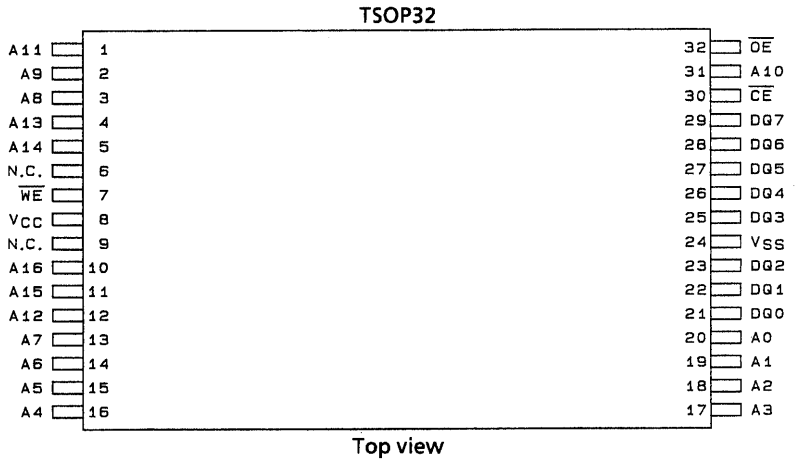
Block Diagram



Pin Assignments



A05759



A05760

Pin Functions

Symbol	Pin	Function
A16 to A0	Address input	Supply the memory address to these pins. The address is latched internally during a write cycle.
DQ7 to DQ0	Data input and output	These pins output data during a read cycle and input data during a write cycle. Data is latched internally during a write cycle. Outputs go to the high-impedance state when either $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip enable	The device is active when $\overline{CE}$ is low. When $\overline{CE}$ is high, the device becomes unselected and goes to the standby state.
$\overline{OE}$	Output enable	Makes the data output buffers active. $\overline{OE}$ is an active-low input.
$\overline{WE}$	Write enable	Makes the write operation active. $\overline{WE}$ is an active-low input.
V_{CC}	Power supply	Apply 5 V (±10%) to this pin.
V_{SS}	Ground	
N.C.	No connection	These pins must be left open.

Function Logic

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A16 to A0	DQ7 to DQ0
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Standby	V_{IH}	X	X	X	High-Z
Write inhibit	X	V_{IL}	X	X	High-Z/D_{OUT}
	X	X	V_{IH}	X	High-Z/D_{OUT}
Software chip erase (5 V, single voltage)	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Product identification	V_{IL}	V_{IL}	V_{IH}	A16 to A10 = V_{IL}, A8 to A1 = V_{IL}, A9 = 12 V, A0 = V_{IL}	Manufacturer code (BF)
				A16 to A10 = V_{IL}, A8 to A1 = V_{IL}, A9 = 12 V, A0 = V_{IH}	Device code (07)

Software Data Protection Command

Byte sequence	Set protection		Reset protection	
	Address	Data	Address	Data
Write 0	5555	AA	5555	AA
Write 1	2AAA	55	2AAA	55
Write 2	5555	A0	5555	80
Write 3			5555	AA
Write 4			2AAA	55
Write 5			5555	20

Note: Address format A14 to A0 (hex.)

Software Chip Erase Command (5 V single-voltage power supply)

Byte sequence	Address	Data
Write 0	5555	AA
Write 1	2AAA	55
Write 2	5555	80
Write 3	5555	AA
Write 4	2AAA	55
Write 5	5555	10

Note: Address format A14 to A0 (hex.)

Software Product ID Entry Command and Exit Command Codes

Byte sequence	Protect ID Entry		Protect ID Exit	
	Address	Data	Address	Data
Write 0	5555	AA	5555	AA
Write 1	2AAA	55	2AAA	55
Write 2	5555	80	5555	F0
Write 3	5555	AA		
Write 4	2AAA	55		
Write 5	5555	60		

Notes on software Product ID Command Code:
1. Command Code Address format: A14 to A0 (hex.)
2. With A14 to A1 = V_{IL},
   Manufacturer Code is read with A0 = V_{IL} to be BFH
   LE28C1001M, T series Device Code is read with A0 = V_{IH} to be 07H
3. The device does not remain in Software Product ID Mode if powered down.
4. A16 and A15 are V_{IH} or V_{IL}.

Device Operation

This Sanyo 1 MEG flash memory allows electrical rewrites using a 5 V single-voltage power supply. The LE28C1001M, T series products are pin and function compatible with the industry standards for this type of product.

Read

The LE28C1001M, T series read operations are controlled by $\overline{CE}$ and $\overline{OE}$. The host must set both pins to the low level to acquire the output data. $\overline{CE}$ is used for chip selection. When $\overline{CE}$ is at the high level, the chip will be in the unselected state and only draw the standby current. $\overline{OE}$ is used for output control. The output pins go to the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. See the timing waveforms (Figure 1) for details.

Page Write Operation

The write operation starts when both $\overline{CE}$ and $\overline{WE}$ are at the low level, and furthermore $\overline{OE}$ is at the high level. The write operation is executed in two stages. The first stage is a byte load cycle in which the host writes to the LE28C1001M, T series internal page buffers. The second stage is an internal programming cycle in which the data in the page buffer is written to the nonvolatile memory cell array. In the byte load cycle, the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The input data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. The internal programming cycle starts if either $\overline{WE}$ or $\overline{CE}$ remains high for 200 μs (t_{BLCO}). Once this programming cycle starts, the operation continues until the programming operation is completely done. This operation executes within 5 ms (typical). Figures 2 and 3 show the $\overline{WE}$ and $\overline{CE}$ control write cycle timing diagrams, and Figure 10 shows the flowchart for this operation.

In the page write operation, 128 bytes of data can be written to the LE28C1001M, T series internal page buffer before the internal programming cycle. All the data in the page buffer is written to the memory cell array during the 5 ms (typical) internal programming cycle. Therefore the LE28C1001M, T series page write function can rewrite all memory cells in 5 seconds (typical). The host can perform any other activities desired, such as moving data at other locations within the system and preparing the data required for the next page write, during the period prior to the completion of the internal programming cycle. In a given page write operation, all the data bytes loaded into the page buffers must be for the same page address specified by address lines A7 through A16. All data that was not explicitly loaded into the page buffer is set to FFH.

Figure 2 shows the page write cycle timing diagram. If the host loads the second data byte into the page buffer within the 100 μs byte load cycle time (t_{BLC}) after the first byte load cycle the LE28C1001M, T series stop in the page load cycle thus allowing data to be loaded continuously. The page load cycle terminates if additional data is not loaded into the internal page buffer within 200 μs (t_{BLCO}) after the previous byte load cycle, as in the case where $\overline{WE}$ does not switch from high to low after the last $\overline{WE}$ rising edge. The data in the page buffer can be rewritten in the next byte load cycle.

The page load period can continue indefinitely as long as the host continues to load data into the device within the 100 μs byte load cycle. The page that is loaded is determined by the page address of the last byte loaded.

Detecting the Write Operation State

The LE28C1001M, T series products provide two functions for detecting the completion of the write cycle. These functions are used to optimize the system write cycle time. These functions are based on detecting the states of the $\overline{Data}$ polling bit (DQ7) and the toggle bit (DQ6).

$\overline{Data}$ Polling (DQ7)

The LE28C1001M, T series products output to DQ7 the inverse of the last data loaded during the page and byte load cycles when the internal programming cycle is in progress. The last data loaded can be read from DQ7 when the internal programming cycle completes. Figure 4 shows the $\overline{Data}$ polling cycle timing diagram and Figure 11 shows the flowchart for this operation.

Toggle Bit (DQ6)

Data values of 0 and 1 are output alternately for DQ6, that is DQ6 is toggled between 0 and 1, during the internal programming cycle. When the internal programming cycle completes this toggling is stopped and the device becomes ready to execute the next operation. Figure 5 shows the toggle bit timing diagram and Figure 11 shows the flowchart for this operation.

Data Protection

Hardware Data Protection

Noise and glitch protection: The LE28C1001M, T series do not execute write operations for $\overline{WE}$ or $\overline{OE}$ pulses that are 15 ns or shorter.
Power (V_{CC}) on and cutoff detection: The programming operation is disabled when V_{CC} is 2.5 V or lower.
Write inhibit mode: Writing is disabled when $\overline{OE}$ is low and either $\overline{CE}$ is high or $\overline{WE}$ is high. Use this function to prevent writes from occurring when the power is being turned on or off.

Software Data Protection

The LE28C1001M, T series implement the optional software data protection function recognized by JEDEC. This function requires a 3-byte load operation to be performed before a write operation data load. The 3-byte load sequence starts a page load cycle without activating any write operation. Thus this is an optimal protection scheme for unintended write cycles triggered by noise associated with powering the chip on or off. Note that the LE28C1001M, T series are shipped with the software data protection function disabled.
The software data protection circuit is activated by executing a 3-byte byte load cycle in advance of the data sequence in the page load cycle. (See Figure 6.) This causes the device to automatically enter data protection mode. After this, write operations require a 3-byte byte load cycle to be executed in advance. A 6-byte write sequence is required to switch the device out of this protection mode. Figure 7 shows the timing diagram. If a write operation is attempted in software protection mode, all device functions are disabled for 200 μs. Figure 12 shows the flowchart for this operation.

Chip Erase

The LE28C1001M, T series provide a chip erase mode that erases all of the memory cell array and sets each bit to the 1 state. This mode can be effective when it is necessary to erase all data quickly.

5 V Single-Voltage Power Supply Software Chip Erase

The software chip erase mode operation is started by executing a specially defined 6-byte byte load sequence, similar to page mode operation under software protection. After the load cycle is executed, the device enters an internal programming cycle similar to the write cycle. Figure 8 shows the timing diagram and Figure 14 shows the flowchart for this operation.

Product Identification

The device identification code is used for recognizing the device and its manufacturer. This mode can be used by hardware and software. The hardware operating mode is used to recognize algorithms that match the device when an external programming unit is used. Also, user systems can recognize the product number using software product identification mode. Figure 13 shows the flowchart for this operation. The manufacturer and device codes are the same in both modes.

Specifications

Absolute Maximum Ratings at Ta 25°C

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{CC}	–0.5 to +6.0	V	1
Input pin voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V	1, 2
DQ pin voltage	V_{OUT}	–0.5 to V_{CC} + 0.5	V	1, 2
A9 pin voltage	V_{A9}	–0.5 to +14.0	V	1, 3
Allowable power dissipation	Pd max	600	mW	1, 4
Operating temperature	Topr	0 to +70	°C	1
Storage temperature	Tstg	–65 to +150	°C	1

Note: 1. The device may be destroyed by the application of stresses in excess of the absolute maximum ratings.
2. –1.0 V to V_{CC} + 1.0 V for pulses less than 20 ns
3. –1.0 V to +14 V for pulses less than 20 ns

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low-level voltage	V_{IL}			0.8	V
Input high-level voltage	V_{IH}	2.0			V

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain during read	I_{CCR}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all DQ pins open, address inputs = V_{IH} or V_{IL}, operating frequency = $1/t_{RC}$ (minimum), V_{CC} = V_{CC} max			30	mA
Current drain during write	I_{CCW}	$\overline{CE}$ = $\overline{WE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = V_{CC} max			50	mA
TTL standby current	I_{SB1}	$\overline{CE}$ = $\overline{OE}$ = $\overline{WE}$ =V_{IH},V_{CC} = V_{CC} max			3	mA
CMOS standby current	I_{SB2}	$\overline{CE}$ = $\overline{OE}$ = $\overline{WE}$ =V_{CC} – 0.3 V, V_{CC} = V_{CC} max			20	µA
Input leakage current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max			10	µA
Output leakage current	I_{LO}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max			10	µA
Output low-level voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = V_{CC} min			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –400 µA, V_{CC} = V_{CC} min	2.4			V

Input/output Capacitances at Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz

Parameter	Symbol	Conditions	max	Unit
Input/output capacitance	C_{DQ}	V_{DQ} = 0 V	12	pF
Input capacitance	C_{IN}	V_{IN} = 0 V	6	pF

Power on Timing

Parameter	Symbol	Conditions	max	Unit
Time from power on until first read operation	$t_{PU-READ}$		100	µs
Time from power on until first write operation	$t_{PU-WRITE}$		5	ms

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

AC Testing Conditions (See Figure 9)

Input rise and fall times: .....10 ns (max.)
Output load: .....1 TTL gate + 100 pF

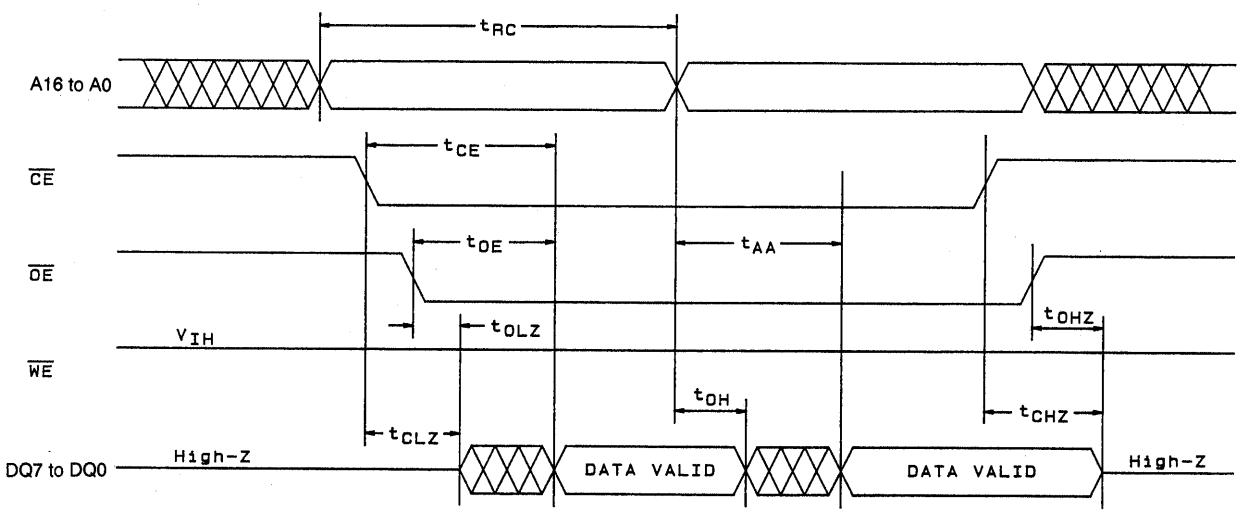
Read Cycle

Parameter	Symbol	LE28C1001M, T						Unit
		-90		-12		-15		
		min	max	min	max	min	max	
Read cycle time	t_{RC}	90		120		150		ns
$\overline{CE}$ access time	t_{CE}		90		120		150	ns
Address access time	t_{AA}		90		120		150	ns
$\overline{OE}$ access time	t_{OE}		50		60		70	ns
Output low-impedance time from $\overline{CE}$	t_{CLZ}	0		0		0		ns
Output low-impedance time from $\overline{OE}$	t_{OLZ}	0		0		0		ns
Output high-impedance time from $\overline{CE}$	t_{CHZ}		40		40		40	ns
Output high-impedance time from $\overline{OE}$	t_{OHZ}		40		40		40	ns
Output valid time from address input	t_{OH}	0		0		0		ns

Page Write Cycle

Parameter	Symbol	min	typ*	max	Unit
Write cycle time (erase and program)	t_{WC}		5	10	ms
Address setup time	t_{AS}	0			ns
Address hold time	t_{AH}	50			ns
$\overline{CE}$ setup time	t_{CS}	0			ns
$\overline{CE}$ hold time	t_{CH}	0			ns
$\overline{OE}$ setup time	t_{OES}	0			ns
$\overline{OE}$ hold time	t_{OEH}	0			ns
$\overline{CE}$ pulse width	t_{CP}	70			ns
$\overline{WE}$ pulse width	t_{WP}	70			ns
Data setup time	t_{DS}	45			ns
Data hold time	t_{DH}	0			ns
Byte load cycle time	t_{BLC}	0.05		100	µs
Byte load timeout time	t_{BLCO}	200			µs

Note: * typ is a reference value at V_{CC} = 5.0, Ta = 25 °C.



A05761

Figure 1 Read Cycle

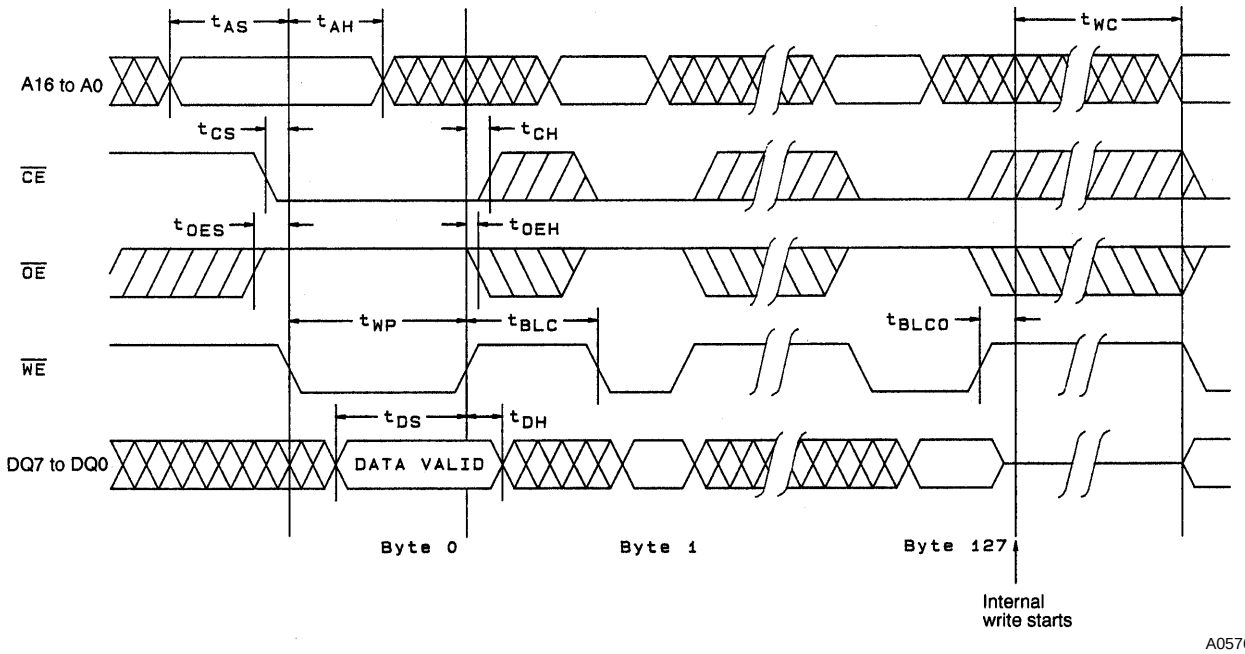


Figure 2 $\overline{WE}$ Control Page Write Cycle

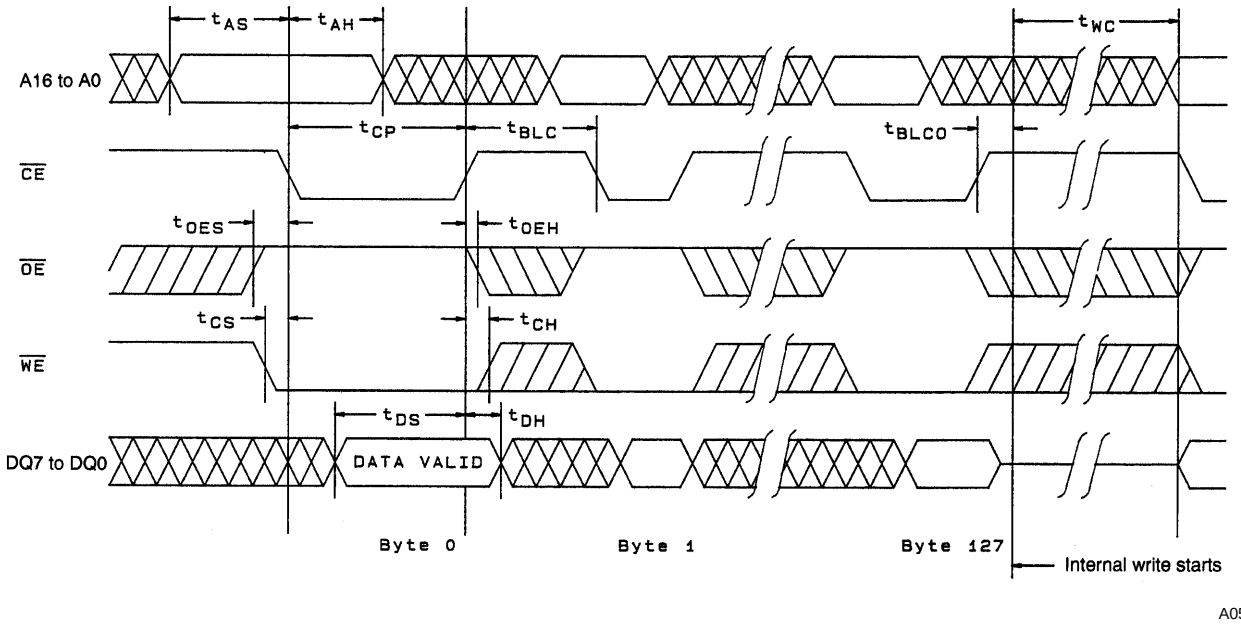


Figure 3 $\overline{CE}$ Control Page Write Cycle

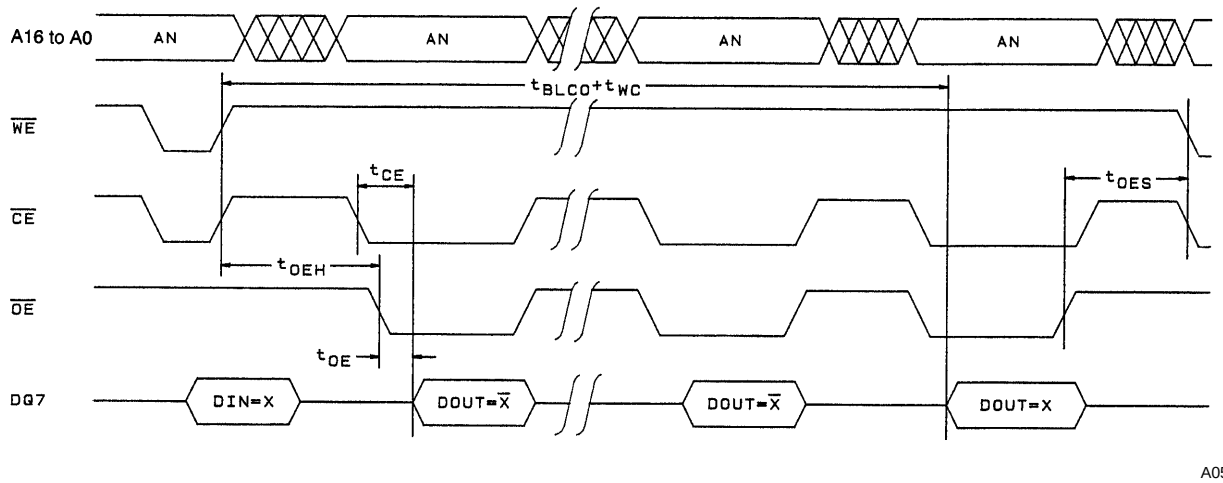


Figure 4 $\overline{\text{Data}}$ Polling

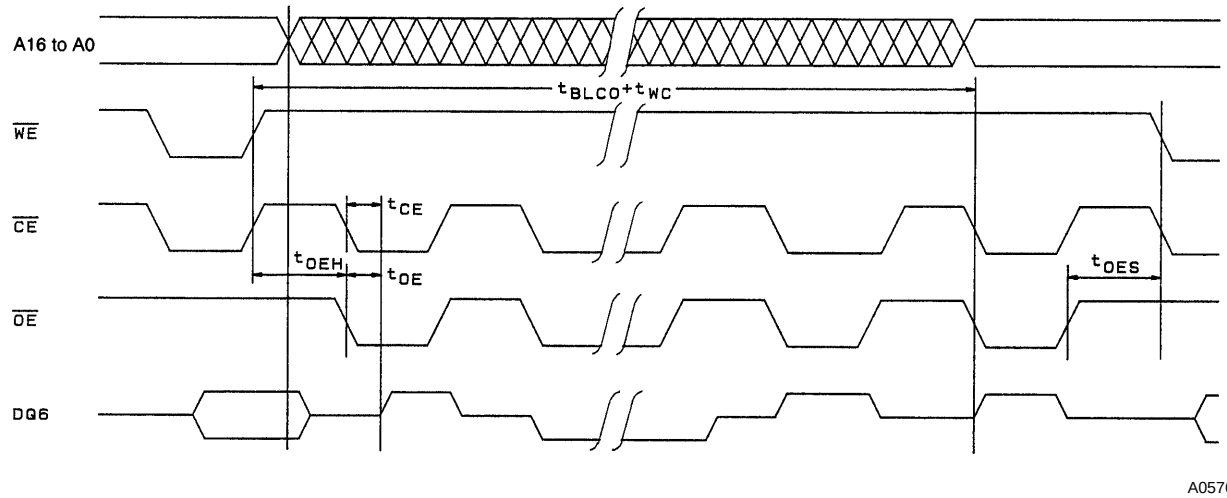


Figure 5 Toggle Bit

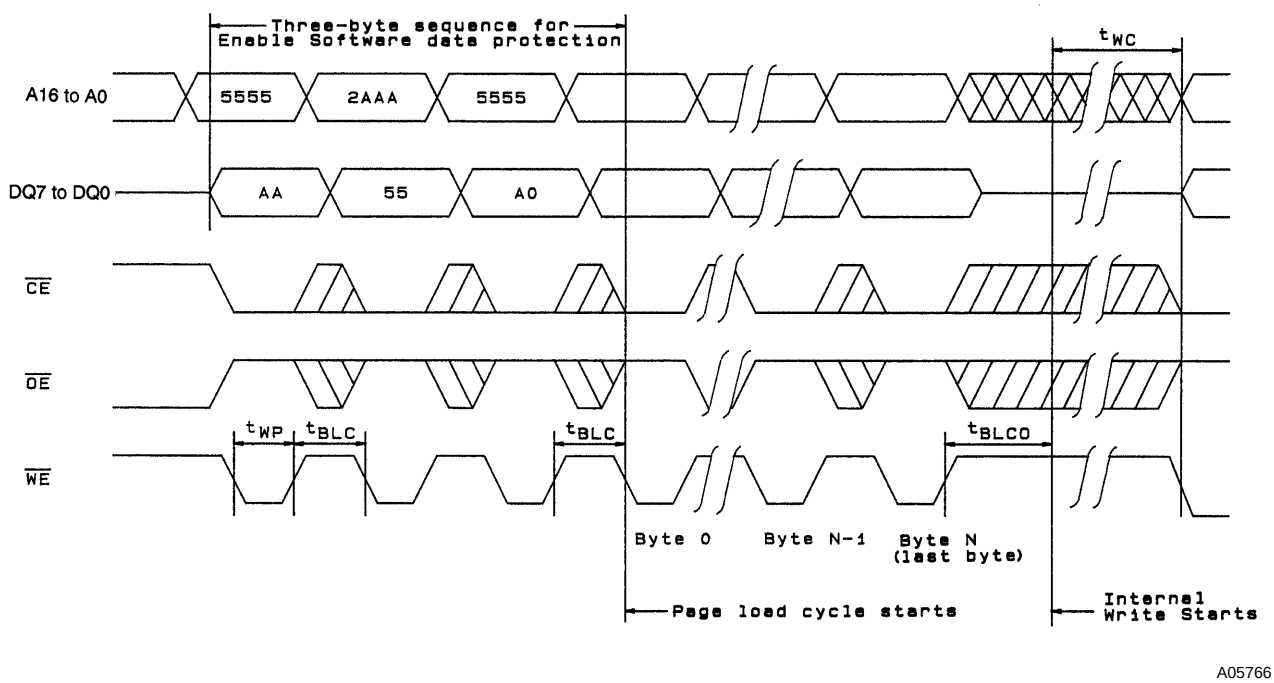


Figure 6 Enable Software Data Protection

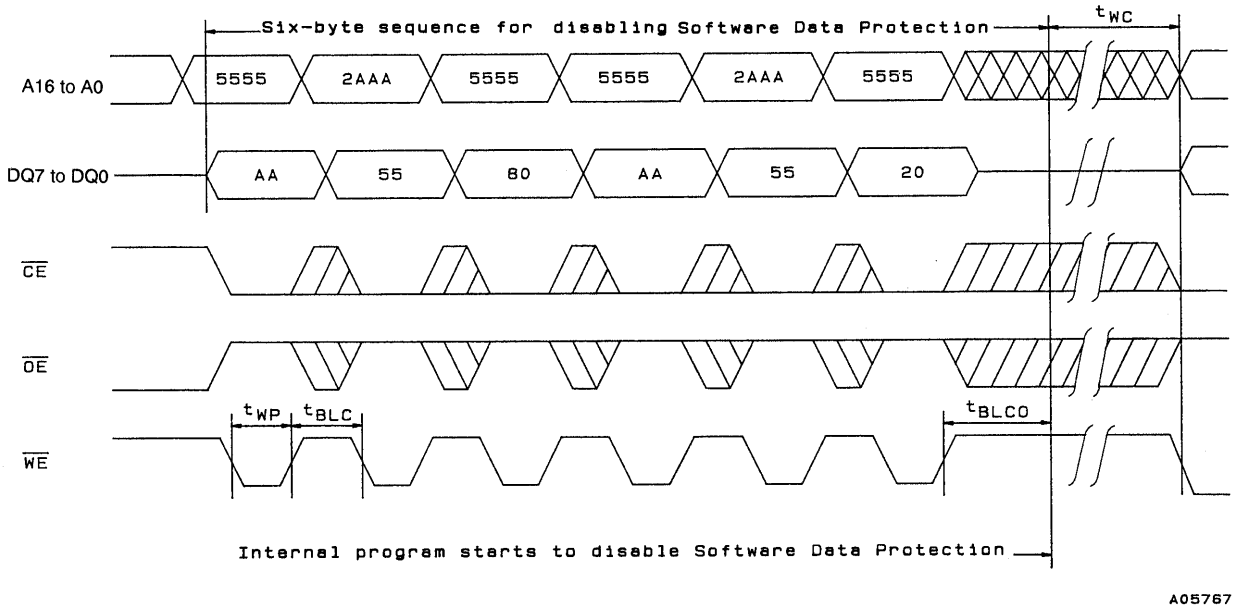


Figure 7 Disable Software Data Protection

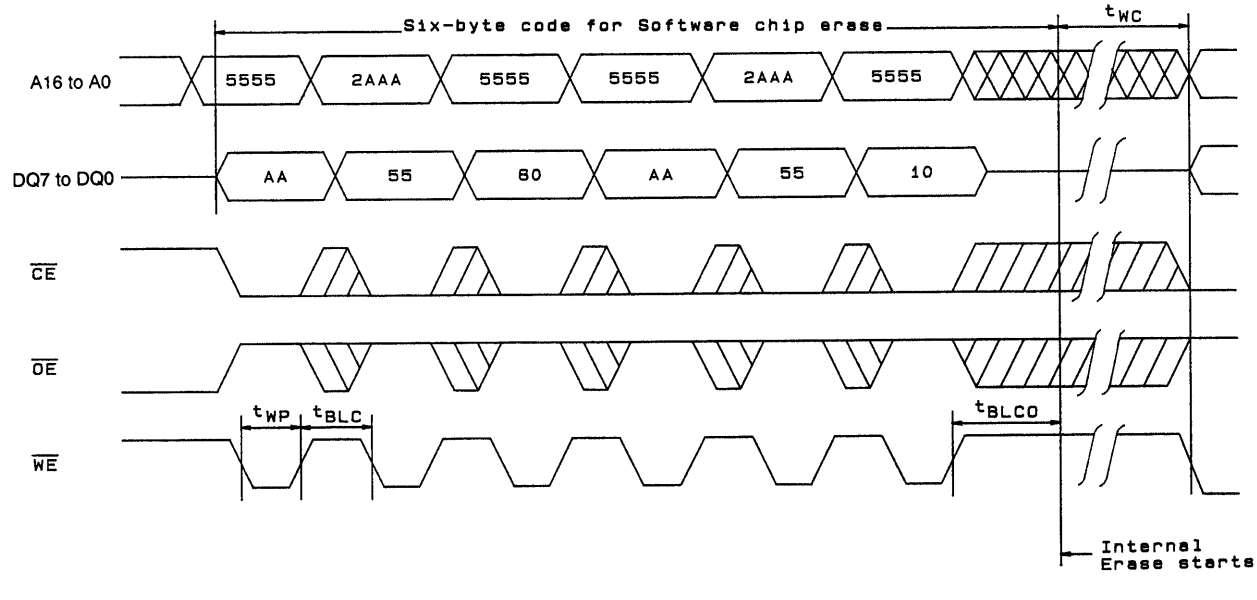
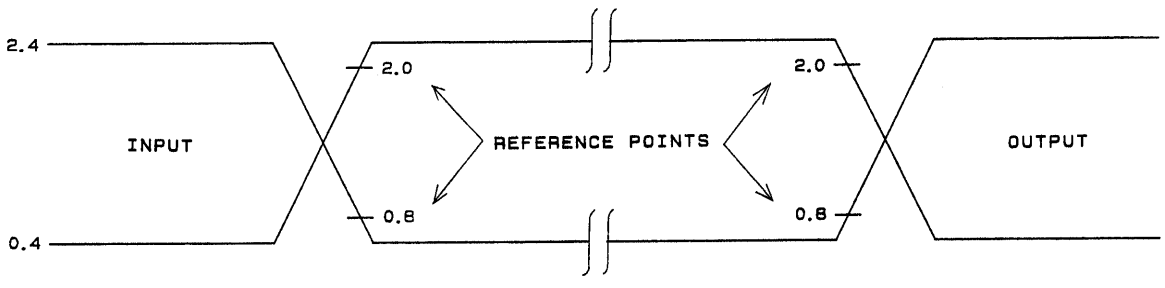


Figure 8 Software Chip Erase



AC test inputs are driven at V_{OH} (2.4 V) for a logic 1 and at V_{OL} (0.4 V) for a logic 0. The I/O measurement reference points are V_{IH} (2.0 V) and V_{IL} (0.8 V). The input rise and fall times (10% ↔ 90%) must be 10 ns or shorter.

Figure 9 AC I/O Reference Waveform

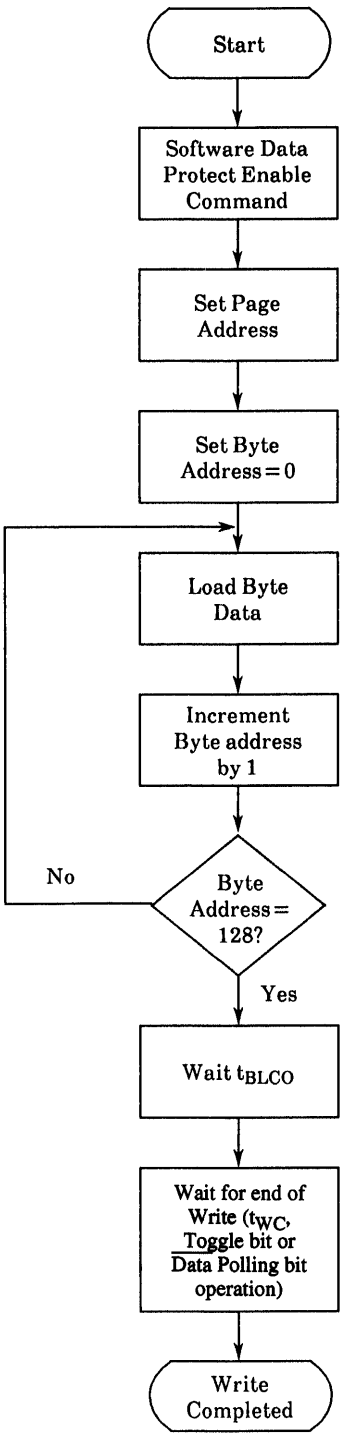


Figure 10 Write Algorithm

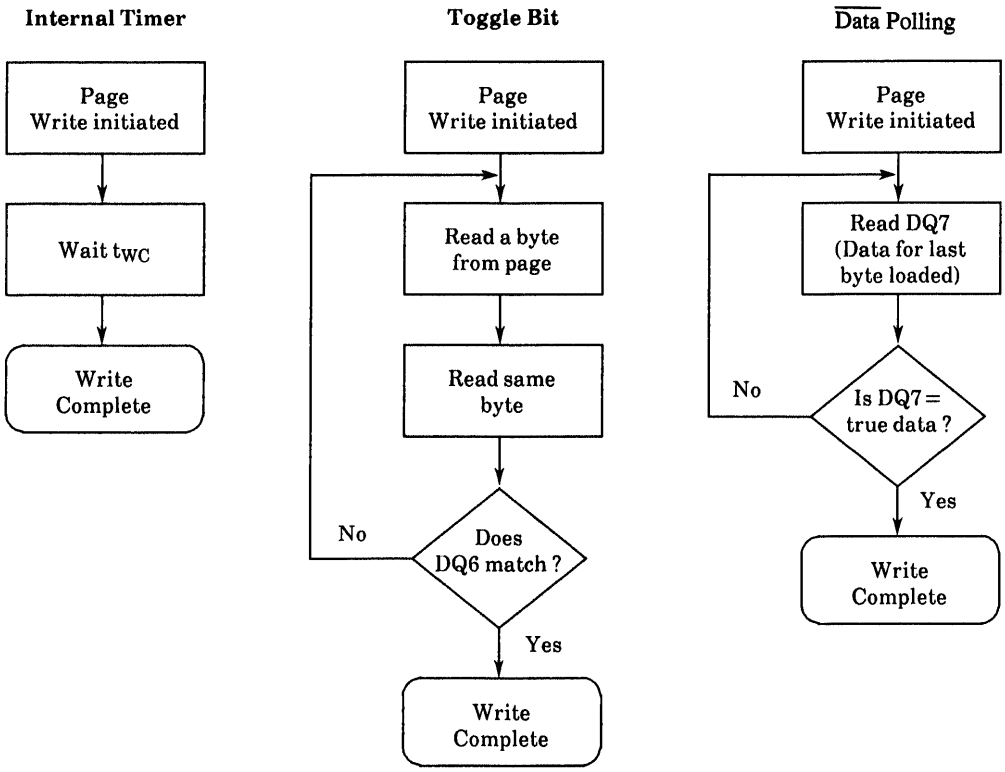


Figure 11 Write Operating State Detection

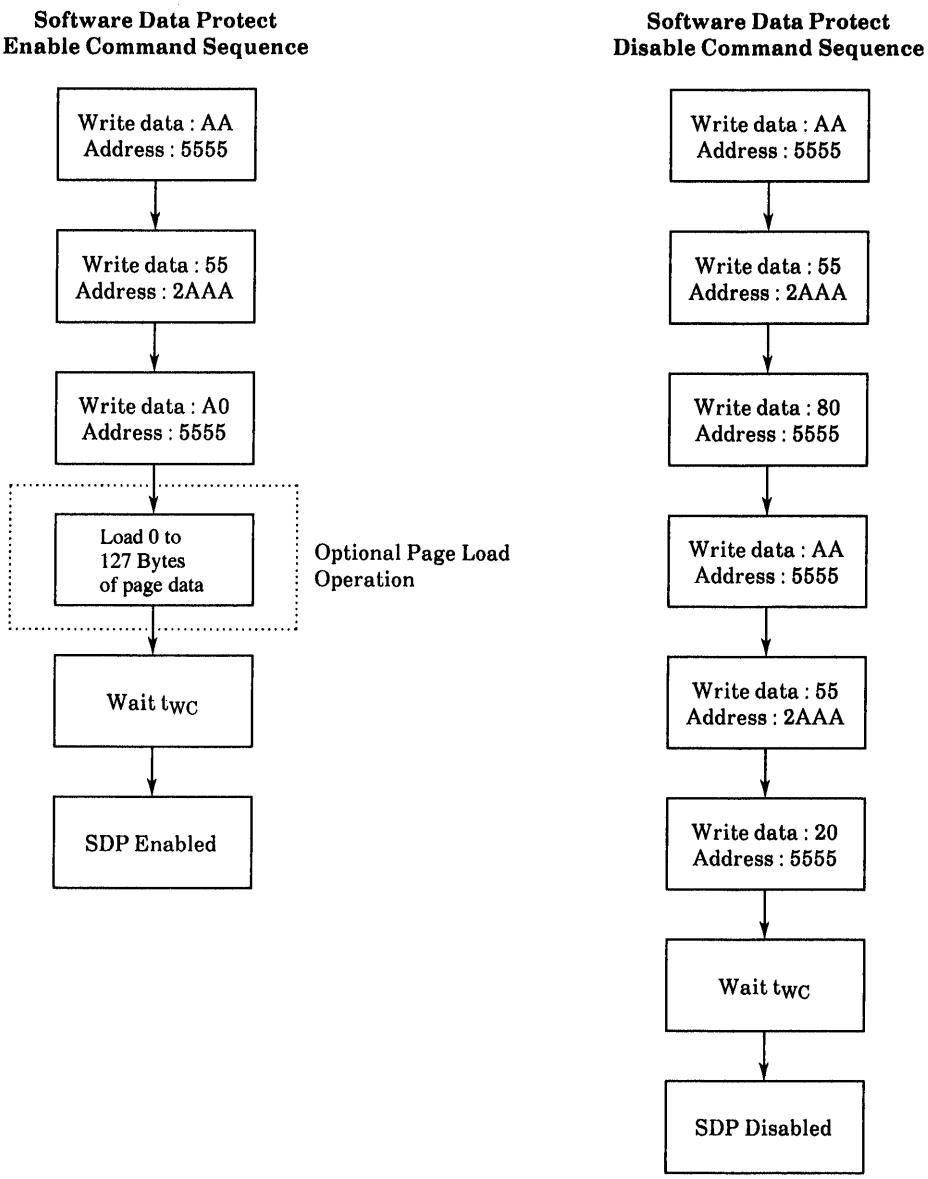


Figure 12 Software Data Protection Flowcharts

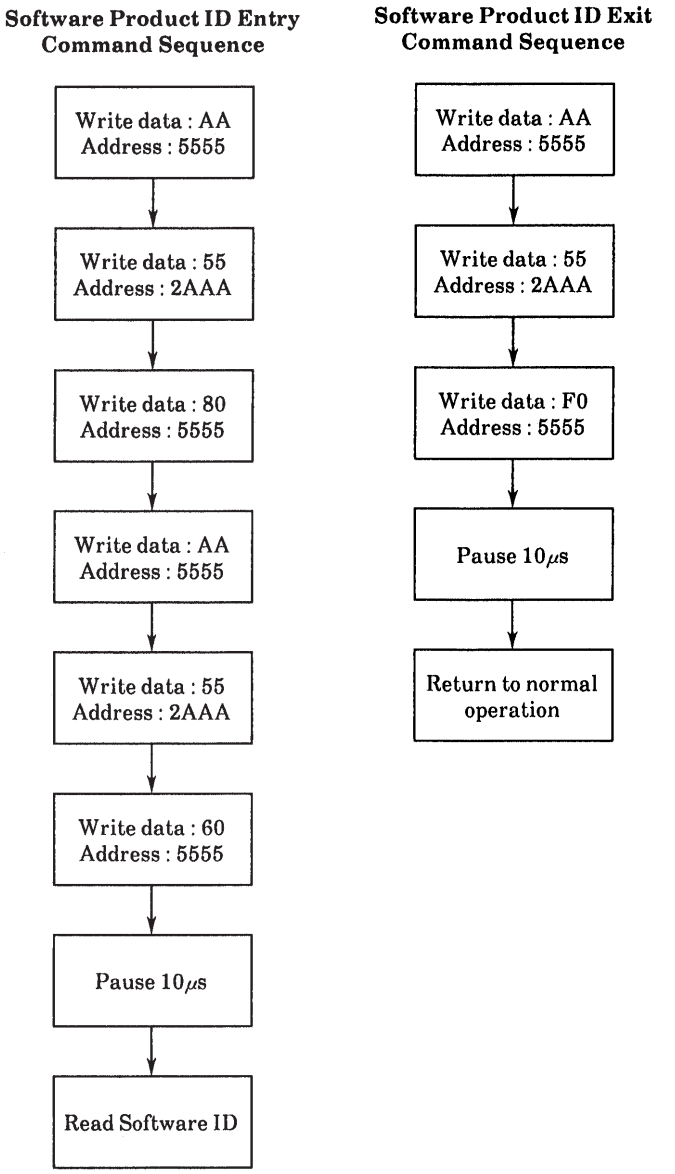


Figure 13 Product ID Flowcharts

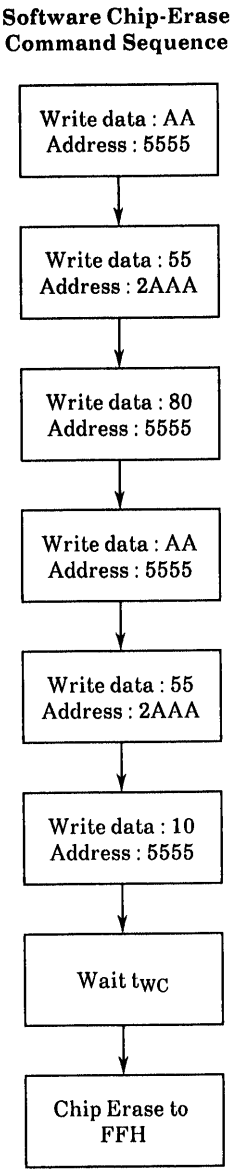


Figure 14
Software Chip-Erase Flowchart