

## Overview

The STK6217 is a hybrid IC that combines in a single package a unidirectional DC motor driver, a PLL constant-speed controller (the LC7991) and associated peripheral components, including a separately excited oscillator, a comparator, and an FG amplifier. The motor controller uses a PLL circuit for precise motor control. The wide range of the STK6217's FG lock frequency allows it to handle a wide range of applications. Since the motor driver block uses MOSFET devices as power elements, it features high output currents (rush current) and low loss.

## Applications

- Plain paper copier DC motor drivers
- FAX paper transport motor drivers
- Other DC motor applications

## Features

### <Motor Controller Block>

- High FG frequency upper limit (locking range: 200 to 2500 Hz)
- Built-in FG divider (FG lock upper limit with divider in use: 5000 Hz)
- Speed lock indicator output directly drives an external LED.
- TTL level compatible  $\overline{\text{ROT}}$  input

## Specifications

### Absolute Maximum Ratings at Ta = 25°C

| Parameter                       | Symbol                 | Conditions                            | Ratings     | Unit |
|---------------------------------|------------------------|---------------------------------------|-------------|------|
| Maximum supply voltage 1        | $V_{CC1 \max}$         | No signal                             | 52          | V    |
| Maximum supply voltage 2        | $V_{CC2 \max}$         | No signal                             | 7           | V    |
| Maximum motor rush current      | $I_O \text{ peak max}$ | Duty 1%, period $\leq 100 \text{ ms}$ | 18          | A    |
| Maximum input voltage           | $V_{IH \max}$          |                                       | 7           | V    |
| Storage temperature range       | $T_{stg}$              |                                       | -40 to +125 | °C   |
| Junction temperature            | $T_j \text{ max}$      |                                       | 150         | °C   |
| Operating substrate temperature | $T_c \text{ max}$      |                                       | 105         | °C   |

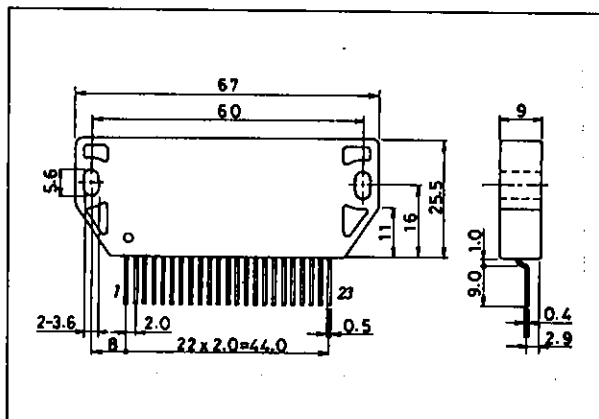
### <Motor Driver Block>

- MOSFET power elements provide high output currents (rush current).
- Low-loss PWM speed controller (built-in externally excited oscillator: 25 kHz)
- Wide power supply voltage range ( $V_{DSS} = 60\text{ V}$ )
- Built-in motor start-up overcurrent limiter

## Package Dimensions

unit: mm

4138



**Allowable Operating Ranges at Ta = 25°C**

| Parameter                  | Symbol           | Conditions                 | Ratings          | Unit |
|----------------------------|------------------|----------------------------|------------------|------|
| Operating supply voltage 1 | V <sub>CC1</sub> | Input active               | 10 to 42         | V    |
| Operating supply voltage 2 | V <sub>CC2</sub> | Input active               | 5 ± 5%           | V    |
| Motor output current       | I <sub>O</sub>   | DC (T <sub>c</sub> = 25°C) | 8                | A    |
| FET withstand voltage      | V <sub>DSS</sub> |                            | 60 min           | V    |
| Input voltage              | V <sub>IH</sub>  |                            | V <sub>CC2</sub> | V    |


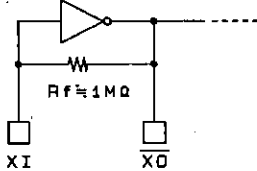
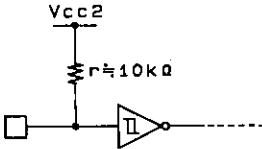
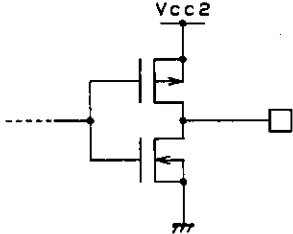
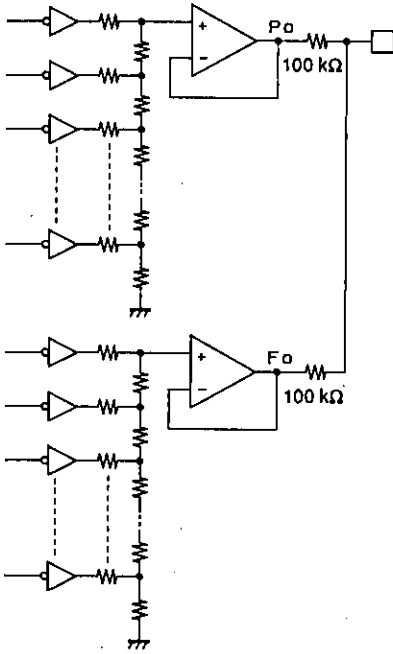
**Operating Characteristics at Ta = 25°C, V<sub>CC1</sub> = 24 V, V<sub>CC2</sub> = 5.0 V**

| Parameter                            | Symbol             | Conditions  | Ratings              |      |                        | Unit             |
|--------------------------------------|--------------------|---|----------------------|------|------------------------|------------------|
|                                      |                    |   | min                  | typ  | max                    |                  |
| V <sub>CC2</sub> current dissipation | I <sub>CC</sub>    | When the ROT input is used                            |                      | 10   | 15                     | mA               |
| Output FET saturation voltage        | V <sub>SAT</sub>   | R <sub>L</sub> = 3 Ω                                  |                      | 0.95 | 1.3                    | V                |
| Built-in oscillator frequency        | f <sub>O</sub>     |   | 21                   | 25   | 31                     | kHz              |
| OSC output amplitude                 | V <sub>OP-P</sub>  |   | 1.9                  | 2.3  | 2.7                    | Vp-p             |
| OSC output effective amplitude       | V <sub>ORMS</sub>  | Pin 7 output voltage                                  | 0.54                 | 0.66 | 0.80                   | V <sub>rms</sub> |
| Common mode input voltage range      | V <sub>ICM</sub>   | Integrating amplifier and FG amplifier input voltage  | 0                    |      | V <sub>CC2</sub> - 1.5 | V                |
| FG amplifier feedback resistance     | R <sub>f</sub>     |   | 95                   | 100  | 105                    | kΩ               |
| High input level voltage             | V <sub>IH</sub>    | DIV1 to DIV3, PR1, PR2 and ROT inputs                 | 0.7 V <sub>CC2</sub> |      | V <sub>CC2</sub>       | V                |
| Low input level voltage              | V <sub>IL</sub>    |   | 0                    |      | 0.3 V <sub>CC2</sub>   | V                |
| High input level current             | I <sub>IH</sub>    | DIV1 to DIV3, PR1 and PR2 inputs                      |                      |      | 1                      | μA               |
| Low input level current              | I <sub>IL</sub>    |   | -1                   |      |                        | μA               |
| High output level current            | I <sub>OH</sub>    | Lock input V <sub>OH</sub> = V <sub>CC2</sub> - 0.4 V |                      |      | -2                     | mA               |
| Low output level current             | I <sub>OL</sub>    | Lock input V <sub>OL</sub> = 0.4 V                    | 2                    |      |                        | mA               |
| Input frequency range                | f <sub>XI</sub>    | XI input  | 0.1                  |      | 10.5                   | MHz              |
|                                      | f <sub>FG</sub>    | FGI input   |                      |      | 50                     | kHz              |
| FG lock frequency                    | f <sub>FLOCK</sub> | FG input divider off                                  | 200                  |      | 2500                   | Hz               |
|                                      | f <sub>FLOCK</sub> | FG input divider on                                   | 400                  |      | 5000                   | Hz               |
| Output cut voltage                   | V <sub>ocut</sub>  | Pin 5 input voltage                                   | 0                    |      | 25                     | mV               |

**Pin Functions**

| Pin No. | Symbol            | Function   |
|---------|-------------------|--|
| 1       | OUT               | Motor output   |
| 2       |                   |  |
| 3       | V <sub>rs</sub>   | Current detection resistor connection                                  |
| 4       |                   |  |
| 5       | V <sub>ref4</sub> | Motor start-up current control reference voltage                       |
| 6       | V <sub>CC2</sub>  | Power supply voltage input (+5 V)                                      |
| 7       | V <sub>ref1</sub> | H/IC built-in oscillator bias voltage setting                          |
| 8       | V <sub>ref2</sub> | Integrating amplifier reference voltage setting                        |
| 9       | V <sub>ref3</sub> | FG input reference voltage setting                                     |
| 10      | FG                | FG input   |
| 11      | R <sub>f</sub>    | Integrating amplifier output   |
| 12      | Mix in            | Integrating amplifier input  |
| 13      | Mix out           | PO and FO sum output (PO and FO each have a 100 kΩ output resistance.) |
| 14      | XI                | Crystal oscillator connection (input)                                  |
| 15      | XO                | Crystal oscillator connection (output)                                 |
| 16      | DIV1              | Variable divider setting   |
| 17      | DIV2              |  |
| 18      | DIV3              |  |
| 19      | PR1               | Phase comparison range select  |
| 20      | PR2               |  |
| 21      | ROT               | Motor rotate/stop input; H: stop, L: rotate                            |
| 22      | Lock              | Lock output; Outputs a low level when locked                           |
| 23      | SG                | Ground   |

# I/O Formats

| Pin No.        | Format   |
|----------------|--|
| 16, 17, 18, 19 |    |
| 14, 15         |    |
| 21             |    |
| 22             |  |
| 13             |  |



## Operating Principles

### 1. Overview

Figure 1 shows the block diagram for the STK6217. The PLL control block compares the frequencies and phases of the FG signal frequency fed back from the motor with a reference clock, which is formed by dividing a reference signal. When they agree, the frequency is locked with a 50% duty. The control signals consist of two systems with D/A converted outputs: FO, which is the frequency control output and PO, which is the phase control output. Since PLL control provides a motor speed that is synchronized with a reference clock frequency  $f_{ref}$ , which is created by dividing a reference signal, the stability of  $f_{ref}$  directly influences the stability of the rotation. Therefore, quartz precision digital control is possible by using a crystal oscillator for reference signal generation. The control signals are added by an integration circuit, which also functions as an active filter. It is here that the servo system gain and phase compensation are performed. The output of this system is sent to the PWM conversion block and a PWM signal, which is based on the period of an associated oscillator circuit, is input to the unidirectional driver of the final stage, which drives the DC motor.

### 2. Motor Speed, Resonant Frequency, and Encoder Pulse Count

The frequency  $f_{FG}$  of the signal generated by the encoder is given by:

$$f_{FG} \text{ (Hz)} = \frac{N \text{ (rpm)}}{60} \times P \text{ (P/R)} \dots\dots\dots ①$$

Where, N: Motor speed (rpm)

P: Number of pulses per encoder rotation

Formula ① can be transformed as follows:

$$N \text{ (rpm)} = \frac{60 \times f_{FG}}{P \text{ (P/R)}} \dots\dots\dots ②$$

Alternatively,

$$P \text{ (P/R)} = \frac{60 \times f_{FG}}{N} \dots\dots\dots ③$$

Here, the relationship with the oscillator resonant frequency is given by:

$$N \text{ (rpm)} = \frac{60}{P} \times \frac{f_{xtal}}{DIV \times 2050 \text{ (1025)}} \dots\dots\dots ④$$

Alternatively,

$$P \text{ (P/R)} = \frac{60}{N} \times \frac{f_{xtal}}{DIV \times 2050 \text{ (1025)}} \dots\dots\dots ⑤$$

Here, DIV: Variable divider ratio

See item 3-1, subsection (3).

The value (1025) is used when the  $f_{FG}$  input frequency is divided by 2 (as determined by DIV setting).

See item 3-1, subsection (3).

Note that the following three methods for increasing the stability of the motor speed can be considered.

- ① Increasing the number of encoder output pulses for a given motor speed.
- ② Not using the FG divider if at all possible, since using it decreases the precision of the rotation data.
- ③ Setting the divider ratio to as low a value as possible, so that the oscillator precision is not reduced.

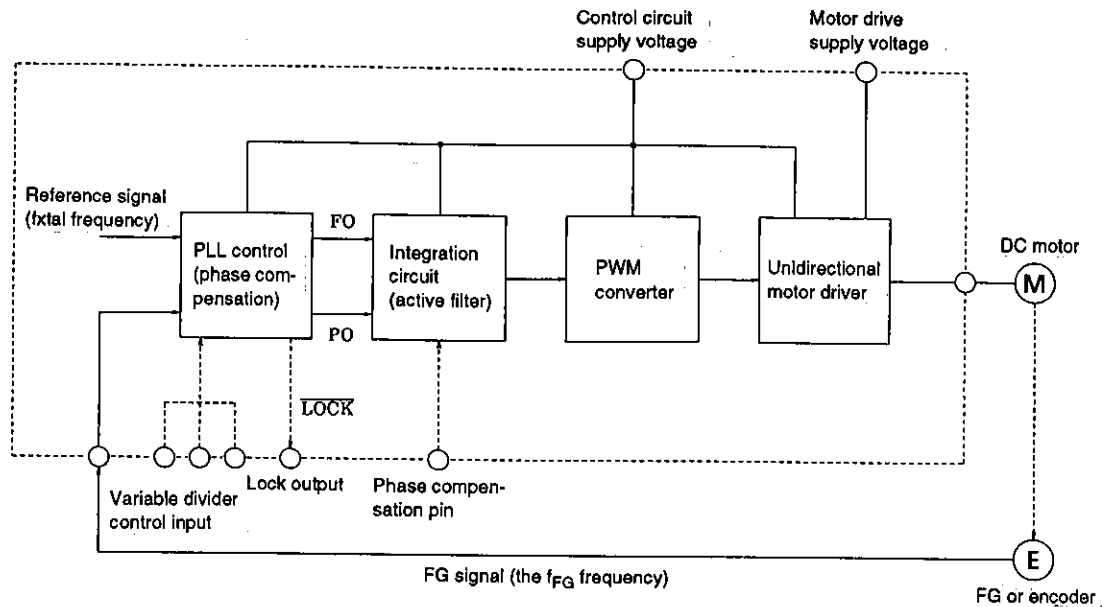


Figure 1 STK6217 Block Diagram

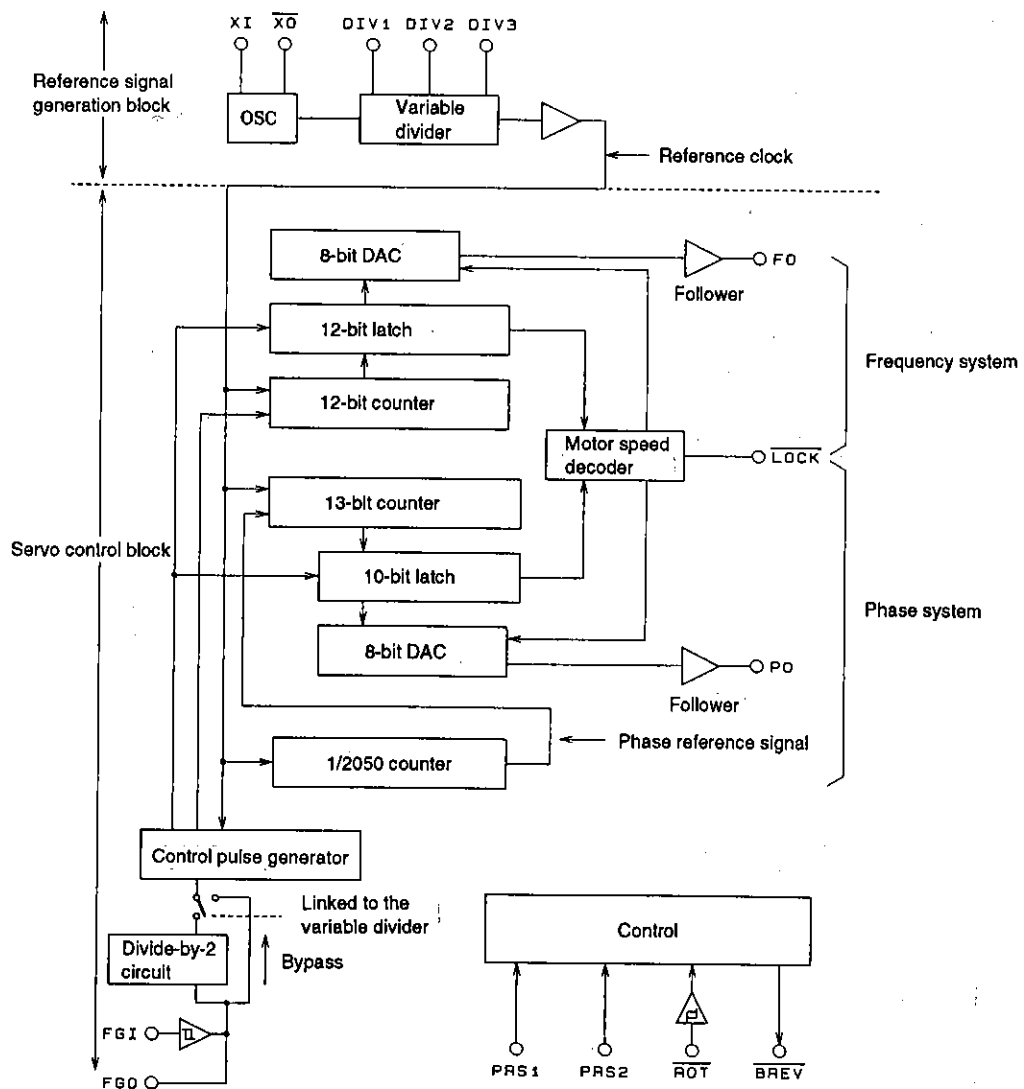


Figure 2 PLL IC Block Diagram

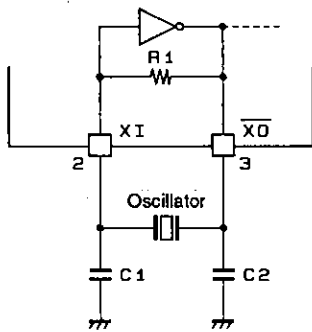
### 3. Block Functional Descriptions

#### 3-1 Reference Signal Generation Block

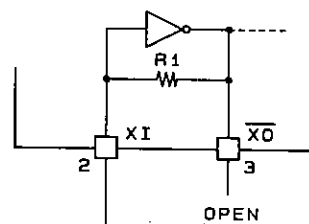
##### (1) Crystal oscillator circuit

The controller block generates a reference clock using a crystal oscillator and a capacitor connected to the XI and  $\overline{XO}$  pins. It is also possible to leave the  $\overline{XO}$  pin open and input an external clock to the XI pin.

Reference oscillator calculation



External clock input



The external clock should be a square wave with an amplitude of 5 V and a duty of approximately 50%.  $V_{DD} = 5\text{ V}$ .

##### (2) Crystal resonant frequency calculation

After determining the FG frequency to be locked, use the following formula to derive the required crystal frequency.

- With the FG divider off  

$$f_{xtal} = f_{FGLock} \times DIV \times 2050\text{ (Hz)}$$
- With the FG divider on  

$$f_{xtal} = f_{FGLock} \times DIV \times 1025\text{ (Hz)}$$

Where:

- $f_{xtal}$ : Crystal resonant frequency  
 $f_{FGLock}$ : The FG frequency to be locked  
 $DIV$ : The variable divider ratio

##### (3) Variable divider and the FG divider

The controller block includes a 6-setting variable divider and an FG divider (divide-by-2, by-passable) to expand the range of input FG frequencies. These dividers are controlled by the three pins DIV1, DIV2 and DIV3 as shown in Table 1.

**Table 1 Divider Control**

| Control input |            |            | Variable divider ratio | FG divider |
|---------------|------------|------------|------------------------|------------|
| DIV3          | DIV2       | DIV1       |                        |            |
| High level    | High level | High level | 20                     | OFF        |
| High level    | High level | Low level  | 10                     | OFF        |
| High level    | Low level  | High level | 6                      | OFF        |
| High level    | Low level  | Low level  | 3                      | OFF        |
| Low level     | High level | High level | 2                      | OFF        |
| Low level     | High level | Low level  | 1                      | OFF        |
| Low level     | Low level  | High level | 2                      | ON         |
| Low level     | Low level  | Low level  | 1                      | ON         |

### 3-2 Servo Control Block

The servo block compares the reference clock generated by the reference signal generation block with the FGI input (the FG signal input from the motor) and generates three output signals: FO (frequency system control output), PO (phase system control output), and  $\overline{\text{Lock}}$  (the lock indicator output). The FO and PO outputs are 8-bit D/A converter outputs. The motor drive signal is created from these two outputs. The  $\overline{\text{Lock}}$  output indicates whether the motor is within the lock range.

#### (1) Servo Operation

Control system operation is divided into the following three aspects depending on the input FG frequency: drive, tracking (locked), and brake.

| FG input frequency                        | Operation | $\overline{\text{Lock}}$ output | FO output                                | PO output                            |
|---|-----------|---------------------------------|--|--------------------------------------|
| $> f_{\text{FGLock}} + 6\%$<br>Overspeed  | Brake     | High level                      | Low level                                | Low level                            |
| $f_{\text{FGLock}} \pm 6\%$<br>Lock range | Tracking  | Low level                       | DA output (frequency-voltage conversion) | DA output (phase-voltage conversion) |
| $< f_{\text{FGLock}} - 6\%$<br>Underspeed | Drive     | High level                      | High level                               | High level                           |

Notes

$$f_{\text{FGLock}} = \frac{f_{\text{xtal}}}{\text{DIV} \times 2050 (1025)} \text{ (Hz)}$$

Caution: The value in parentheses is used when the FG divider is on.

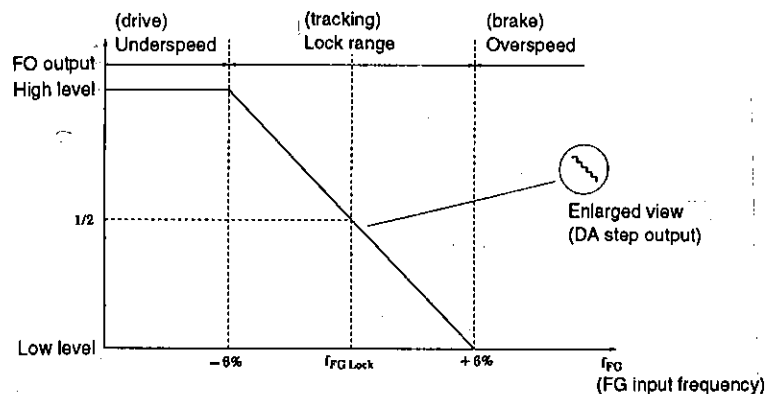
$f_{\text{FGLock}}$ : FG frequency when locked;  $f_{\text{xtal}}$ : Crystal resonant frequency; DIV: Variable divider ratio

- The drive operation is performed at start-up (underspeed) time.
- When the FO and PO outputs are set to the high level, the motor is driven at full speed.
- Braking operation is performed when the motor is in overspeed range.
- When the FO and PO outputs are set to the low level, the motor brake is applied.
- The servo control block controls the motor by using these two operations to pull the motor speed into the lock range.  
(Note that the operations described up to this point are the rough adjustments performed by the frequency system.)

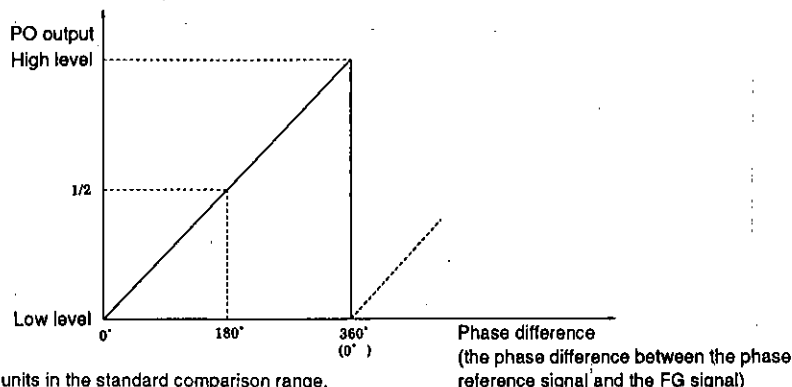
#### (2) FO and PO outputs (frequency system control output and phase system control output)

When the FG input frequency enters the lock range, the servo control switches to tracking operation. Frequency system fine control and phase system control starts, and the FO and PO outputs are switched to voltage outputs from internal D/A converters. Since the internal D/A converters are 8-bit converters, these output voltages have 256 possible levels. The figures below show the FO and PO output characteristics.

##### ● FO Output Characteristics



##### ● PO Output Characteristics (during tracking)



Caution: These characteristics are for units in the standard comparison range.



### 3-3 Accessory Functions

#### (1) $\overline{\text{ROT}}$ input (rotate/stop)

The  $\overline{\text{ROT}}$  input turns the motor on or off.

| ROT input  | State   | FO output | PO output |
|------------|---------|-----------|-----------|
| High level | Stop    | Low level | Low level |
| Low level  | Operate | *         | *         |

\*: Determined by the motor control function.

#### (2) PRS1 and PRS2 inputs (phase comparison range selection)

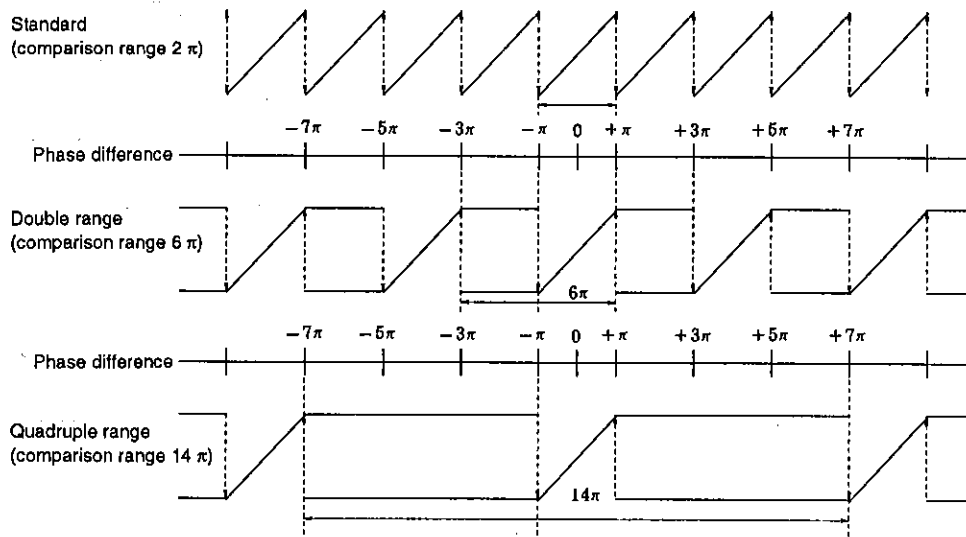
The phase system comparison range can be switched using the PRS1 and PRS2 inputs.

#### Phase System Comparison Range Selection

| PRS2 input | PRS1 input | Range name      | Comparison range | Phase output frequency    |
|------------|------------|-----------------|------------------|---------------------------|
| Low level  | Low level  | Standard range  | $2\pi$           | Once every FG input       |
| Low level  | High level | Test mode       | .....            | .....                     |
| High level | Low level  | Double range    | $6\pi$           | Once every two FG inputs  |
| High level | High level | Quadruple range | $14\pi$          | Once every four FG inputs |

Caution: The phase range becomes more than two and four times the normal range due to the operation of a built-in limiter. These phase output frequency values are divided by two when the FG divider is used.

#### ● Phase Output Characteristics



Caution: The "phase difference" is the phase difference in the FG signal input with respect to the internal reference signal. The double and quadruple ranges have hysteresis.

#### ● FG Clock Frequencies (examples)

| Variable divider ratio | FG divider | Oscillator resonant frequency (MHz) |      |      |      |       | Unit |
|------------------------|------------|-------------------------------------|------|------|------|-------|------|
|                        |            | 2.05                                | 4.1  | 6.15 | 8.2  | 10.25 |      |
| 20                     | OFF        | 50                                  | 100  | 150  | 200  | 250   | Hz   |
| 10                     |            | 100                                 | 200  | 300  | 400  | 500   | Hz   |
| 6                      |            | 116                                 | 333  | 500  | 667  | 833   | Hz   |
| 3                      |            | 333                                 | 667  | 1000 | 1333 | 1667  | Hz   |
| 2                      |            | 500                                 | 1000 | 1500 | 2000 | 2500  | Hz   |
|                        | ON         | 1000                                | 2000 | 3000 | 4000 | 5000  | Hz   |

The following two ceramic oscillators, which are available as commercial products, can be used.

CSA6.14MT (Murata) ... Handles FG frequencies of 500, 1000 and 1500 Hz.

CSA8.20MT (Murata) ... Handles an FG frequency of 2000 Hz.

#### 4. Rush Current Limiter Circuit

##### 4-1 Circuit Purpose

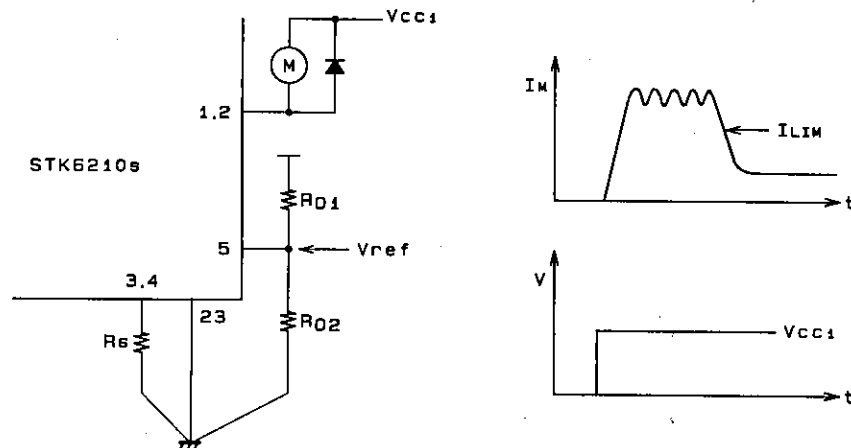
The STK6217 provides a function that can limit the current when the motor starts (or brakes). This function allows the external current (peak) output capacity to be reduced. The rush current limit value can be changed arbitrarily by adjusting the value of an external resistor.

##### 4-2 Setting the Limit Value

Figure 3 shows the method for setting the limit value. The  $V_{ref}$  voltage is adjusted by changing the value of  $RO2$ . Formula 6 is the formula for the limit value,  $I_{LIM}$ .

$$I_{LIM} (A) \approx \underbrace{\frac{RO2}{RO1 + RO2}}_{V_{ref}} \times V_{CC2} \times \frac{1}{R_s} \quad \text{⑥}$$

$RO1$ : 6.8 k $\Omega$  (fixed)  
 $RO2$ : Variable  
 $V_{CC2}$ : 5 V  
 $R_s$ : Current detection resistance ( $\Omega$ )



**Figure 3 External Peripheral Circuit and Motor Start-up Timing Chart**

- Caution:**
- Here, the  $V_{ref}$  voltage must be set in a range that fulfills the following condition.  
 $V_{ref} \geq 0.025 \text{ V}$  (However,  $V_{CC2} = 5 \text{ V} \pm 5\%$  is the alteration condition.)  
 The limiter function will not operate if the above condition is not met.
  - Although formula ⑥ can be used as a rough formula for setting the output current, the actual value will differ due to the influence of voltage drops due to the ground pattern design external to the hybrid IC. Therefore we recommend that  $I_{LIM}$  final confirmation be performed in a circuit that has a form close to that of the PCB final pattern.

##### 4-3 Value of the Current Detection Resistor ( $R_s$ )

$R_s$  detects current flowing from the motor, and the voltage drop across  $R_s$  is sensed by an internal comparator. When an external  $R_s$  is connected to the STK6217, a resistor with a value that fulfills the following condition must be used.

$$R_s \times I_{LIM} \leq 0.5 \text{ V} \quad \text{⑦}$$

Also, the PCB pattern should be designed so that  $R_s$ ,  $RO2$  and the STK6217's ground pin (pin 23) are connected to a single ground point as close as possible to the STK6217 in the pattern. In particular,  $R_s$  and the STK6217's pins 3 and 4 must not be located any significant distance from the IC.

## 5. MOSFET Drain-Source Overvoltage

When using the STK6217, a diode is connected in parallel with the DC motor as a regenerative diode for the motor. This also functions as a protective measure against excessive MOSFET flyback voltage. Flyback voltage is due to the influence of circuit factors such as lead inductances, and will remain when the MOSFET turns off. (In general, these voltages are a few volts for periods of up to 0.5  $\mu$ s.) Therefore, as a final circuit operation check, confirm that the flyback voltage does not exceed  $V_{OSS}$ .

## 6. Thermal Design

Applications must be designed so that the temperature of the STK6217's aluminum substrate side never exceeds 105°C in any situation. The remainder of this section discusses thermal design for the STK6217.

### 6-1 Hybrid IC Average Internal Loss Derivation

The main component of the average internal loss occurs in the MOSFET, which is the PWM element.

The MOSFET loss is expressed as follows:

$$P_d (W) = V_{SAT} \times I_M \times f_p \times t_{ON} \dots\dots\dots ⑧$$

$V_{SAT}$ : FET saturation voltage  
 $I_M$ : Motor output peak current  
 $t_{ON}$ : FET on time  
 $f_p$ : IC internal oscillator frequency

### 6-2 Deriving the heat sink size

Formula ⑨ shows the thermal resistance of the required heat sink.

$$\theta_{c-a} (^{\circ}C/W) = \frac{T_c \text{ max} - T_a}{P_d} \dots\dots\dots ⑨$$

A heat sink that is appropriate for  $\theta_{c-a}$  must be selected. (Note that  $\theta_{c-a}$  for the STK6217 is 18.5°C/W.)

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