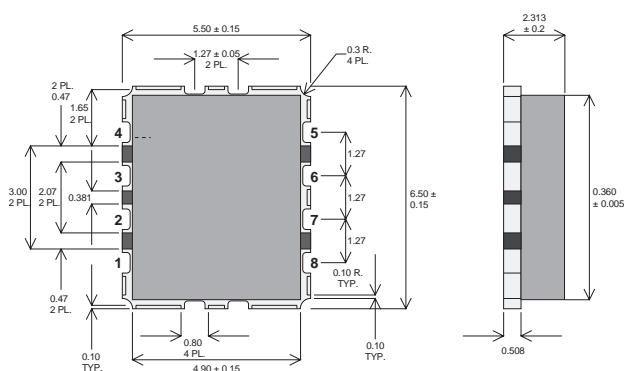


MECHANICAL DATA

Dimensions in mm.



F-0127 PACKAGE

PIN 1 – SOURCE	PIN 5 – SOURCE
PIN 2 – DRAIN	PIN 6 – GATE
PIN 3 – DRAIN	PIN 7 – GATE
PIN 4 – SOURCE	PIN 8 – SOURCE

Ceramic Material: Alumina.

Parts can also be supplied with AlN or BeO for improved thermal resistance.

Contact Semelab for details.

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 10W – 12.5V – 500MHz SINGLE ENDED

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- VERY LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 10 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from 1 MHz to 1 GHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	30W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	10A
T_{stg}	Storage Temperature	-65 to $150^{\circ}C$
T_j	Maximum Operating Junction Temperature	$200^{\circ}C$

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{DSS} Drain–Source Breakdown Voltage	V _{GS} = 0 I _D = 10mA	40			V
I _{DSS} Zero Gate Voltage Drain Current	V _{DS} = 12.5V V _{GS} = 0			1	mA
I _{GSS} Gate Leakage Current	V _{GS} = 20V V _{DS} = 0			1	μA
V _{GS(th)} Gate Threshold Voltage*	I _D = 10mA V _{DS} = V _{GS}	0.5		7	V
g _{fs} Forward Transconductance*	V _{DS} = 10V I _D = 1A	0.8			S
G _{PS} Common Source Power Gain	P _O = 10W	10			dB
η Drain Efficiency	V _{DS} = 12.5V I _{DQ} = 0.4A	50			%
VSWR Load Mismatch Tolerance	f = 500MHz	20:1			—
C _{iss} Input Capacitance	V _{DS} = 0V V _{GS} = –5V f = 1MHz			60	pF
C _{oss} Output Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			40	pF
C _{rss} Reverse Transfer Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			4	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 6°C / W
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