

TECHNICAL DATA
Datasheet 4165, Rev. B**Three-Phase IGBT BRIDGE, With Gate Driver and Optical Isolation****DESCRIPTION:** A 1200 VOLT, 60 AMP, THREE PHASE IGBT BRIDGE**ELECTRICAL CHARACTERISTICS PER IGBT DEVICE**(T_j=25°C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|----------------------|------|------------|----------|----------|
| IGBT SPECIFICATIONS | | | | | |
| Collector to Emitter Breakdown Voltage I _C = 500 μA, V _{GE} = 0V | BV _{CES} | 1200 | - | - | V |
| Continuous Collector Current T _C = 25 °C T _C = 90 °C | I _C | - | - | 60 40 | A |
| Pulsed Collector Current, Pulse Width limited by T _{jMax} | I _{CM} | - | - | 100 | A |
| Gate to Emitter Voltage | V _{GE} | - | - | +/-20 | V |
| Gate-Emitter Leakage Current , V _{GE} = +/-20V | I _{GES} | - | - | +/- 200 | nA |
| Zero Gate Voltage Collector Current V _{CE} = 1200 V, V _{GE} =0V T _i =25°C V _{CE} = 800 V, V _{GE} =0V T _i =125°C | I _{CES} | - | - | 1 10 | mA mA |
| Collector to Emitter Saturation Voltage, I _C = 40A, V _{GE} = 15V, T _j = 25 °C T _j = 125 °C | V _{CE(SAT)} | - | 1.9 2.1 | 2.3 - | V |
| Maximum Thermal Resistance | R _{θJC} | - | - | 0.6 | °C/W |
| Maximum operating Junction Temperature | T _{jmax} | -40 | - | 150 | °C |
| Maximum Storage Junction Temperature | T _{jmax} | -55 | - | 150 | °C |

SENSITRON**TECHNICAL DATA****Datasheet 4165, Rev. B**

| Over-Temperature Shutdown | | | | | |
|--------------------------------------|-----|----|-----|-----|---------|
| Over-Temperature Shutdown | Tsd | 90 | 100 | 115 | °C |
| Over-Temperature Output | Tso | | 10 | | 10mV/°C |
| Over-Temperature Shutdown Hysteresis | | | 20 | | °C |

| ULTRAFAST DIODES RATING AND CHARACTERISTICS | | | | | |
|---|-----------------|------|------------|------|------|
| Diode Peak Inverse Voltage | PIV | 1200 | - | - | V |
| Continuous Forward Current, $T_C = 90^\circ\text{C}$ | I_F | - | - | 40 | A |
| Forward Pulse Current, Pulse Width limited by $T_{j\text{Max}}$ | I_{FP} | - | - | 100 | A |
| Diode Forward Voltage, $I_F = 40\text{A}$, $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$ | V_F | - | 1.8 1.8 | 2.3 | V |
| Diode Reverse Recovery Time ($I_F = 40\text{A}$, $V_{RR} = 600\text{V}$, $di/dt = 800\text{ A}/\mu\text{s}$) | t_{rr} | - | 240 | - | nsec |
| Maximum Thermal Resistance | $R_{\theta JC}$ | - | - | 1.0 | °C/W |
| Gate Driver | | | | | |
| Supply Voltage | VCC | 10 | 15 | 20 | V |
| Input On Current | HIN, LIN | 2 | | 5.0 | mA |
| Opto-Isolator Logic High Input Threshold | I_{th} | - | 1.6 | - | mA |
| Input Reverse Breakdown Voltage | BV_{in} | 5.0 | - | - | V |
| Input Forward Voltage @ $I_{in} = 5\text{mA}$ | V_F | - | 1.5 | 1.7 | V |
| Under Voltage Lockout | VCCUV | 11.5 | - | 12.5 | V |
| ITRIP Reference Voltage ⁽¹⁾ | $I_{trip-ref}$ | 2.5 | 2.6 | 2.7 | V |
| Input-to-Output Turn On Delay | t_{ond} | - | TBD | - | nsec |
| Output Turn On Rise Time | t_r | - | TBD | - | |
| Input-to-Output Turn Off Delay | t_{offd} | - | TBD | - | |
| Output Turn Off Fall Time | t_f | - | TBD | - | |
| @ VCC=400V, IC=40A, $T_C = 25$ | | | | | |
| Input-Output Isolation Voltage | - | 1500 | - | - | V |

(1) ITRIP Cycle-by cycle current limit is internally set to 43A peak. The set point can be lowered by connecting a resistor between $I_{trip-ref}$ and Gnd. The set point can be increased by connecting a resistor between $I_{trip-ref}$ and +5V ref

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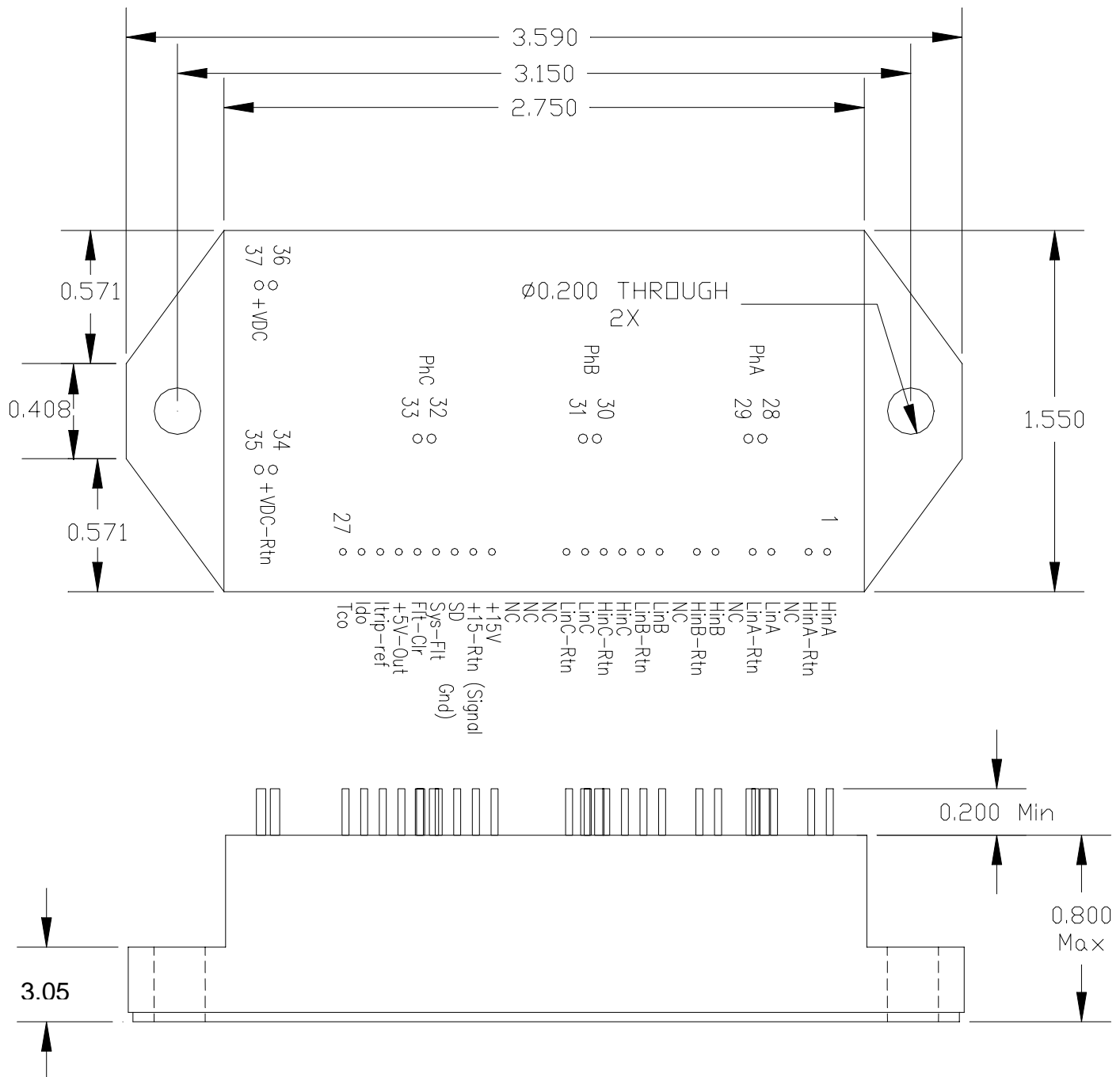
| Pin Number | Function | Pin Number | Function |
|------------|--|------------|---|
| 1 | Isolated Input for High-side IGBT of Phase A | 18 | NC |
| 2 | Return for Input at 1 | 19 | +15V Input |
| 3 | NC | 20 | +15V Rtn (Signal Ground) ⁽³⁾ |
| 4 | Isolated Input for Low-side IGBT of Phase A | 21 | SD ⁽³⁾ |
| 5 | Return for Input at 4 | 22 | Fault Output ⁽³⁾ |
| 6 | NC | 23 | Fault Clear Input ⁽³⁾ |
| 7 | Isolated Input for High-side IGBT of Phase B | 24 | +5V Output |
| 8 | Return for Input at 7 | 25 | Over-Current Trip Set Point ⁽³⁾ |
| 9 | NC | 26 | DC Bus Current Output with Total Gain of 0.06 V/A |
| 10 | Isolated Input for Low-side IGBT of Phase B | 27 | Case Temperature Output with Gain of 0.010 V/°C |
| 11 | Return for Input at 10 | 28 & 29 | Phase A Output |
| 12 | Isolated Input for High-side IGBT of Phase C | 30 & 31 | Phase B Output |
| 13 | Return for Input at 12 | 32 & 33 | Phase C Output |
| 14 | Isolated Input for Low-side IGBT of Phase C | 34 & 35 | DC Bus "+VDC Return" |
| 15 | Return for Input at 14 | 36 & 37 | DC Bus "+VDC" Input |
| 16 | NC | Case | Isolated From All Terminals |
| 17 | NC | | |

SENSITRON

TECHNICAL DATA

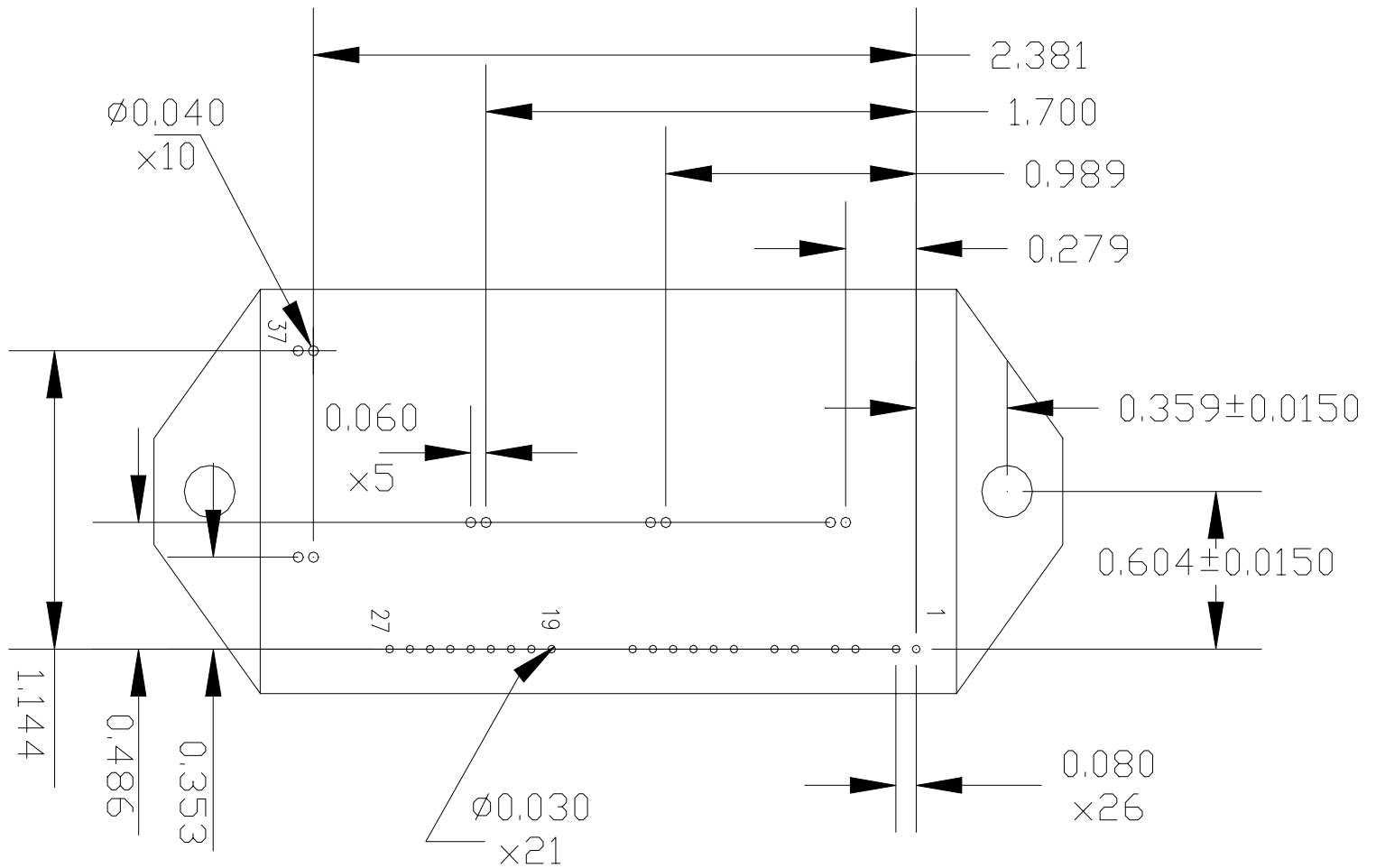
Datasheet 4165, Rev. B

Package Drawing Top View
(All dimensions are in inches, tolerance is +/- 0.010")



SENSITRON**TECHNICAL DATA**

Datasheet 4165, Rev. B

Package Pin Locations**(All dimensions are in inches; tolerance is +/- 0.005" unless otherwise specified)**

SENSITRON**TECHNICAL DATA****Datasheet 4165, Rev. B**

Application Notes:**a- Shutdown Feature:**

- 1- Pin 21, SD, is a dual function input/output, active low input. It is internally pulled high. As a low input, it shuts down all IGBTs regardless of the Hin and Lin signals.
- 2- SD is also internally activated by the over-temperature shutdown, over-current limit, under-voltage shutdown, and desaturation protection.
- 3- Over-temperature shutdown, and over-current limit are not latching features.
- 4- Under-voltage shutdown is automatically reset once the VCC rises above the 12.1V threshold limit.
- 5- Desaturation shutdown is a latching feature and internally reset.
- 6- When any of the internal protection features is activated, SD is pulled down.
- 7- SD can be used to shutdown all IGBTs by an external command. An open collector switch shall be used to pull down SD externally.
- 8- Also, SD can be used as a fault condition output. Low output at SD indicates a fault situation.

b- Fault Output Feature:

- 1- Pin 22, Flt is a dual function pin. It is internally pulled high. If pulled down, it will freeze the status of all the six IGBTs regardless of the Hin and Lin signals
- 2- Pin 22 as an output reports desaturation protection activation. When desaturation protection is activated a low output for about 9 μ sec is reported.
- 3- If any other protection feature is activated, it will not be reported by Pin 22.

c- Fault Clear Output:

- 1- Pin 23, Flt-Clr is a fault clear input. It can be used to reset a latching fault condition, due to desaturation protection.
- 2- Pin 23 is internally pulled down. A latching fault due to desaturation can be cleared by pulling high this input.
- 3- An internal fault clear is activated after 100 μ sec delay. If desired to clear the fault earlier, this input can be used.

d- Signal Ground:

Pin 20, Signal Gnd is a the signal ground for all signals at Pins 19 through 27. This ground is internally connected to the +VDC Rtn. **No external connection shall be established between Signal Gnd and +VDC Rtn.**