

ID343K01

Flash Miniature Card

16M

(Model No.: ID343K01)

Spec No.: U810006

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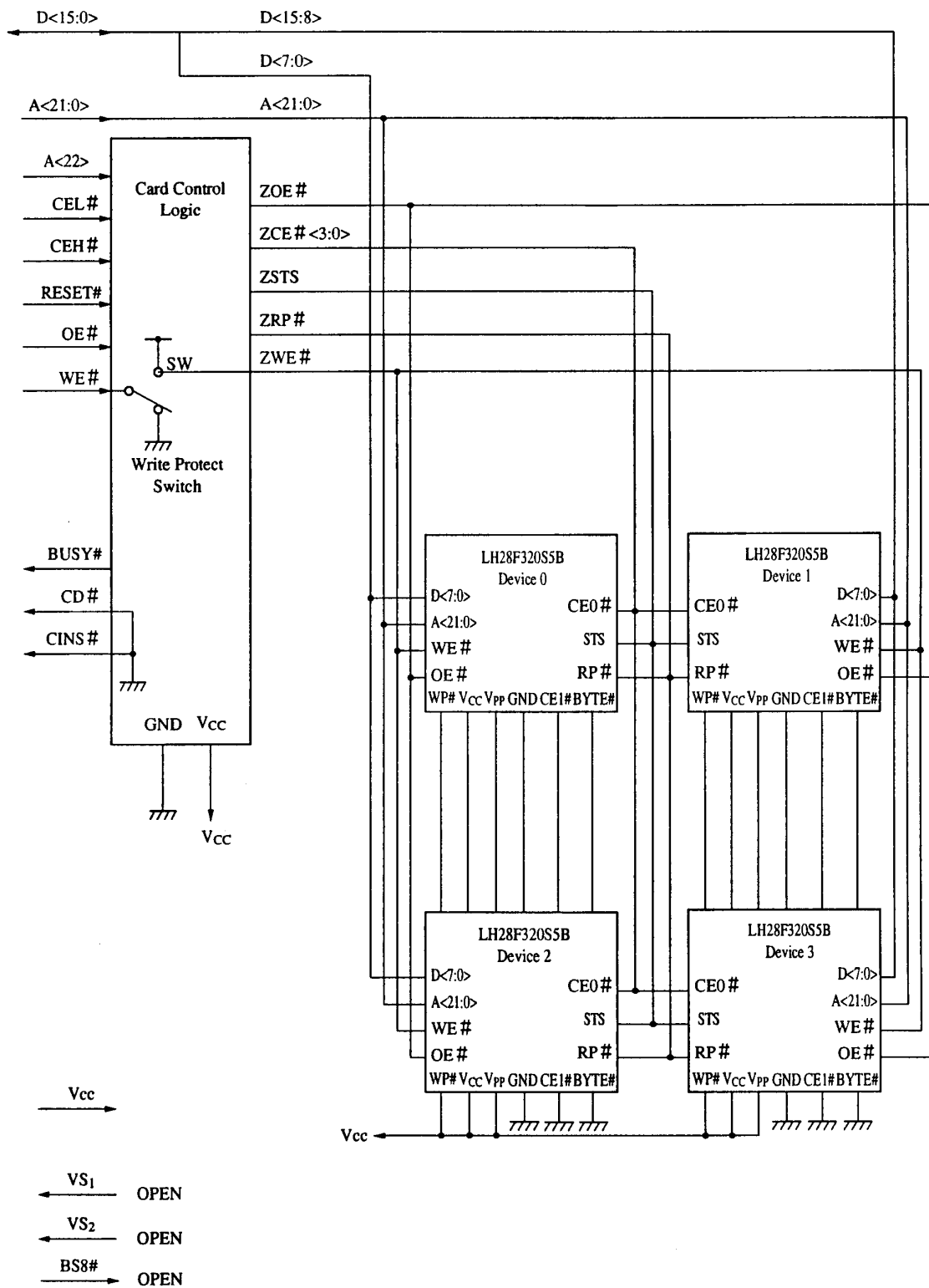
1. General Descriptions

The SHARP ID343K01, which panel design is SHARP standard, is a 16MB Flash Memory Miniature Card conforms to Miniature Card Specification Release 1.1 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

2. Features

- | | | |
|------|--|--|
| 2.1 | Type | 16MB Flash Memory Miniature Card
(Conforms to Miniature Card Specification Release 1.1) |
| 2.2 | Memory Capacity | |
| | Main Memory | 8M words × 16 bits (16M words × 8 bits) |
| 2.3 | Supply Voltage | 5.0V ± 5% |
| 2.4 | Erase Unit | 64K word Blocks |
| 2.5 | Program/Erase Cycles | 100,000 cycles per Block |
| 2.6 | Interface | Parallel I/O Interface |
| 2.7 | Function Table | See Function Table in page. 10 |
| 2.8 | External Dimensions | 33.0 × 38.0 × 3.5 mm |
| 2.9 | Pin Connections | See Pin Connections in page. 5 |
| 2.10 | Type of Connector | Conforms to Miniature Card Specification Release 1.1 Card Use Connector |
| 2.11 | Average Weight | 9g |
| 2.12 | Operating Temp. Range | 0 to 60°C |
| 2.13 | Storage Temp. Range | -30 to 70°C |
| 2.14 | External Appearance | External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales. |
| 2.15 | Manufacturer's Code | The manufacturer's code shall be printed on the Miniature card directly or on the seal which is then attached to the Miniature card. |
| 2.16 | Brand Name | The user's brand name will used. |
| 2.17 | Not designed for rated radiation hardened. | |

3. Block Diagram



4. Pin Connections

PAD#	SIGNAL	I/O	FUNCTION	ACTIVE	PAD#	SIGNAL	I/O	FUNCTION	ACTIVE
1	A ₁₈	I	Address Bit 18		31	A ₁₉	I	Address Bit 19	
2	A ₁₆	I	Address Bit 16		32	A ₁₇	I	Address Bit 17	
3	A ₁₄	I	Address Bit 14		33	A ₁₅	I	Address Bit 15	
4	V _{ccr}	I	Voltage Refresh	N.C.	34	A ₁₃	I	Address Bit 13	
5	CEH#	I	Card Enable High Byte	Low	35	A ₁₂	I	Address Bit 12	
6	A ₁₁	I	Address Bit 11		36	RESET#	I	Reset	Low
7	A ₉	I	Address Bit 9		37	A ₁₀	I	Address Bit 10	
8	A ₈	I	Address Bit 8		38	VS ₁ #	O	Voltage Sence 1	N.C.
9	A ₆	I	Address Bit 6		39	A ₇	I	Address Bit 7	
10	A ₅	I	Address Bit 5		40	BS8#	I	Bus Size 8	N.C.
11	A ₃	I	Address Bit 3		41	A ₄	I	Address Bit 4	
12	A ₂	I	Address Bit 2		42	CEL#	I	Card Enable Low Byte	Low
13	A ₀	I	Address Bit 0		43	A ₁	I	Address Bit 1	
14	RAS#	I	Row Address Strobe	N.C.	44	CASL#	I	Column Address Strobe Low Byte	N.C.
15	A ₂₄	I	Address Bit 24	N.C.	45	CASH#	I	Column Address Strobe High Byte	N.C.
16	A ₂₃	I	Address Bit 23	N.C.	46	CD#	O	Card Detect	Low
17	A ₂₂	I	Address Bit 22		47	A ₂₁	I	Address Bit 21	
18	OE#	I	Output Enable	Low	48	BUSY#	O	Ready/Busy	Low
19	D ₁₅	I/O	Data Bit 15		49	WE#	I	Write Enable	Low
20	D ₁₃	I/O	Data Bit 13		50	D ₁₄	I/O	Data Bit 14	
21	D ₁₂	I/O	Data Bit 12		51	RFU		Reserved	
22	D ₁₀	I/O	Data Bit 10		52	D ₁₁	I/O	Data Bit 11	
23	D ₉	I/O	Data Bit 9		53	VS ₂ #	O	Voltage Sence 2	N.C.
24	D ₀	I/O	Data Bit 0		54	D ₈	I/O	Data Bit 8	
25	D ₂	I/O	Data Bit 2		55	D ₁	I/O	Data Bit 1	
26	D ₄	I/O	Data Bit 4		56	D ₃	I/O	Data Bit 3	
27	RFU		Reserved		57	D ₅	I/O	Data Bit 5	
28	D ₇	I/O	Data Bit 7		58	D ₆	I/O	Data Bit 6	
29	SDA	I/O	Serial Data and Address	N.C.	59	RFU		Reserved	
30	SCL	I	Serial Clock	N.C.	60	A ₂₀	I	Address Bit 20	

Power/Insertion Signals

SIGNAL NO.	SIGNAL
61	GND
62	CINS#
63	V _{CC}

Interface Signals

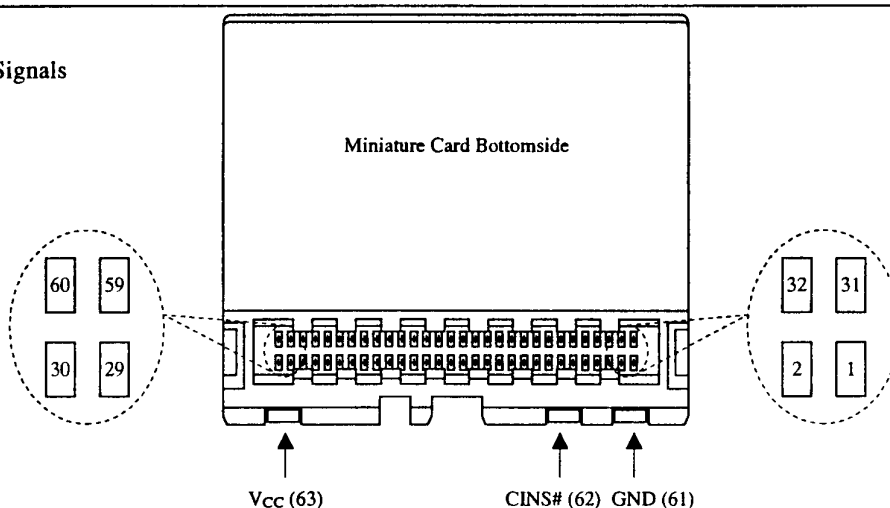


Figure 1. Card Interface Signal Assignment

5. Signal Description

Interface Signal Description

Symbol	Type	Name and Function
A ₀ -A ₂₄	INPUT	ADDRESS INPUTS: Addresses A ₀ through A ₂₄ enable direct addressing of up to 64 MB of memory on the card. The memory will wrap at the card density boundary. The system should NOT try to access memory beyond the card's density, since the upper addresses are not decoded.
D ₀ -D ₁₅	INPUT/OUTPUT	DATA INPUT/OUTPUT: D ₀ through D ₁₅ constitute the bi-directional data bus. D ₁₅ is the most significant bit.
CEL# CEH#	INPUT	CARD ENABLE LOW & HIGH: CEL# enables accesses on the low byte of the data bus D ₀₋₇ . CEH# enables accesses on the high byte of the data bus D ₈₋₁₅ . Both CEL# and CEH# are active low signals. A 16-bit host must always assert both CEL# and CEH#.
OE#	INPUT	OUTPUT ENABLE: Active low signal, enables read data from the Miniature card.
WE#	INPUT	WRITE ENABLE: Active low signal, enables write data to the Miniature card.
BUSY#	OUTPUT	BUSY: Active low signal, indicates the status of internally timed erase or write activities. A high output indicates the Miniature card is ready to accept another command
CD#	OUTPUT	CARD DETECT: Active low signal, provides for card insertion detection. CD# connects to ground internally on the Miniature card, and will be forced low when the CD# interface signal connects to the host.
RESET#	INPUT	RESET: Active low input signal, resets the device's command user interface and places the card into a deep power-down mode. The host must drive this signal.
VS ₁ # VS ₂ #	OUTPUT	VOLTAGE SENSE: Notifies the host socket of the card's V _{CC} requirements. Both VS ₁ # and VS ₂ # are left open to indicate a 5.0V capable card has been inserted.
RFU	—	RESERVED FOR FUTURE USE

Power/Insertion Signal Description

Symbol	Type	Name and Function
CINS#	OUTPUT	CARD INSERTION DETECT: This signal provides for early card insertion detection. CINS# connects to ground internally on the Miniature card, and will be forced low when the power/insertion signals connect to the host.
V _{CC}	—	CARD POWER SUPPLY: 5.0V
GND	—	GROUND

6. LH28F320S5B Control Logic

6. 1 Bus Operations

The host executes read, write and erase operations by issuing the appropriate command to the flash device's Command User Interface (CUI). The CUI serves as the interface between the host processor and internal operation of the flash device. These commands can be issued to the CUI using standard microprocessor bus cycles.

6. 1. 1 Read Array

The host enables reads from the card by writing the appropriate read command to the CUI. The LH28F320S5B automatically resets to read array mode upon initial device power-up, or after reset. CEL#, CEH#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enables (CEL# and CEH#) are used to select the addressed devices. Output Enable (OE#) is the data input/output (D₀–D₁₅) direction control, and when active, drives data from the selected memory onto the data bus. WE# and RESET# must be driven to V_{IH} during a read access.

6. 1. 2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D₀–D₁₅) are placed in a high-impedance state.

6. 1. 3 Standby

CEL# and CEH# at a logic-high level (V_{IH}) places the card in standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D₀–D₁₅) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

6. 1. 4 Deep Power-Down

RESET# at V_{IL} initiates the deep power-down mode.

During reads, an active RESET# deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RESET# must be held low for a minimum of 100 ns. After returning from deep power-down, the host must wait before initial memory access outputs are valid, as determined by t_{PHQV}. After this wake-up interval, the host can resume normal operations to the card. Card reset forces the CUI to reset to read array mode and sets the status register to 80H.

During block erase, full chip erase, (multi)word/byte write, or lock-bit configuration modes, an active RESET# will abort the operation. BUSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET# goes to logic-High (V_{IH}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET# to the card during a system reset. Automated flash memories provide status information when accessed during block erase, full chip erase, (multi) word/byte write and block-lock-bit configuration. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs. For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data.

Sharp's ID343K01 Series Flash Memory Miniature Card allows proper card reset following a system reset through the use of the RESET# input. System RESET# circuitry can reset the host CPU in addition to the card.

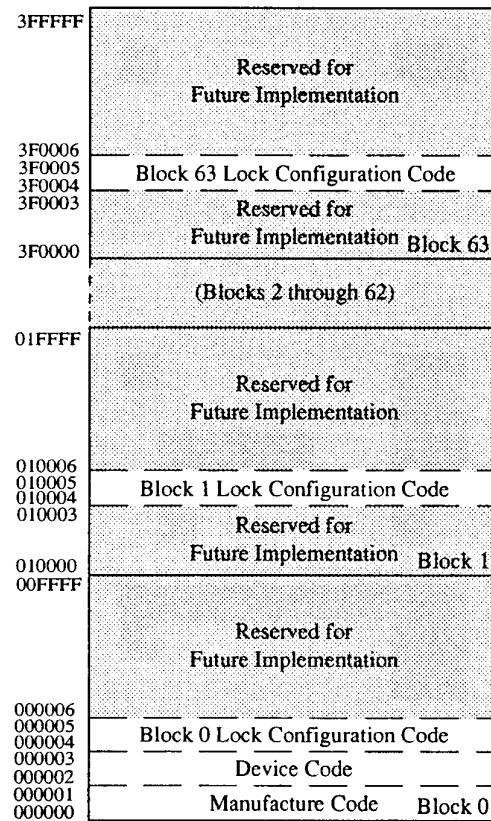


Figure 2. Device Identifier Code Memory Map

6. 1. 5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code (Block 0), device code (Block 0), and block lock configuration codes (for each block), see Figure 2. Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock codes identify locked and unlocked blocks.

6. 1. 6 Query Operation

The query operation outputs the query structure. Query database is stored in the 48byte ROM. Query structure allows system software to gain critical information for controlling the flash component.

6. 1. 7 CUI Writes

Writes to the CUI enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command, address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Write Setup command requires both appropriate command data and the address of the location to be written, while the Write command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CEL#,CEH# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

When a write or erase command has been issued to the CUI, the internal Write State Machine (WSM) becomes busy and will not be ready until it has completed the operation.

7. Card Control Logic

7.1 Word Addressing

Sharp's ID343K01 Series Flash Memory Miniature Card uses two $\times 8$ devices in parallel to form the Miniature card $\times 16$ data bus. If the host writes a command to the card, it must make sure that it writes the command to both devices in the card. For example, a component write command is 40H, so a card write command must be 4040H. This same procedure must be followed when reading from the status register. A component status register is only 8 bits and may return 80H when read. However, the card status register is 16 bits and may return 8080H.

7.2 Decode Logic

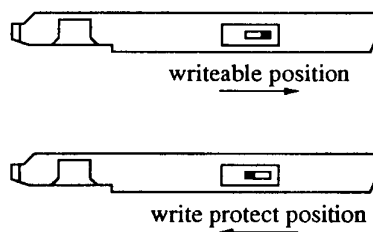
The decode logic enables the appropriate component device pair during a read or write access. Unused upper addresses for the ID343K01 Series Flash Memory Miniature Card will not be decoded. The address decoding will wrap around at the card's density.

7.3 Write Protect Switch

The ID343K01 Series Flash Memory Miniature Card has a write protect switch on the side of the card. When the switch is in the write protect position, the card blocks all writes to the card (see Figure 3).

NOTE

When the write protect switch is in the write protect position, all writes are disabled to the flash array including all commands to the CUI.



NOTE:

The write protect switch is represented by the solid black rectangle.

Figure 3. Write Protect Switch

7. 4 Data Control

As shown in Table 1, data paths and directions are selected by the Data Control logic using WE#, OE#, CEL#, and CEH#, as logic inputs.

NOTE:

This card has a $\times 16$ interface. The High byte CANNOT be accessed on the lower data path (D₀₋₇).

Mode	RESET#	CEH#	CEL#	OE#	WE#	A ₀	D ₈₋₁₅	D ₀₋₇	Notes
Low Byte-Read	V _{IH}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	\times	High-Z	Low ⁽⁶⁾	1.2.3
High Byte-Read	V _{IH}	V _{IL}	V _{IH}	V _{IL}	V _{IH}	\times	High ⁽⁶⁾	High-Z	1.2.3
Word-Read	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	\times	High ⁽⁶⁾	Low ⁽⁶⁾	1.2.3
Low Byte-Write	V _{IH}	V _{IH}	V _{IL}	V _{IH}	V _{IL}	\times	$\times \times \times$	Low ⁽⁶⁾	3.4
High Byte-Write	V _{IH}	V _{IL}	V _{IH}	V _{IH}	V _{IL}	\times	High ⁽⁶⁾	$\times \times \times$	3.4
Word-Write	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	\times	High ⁽⁶⁾	Low ⁽⁶⁾	3.4
Manufacturer ID	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	B0H	B0H	—
Device ID	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	V _{IH}	D4H	D4H	5
Query	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	See Table 5~9	Note 7	Note 7	—
Standby	V _{IH}	V _{IH}	V _{IH}	\times	\times	\times	High-Z	High-Z	—
Output Disable	V _{IH}	\times	\times	V _{IH}	V _{IH}	\times	High-Z	High-Z	—
Power-Down	V _{IL}	\times	\times	\times	\times	\times	High-Z	High-Z	—

Table 1. Function Table

NOTES:

1. Refer to DC Characteristics.
2. \times can be V_{IL} or V_{IH} for control pins and address.
3. BUSY# is V_{OL} when the WSM is executing internal byte write or block erase algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode, or deep power-down mode.
4. Refer to Table 2 for valid D_{IN} during a write operation.
5. Although the device code is D4H, other Sharp's Flash Memory Miniature Card could also have device codes AAH, A6H or A7H. Software should check for all four cases for compatibility with future cards.
6. High indicates high byte data, Low indicates low byte data.
7. See section 8.5 for query data.

8. Command Definitions

Device operations are selected by writing specific commands into the Command User Interface. Table 2 defines the LH28F320S5B commands.

NOTE:

When the write protect switch is in the write protect position, all writes are disabled to the flash array including commands to the CUI.

Table 2. Command Definitions ⁽⁷⁾

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾	Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾
Read Array/Reset	1	—	Write	×	FFFFH	—	—	—
Read Identifier Codes	≥2	4	Write	×	9090H	Read	IA	ID
Query	≥2	—	Write	×	9898H	Read	QA	QD
Read Status Register	2	—	Write	×	7070H	Read	×	SRD
Clear Status Register	1	—	Write	×	5050H	—	—	—
Block Erase Setup / Confirm	2		Write	BA	2020H	Write	BA	D0D0H
Full Chip Erase Setup / Confirm	2		Write	×	3030H	Write	×	D0D0H
Word / Byte Write Setup / Write	2	5	Write	WA	4040H or 1010H	Write	WA	WD
Multi Word / Byte Write Setup / Confirm	≥4	6	Write	WA	E8E8H	Write	WA	N-1
Block Erase and (Multi) Word/byte Write Suspend	1		Write	×	B0B0H	—		—
Confirm and Block Erase and (Multi)Word/byte Write Resume	1		Write	×	D0D0H	—		—

NOTES:

1. BUS operations are defined in Table 1.
2. x = Any valid address within the device.
IA = Identifier Code Address: see Figure 2.
QA = Query Offset Address.
BA = Address within the block being erased or locked.
WA = Address of memory location to be written.
3. SRD = Data read from status register. See Table 10 for a description of the status register bits.
WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (Whichever goes high first).
ID = Data read from identifier codes.
QD = Data read from query database.
4. Following the Read Identifier Codes command, read operations access manufacturer, device and block status codes. See Section 8.2 for read identifier code data.
5. Either 40H or 10H are recognized by the WSM as the byte write setup.
6. Following the Third Bus Cycle, inputs the write address and write data of 'N' times. Finally, input the confirm command 'D0D0H'.
7. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.


8.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the card defaults to read array mode. The host can also read by writing the Read Array command. The device remains enabled for reads until the host writes another valid command. Once the internal WSM has started a block erase, full chip erase or (multi) word/byte write, the device will not recognize the Read Array command until the WSM completes its operation. However, the host can suspend the WSM using an Erase Suspend or Word Write Suspend command. RESET# must be V_{IH} .

8.2 Read Identifier Codes Command

The host initiates the identifier code operation by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 2 retrieve the manufacturer, device and block lock configuration codes (see Table 3 for identifier code data). To terminate the operation, write another valid command. Although Table 3 lists the device code as D4D4, other Sharp's Flash Memory Miniature Card could also have device codes AAAA, A6A6 or A7A7. Host software should check for all four cases for compatibility with future cards.

Table 3. Identifier Codes

Code	Address	Data
Manufacture Code	00000	B0B0
	00001	
Device Code	00002	D4D4
	00003	
Block Status Code	$\times 0004^{(1)}$	
	$\times 0005^{(1)}$	
• Block is Unlocked		
• Block is Locked (3)		
• Last erase operation completed successfully		
• Last erase operation did not completed successfully		
• Reserved for Future Use		D ₂₋₇ , D ₁₀₋₁₅

NOTES:

1. \times selects the specific block status code to be read. See Figure 2 for the device identifier code memory map.
2. The addresses listed are word addresses and store 16 bits of data.
3. This card is can not lock bit configuration.

8.3 Read Status Register Command

The LH28F320S5B components on the ID343K01 Series Flash Memory Miniature Card each contain a Status Register which may be read to determine when a (multi) word/byte write, block erase or full chip erase is complete, and whether that operation completed successfully (see Table 10). The host may read the Status Register at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the Status Register, until the host writes another valid command to the CUI. The flash components latch the contents of the Status Register on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must be toggled to V_{IH} before further reads to update the Status Register latch. RESET# must be V_{IH} .

NOTE:

The ID343K01 Series Flash Memory Miniature Card arranges two LH28F320S5B devices in parallel to from a $\times 16$ bus. Both status registers need to be checked when determining the status of a $\times 16$ erase/write operation.

8.4 Clear Status Register Command

The WSM sets the Erase Status and Write Status bits to "1"s and they can only be reset by the Clear Status Register command. These bits indicate various failure conditions(see Table 10). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence.

The WSM sets these bits to "1" when a write or erase operation has failed. The host can issue additional write and erase commands to the CUI without clearing the status register. This allows a system to write a sequence of bytes before checking the write status bit. However, if an error has occurred the system will not know which write in the sequence has failed. To clear the Status Register, the Clear Status Register command (5050H) is written to the CUI.

RESET# must be V_{IH} . This command is not functional during block erase, full chip erase, (multi) word/byte write, block erase suspend or (multi) word/byte write suspend modes.

8.5 Query Command

Query database can be read by writing Query command (98H). Following the command write, read cycle from address shown in Table 5~ 8 retrieve the critical information to write, erase and otherwise control the flash component. A_0 of query offset address is ignored. RESET# must be V_{IH} .

Table 4. Example of Query Output

Mode	Offset Address	Output	
		DQ15~8	DQ7~0
$\times 16$ Mode	$A_5, A_4, A_3, A_2, A_1, A_0$		
	1, 0, 0, 0, 0, 0 (20H)	"Q"	"Q"
	1, 0, 0, 0, 0, 1 (21H)	"Q"	"Q"
	1, 0, 0, 0, 1, 0 (22H)	"R"	"R"
	1, 0, 0, 0, 1, 1 (23H)	"R"	"R"

8. 5. 1 Block Status Register

This field provides lock configuration and erase status for the specified block. These informations are only available when device is ready (SR.7=1). If block erase or full chip erase operation is finished irregularly, block erase status bit will be set to "1". If bit 1 is "1", this block is invalid. This card is not support Block lock configuration.

Table 5. Query Block Status Register

Offset (Word Address)	Length	Description
(BA+2)H	01H	Block Status Register bit0 Block Lock Configuration 0 = Block is unlocked 1 = Block is Locked bit1 Block Erase Status 0 = Last erase operation completed successfully 1 = Last erase operation not completed successfully bit2-7 reserved for future use

Note:

1. BA = The beginning of a Block Address.

8. 5. 2 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the spec and which Vendor-specified command set(s) is (are) supported.

Table 6. CFI Query Identification String

Offset (Word Address)	Length	Description
10H, 11H, 12H	03H	Query Unique ASCII string "QRY" 51H, 52H, 59H
13H, 14H	02H	Primary Vendor Command Set and Control Interface ID Code 01H, 00H (SCS ID Code)
15H, 16H	02H	Address for Primary Algorithm Extended Query Table 31H, 00H (SCS Extended Query Table Offset)
17H, 18H	02H	Alternate Vendor Command Set and Control Interface ID Code 0000H (0000H means that no alternate exists)
19H, 1AH	02H	Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists)

8.5.3 System Interface Information

The following device information can be useful in optimizing system interface software.

Table 7. System Information String

Offset (Word Address)	Length	Description
1BH	01H	V _{CC} Logic Supply Minimum Write/Erase voltage 45H (4.5V)
1CH	01H	V _{CC} Logic Supply Maximum Write/Erase voltage 55H (5.5V)
1DH	01H	V _{PP} Programming Supply Minimum Write/Erase voltage 45H (4.5V)
1EH	01H	V _{PP} Programming Supply Maximum Write/Erase voltage 55H (5.5V)
1FH	01H	Typical Timeout per Single Byte/Word Write 04H ($2^4 = 16 \mu\text{s}$), $2^N \mu\text{s}$
20H	01H	Typical Timeout for Maximum Size Buffer Write (32 Bytes) 06H ($2^6 = 64 \mu\text{s}$)
21H	01H	Typical Timeout per Individual Block Erase 09H (09H = 9, $2^9 = 512\text{ms}$)
22H	01H	Typical Timeout for Full Chip Erase 0FH (0FH = 15, $2^{15} = 32768\text{ms}$)
23H	01H	Maximum Timeout per Single Byte/Word Write, 2^N times of typical. 04H ($2^4 = 16, 16 \mu\text{s} \times 16 = 256 \mu\text{s}$)
24H	01H	Maximum Timeout Maximum Size Buffer Write, 2^N times of typical. 04H ($2^4 = 16, 64 \mu\text{s} \times 16 = 1024 \mu\text{s}$)
25H	01H	Maximum Timeout per Individual Block Erase, 2^N times of typical. 04H ($2^4 = 16, 1024\text{ms} \times 16 = 16384\text{ms}$)
26H	01H	Maximum Timeout For Full Chip Erase, 2^N times of typical. 04H ($2^4 = 16, 32768\text{ms} \times 16 = 524288\text{ms}$)

8.5.4 Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 8. Device Geometry Definition

Offset (Word Address)	Length	Description
27H	01H	Device Size 16H (16H = 22, $2^{22} = 4194304 = 4\text{M Bytes}$)
28H, 29H	02H	Flash Device Interface description 02H, 00H ($\times 8/\times 16$ supports $\times 8$ and $\times 16$ via BYTE#)
2AH, 2BH	02H	Maximum Number of Bytes in Multi-byte 05H, 00H ($2^5 = 32 \text{ Bytes}$)
2CH	02H	Number of Erase Block Regions within device 01H (symmetrically blocked)
2DH, 2EH	02H	The Number of Erase Blocks 3FH, 00H (3FH = 63 ==> $63 + 1 = 64 \text{ Blocks}$)
2FH, 30H	02H	The Number of "256 Bytes" cluster in a Erase block 00H, 01H (0100H = 256 ==> $256 \text{ Bytes} \times 256 = 64\text{K Bytes in a Erase Block}$)

8. 5. 5 SCS OEM Specific Extended Query Table

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific Query table(s) may be used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

Table 9. SCS OEM Specific Extended Query Table

Offset (Word Address)	Length	Description
31H, 32H, 33H	03H	PRI 50H, 52H, 49H
34H	01H	31H (1) Major Version Number, ASCII
35H	01H	30H (0) Minor Version Number, ASCII
36H, 37H, 38H, 39H	04H	0FH, 00H, 00H, 00H Optional Command Support bit0 = 1 : Chip Erase Supported bit1 = 1 : Suspend Erase Supported bit2 = 1 : Suspend Write Supported bit3 = 1 : Lock/Unlock Supported bit4 = 0 : Queued Erase Not Supported bit5-31 = 0 : reserved for future use
3AH	01H	01H Supported Functions after Suspend bit0 = 1 : Write Supported after Erase Suspend bit1-7 = 0 : reserved for future use
3BH, 3CH	02H	03H, 00H Block Status Register Mask bit0 = 1 : Block Status Register Lock Bit [BSR.0] active bit1 = 0 : Block Status Register Valid Bit [BSR.1] active bit2-15 = 0 : reserved for future use
3DH	01H	V _{CC} Logic Supply Optimum Write/Erase voltage (highest performance) 50H (5.0V)
3EH	01H	V _{PP} Programming Supply Optimum Write/Erase voltage (highest performance) 50H (5.0V)
3FH	reserved	Reserved for future versions of the SCS Specification

8. 6 Block Erase Command

The host executes an erase command one block at a time using a two-cycle command. The host writes a block erase setup command first, followed by a block erase confirm command. These two commands require appropriate sequencing and an address within the block to complete (erase changes all block data to FFH). The WSM handles block preconditioning, erase, and verify internally (invisible to the system). After the host writes the two-cycle block erase sequence, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output data of the BUSY# signal or status register bit SR.7.

When the block erase completes, status register bit SR.5 should be checked. If a block erase error is detected, the host should clear the status register before system software attempts corrective actions. The CUI remains in read status register mode until the host issues a new command.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1".

8. 7 Full Chip Erase Command

This command followed by a confirm command(D0D0H) erases all of the unlocked blocks. A full chip erase setup is first written, followed by a full chip erase confirm. After a confirm command is written, device erases the all unlocked blocks from Block 0 to Block 31 block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM(invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read. The CPU can detect full chip erase completion by analyzing the output data of the BUSY# pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Reading the block valid status by issuing Read ID Codes command or Query command informs which blocks failed to its erase.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1".

8. 8 Word/Byte Write Command

The host executes a word/byte write by a two-cycle command sequence. The host writes word/byte write setup (standard 4040H or alternate 1010H) first, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the host writes the word/byte write sequence, the device automatically output status register data when read. The CPU can detect the completion of the word/byte write event by analyzing the BUSY# pin or status register bit SR.7.

When the WSM completes the word/byte writes, the host should check status register bit SR.4. If the host detects a write error, it should clear the status register. The internal WSM verify only detects errors for "1"s that do not successfully writes to "0"s. The CUI remains in read status register mode until it receives another command.

8. 9 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes can be loaded into the buffer and written to Flash Array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the device automatically outputs extended status register data (XSR) when read. If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry, continue monitoring XSR.7 by writing multi word/byte write setup with write address until XSR.7 transitions to 1. When XSR.7 transitions to 1, the device is ready for loading the data to the buffer. A word/byte count (N)-1 is written with write address. After writing a word/byte count (N)-1 must be less than or equal to 1FH. On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the Flash Array. An invalid Multi Word/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH320S5B has two buffers. If an error occurs while writing, the device will stop writing and flash next multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command is available if either SR.4 or SR.5 are set to "1". SR.4 and SR.5 should be cleared before issuing multi word/byte write command. If a multi word/byte write command is attempted past an erase block boundary, the device will write the data to Flash Array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

8. 10 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. After the host writes the Block Erase Suspend command, the host should then write the Read Status Register command. Polling status register bits SR.7 and SR.6 can determine when the WSM suspends the block erase operation (both will be set to "1"). BUSY# will also transition to V_{OH} . Specification t_{WHRH2} defines the block erase suspend latency. It is also possible that the block erase completes before the device has an opportunity to suspend. The host should also check for this condition.

After the block erase has been suspended, the host can issue a read array command or a word write command to any block except the one that has been suspended. Using the Word Write Suspend command (see Section 8.11), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the BUSY# output will transition to V_{OL} . However, SR.6 will remain "1" to indicate block erase suspend status. The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After the host writes a Block Erase Resume command to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and BUSY# will return to V_{OL} . After the host writes the Erase Resume command, the device automatically outputs status register data when read. Block erase cannot resume until word write operation initiated during block erase suspend have completed.

8. 11 (Multi)Word/Byte Write Suspend Command

The (Multi)Word/Byte Write Suspend command allows (multi)word/byte write interruption to read data in other flash memory locations. Once the (multi)word/byte write process starts, writing the (Multi)Word/Byte Write Suspend command requests that the WSM suspend the (multi)word/byte write sequence at a predetermined point in the algorithm. After the host writes the (Multi)Word/Byte Write Suspend command, it should write the Read Status Register command. Polling status register bits SR.7 and SR.2 can determine when the WSM suspends the (multi)word/byte write operation (both will be set to "1"). BUSY# will also transition to V_{OH} . Specification t_{WHRH1} defines the (multi)word/byte write suspend latency. It is also possible that the (multi)word/byte write completes before the device has an opportunity to suspend. The host should also check for this condition.

After the (multi)word/byte write has been suspended, the host can write the Read Array command to read data from any location except the suspended location. The only other valid commands while (multi)word/byte write is suspended are Read Status Register and (Multi)Word/Byte Write Resume. After the host writes a (Multi)Word/Byte Write Resume to the CUI, the WSM will continue the (multi)word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and BUSY# will return to V_{OL} . After the host writes the (Multi)Word/Byte Write Resume command, the device automatically outputs status register data when read.

8.12 Status Register

The memory devices in this card have Status Register which shows state of the device.

Byte Access × 8 Bits

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0
WSMS	BESS	ECBLBS	WSBLBS	VPPS	WSS	DPS	R

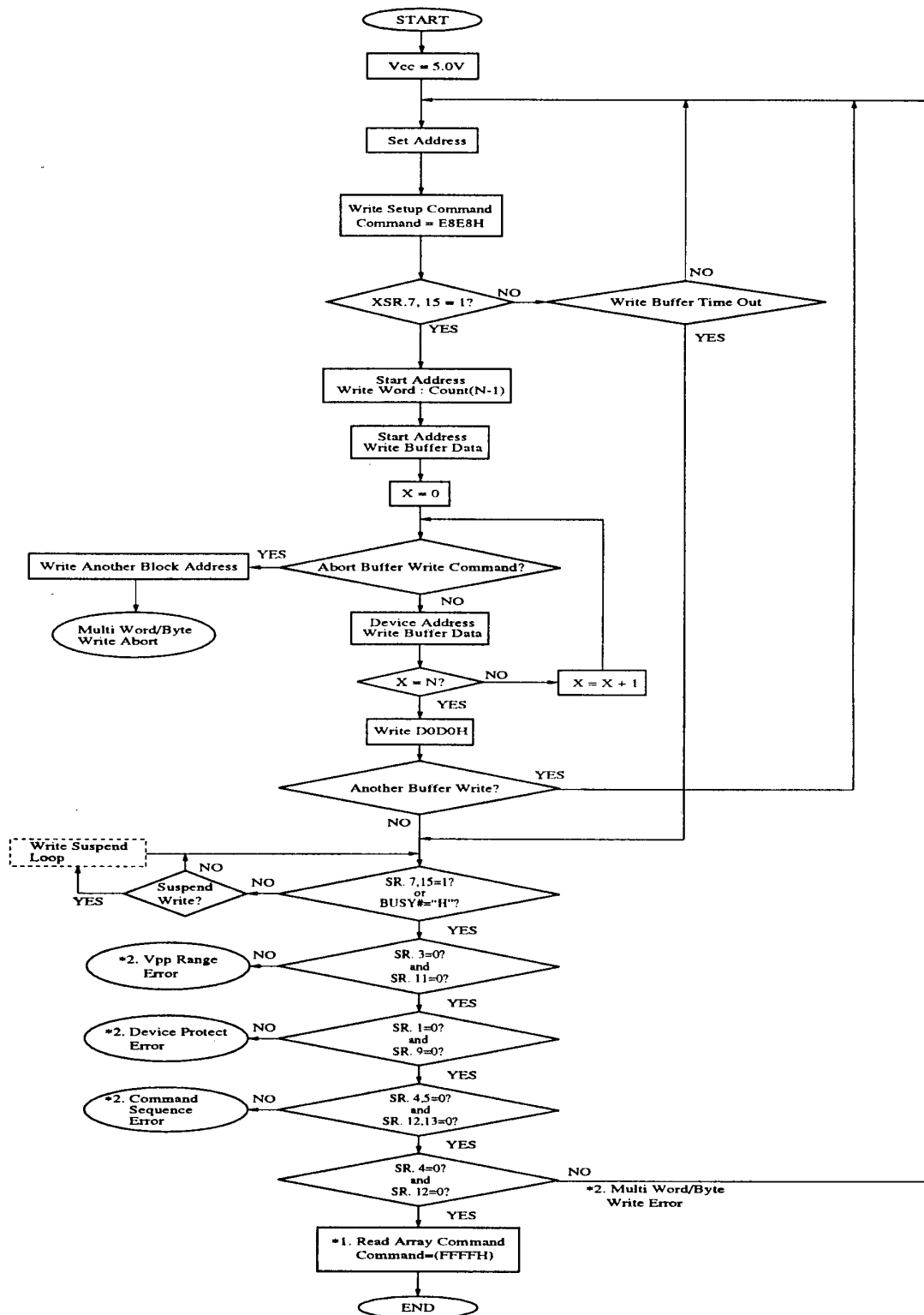
Table 10. Status Register Definition

<p>SR. 7 = WRITE STATE MACHINE STATUS</p> <p>1 = Ready</p> <p>0 = Busy</p> <p>SR. 6 = BLOCK ERASE SUSPEND STATUS</p> <p>1 = Block Erase Suspended</p> <p>0 = Block Erase in Progress/Completed</p> <p>SR. 5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS</p> <p>1 = Error in Erase or Clear Block Lock-Bits</p> <p>0 = Successful Erase or Clear Block Lock-Bits</p> <p>SR. 4 = WRITE AND SET BLOCK-BIT STATUS</p> <p>1 = Error in Write or Set Block Lock-Bit</p> <p>0 = Successful Write or Set Block Lock-Bit</p> <p>SR. 3 = V_{PP} STATUS</p> <p>1 = V_{PP} Low Detect, Operation Abort</p> <p>0 = V_{PP} OK</p> <p>SR. 2 = WRITE SUSPEND STATUS</p> <p>1 = Write Suspended</p> <p>0 = Write in Progress/Completed</p> <p>SR. 1 = DEVICE PROTECT STATUS</p> <p>1 = Block Lock-Bit and/or WP# Lock Detected, Operation Abort</p> <p>0 = Unlock</p>	<p>SR. 0 = RESERVED FOR FUTURE ENHANCEMENTS</p> <p>NOTES:</p> <p>Check SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when V_{PP} 5V±5%</p> <p>SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bit, and WP# only after Block Erase, full chip erase, (multi) Word/Byte Write, or Block Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or WP# is not V_{IH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p>
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Word Access × 16 Bits

***2.If error is detected, clear the Status Register before attempting retry or other error recovery.**

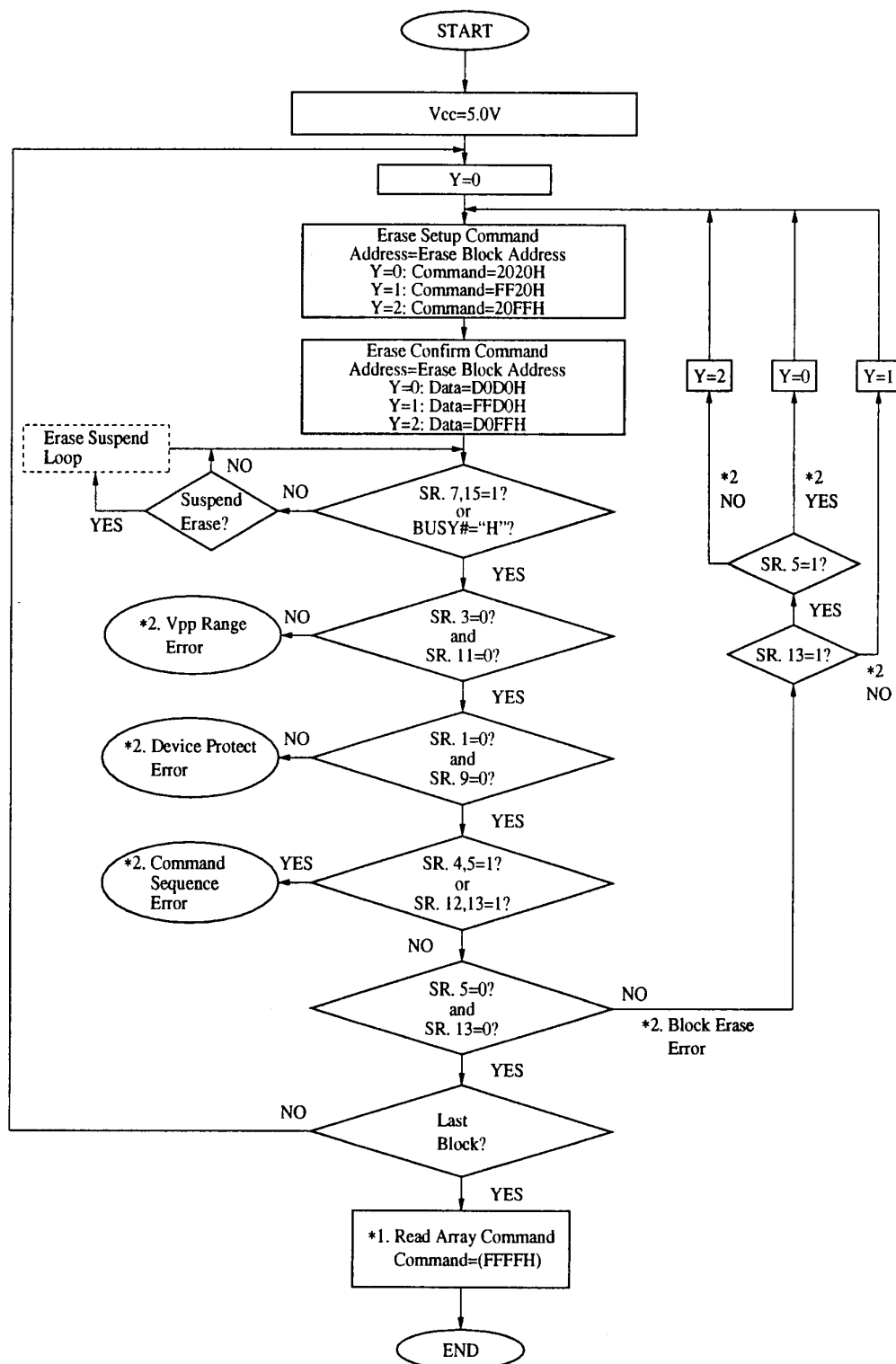
8.14 Multi Word/Byte Write Flowchart



Note) *1. Write FFH after the last word write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

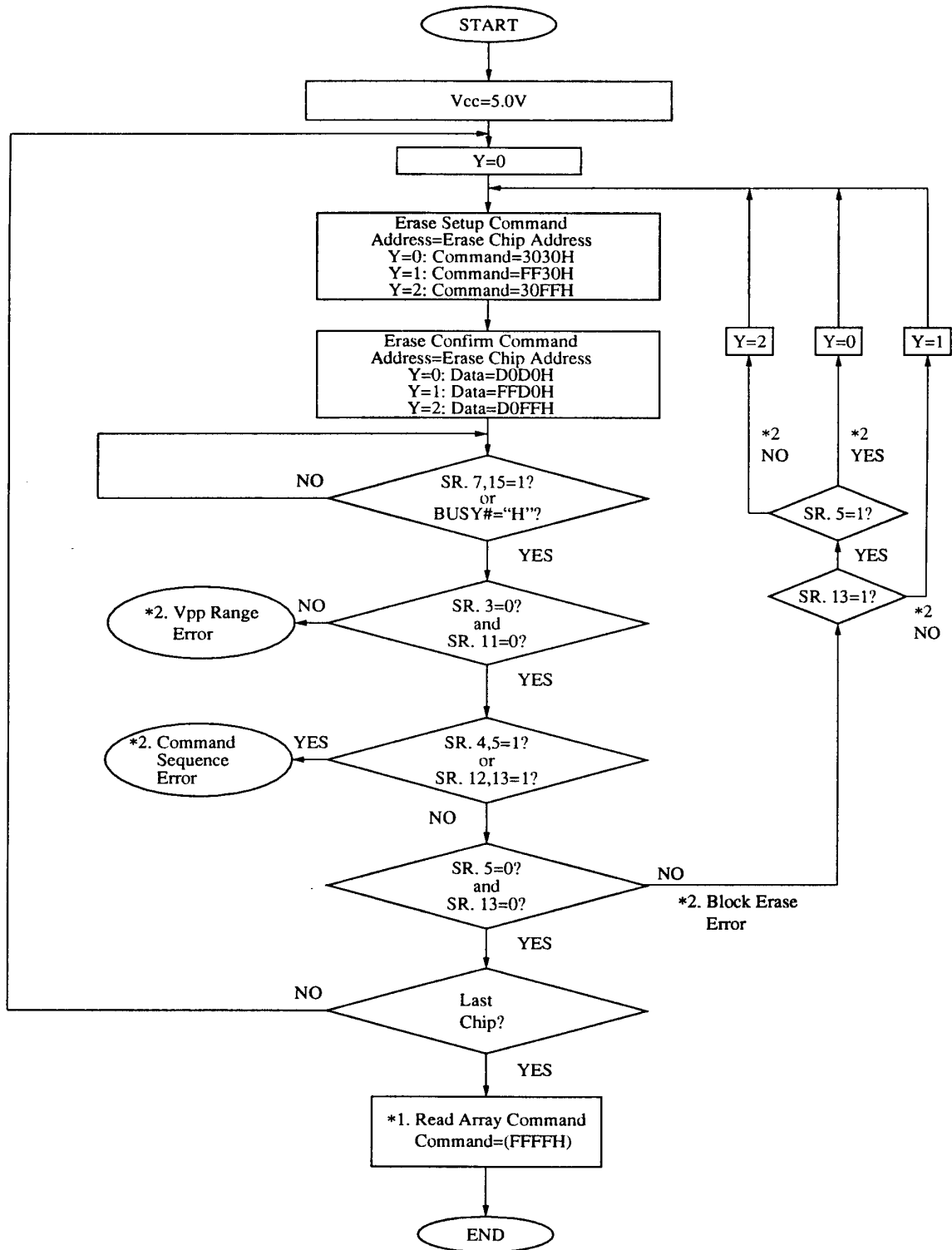
8.15 Automated Block Erase Flowchart



(Note)*1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

8.16 Automated Full Chip Erase Flowchart



Note) *1. Write FFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

9. Electrical Specifications

9.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage ⁽²⁾	V _{CC}	-0.2 to 7.0	V
Input Voltage ⁽²⁾	V _{IN}	-0.5 to V _{CC} + 0.5 (Max: 7.0)	V
Output Short Circuit Current ⁽³⁾	I _{OUT}	100	mA
Operating Temperature ⁽¹⁾	T _{OPR}	0 to 60	°C
Storage Temperature	T _{STG}	-30 to 70	°C

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND.
3. Output shorted for no more than one second. No more than one output shorted at a time.

9.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MINIMUM	MAXMUM	UNIT
Operating Temperature	T _{OPR}	0	60	°C
Supply Voltage	V _{CC}	4.75	5.25	V

9.3 Capacitance

T_a = 25°C, f = 1MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C _{IN}	—	28	40	pF	V _{IN} = 0.0V
Input/Output Capacitance	C _{IO}	—	18	24	pF	V _{OUT} = 0.0V

9.4 AC Input/Output Test Conditions

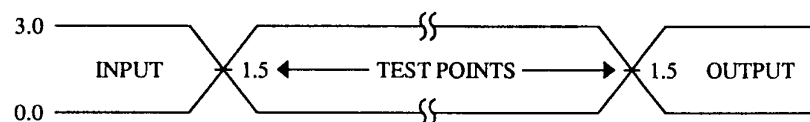


Figure 4. Transient Input/Output Reference Waveform for V_{CC} = 5.0V ± 5%
(Standard Testing Configuration)

AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10ns.

10. DC Characteristics

(Ta = 0~60°C)

PARAMETER	SYMBOL	NOTES	V _{CC} = 5.0V		UNIT	TEST CONDITIONS
			MIN	MAX		
Input Leakage Current (A0–A21)	I _{LI1}	1	—	±5	μ A	V _{CC} = V _{CC} Max, V _{IN} = V _{CC} or GND
Input Leakage Current (A22)	I _{LI2}	1	–2	58	μ A	V _{CC} = V _{CC} Max, V _{IN} = V _{CC} or GND
Input Leakage Current (CEL#,CEH#,RESET#)	I _{LI3}	1	–57	1	μ A	V _{CC} = V _{CC} Max, V _{IN} = V _{CC} or GND
Input Leakage Current (OE#,WE#)	I _{LI4}	1	–60	4	μ A	V _{CC} = V _{CC} Max, V _{IN} = V _{CC} or GND
Output Leakage Current (D0–D15)	I _{LO}	1	—	±20	μ A	V _{CC} = V _{CC} Max, V _{IN} = V _{CC} or GND
V _{CC} Standby Current	I _{CCS}	1, 3	—	550	μ A	V _{CC} = V _{CC} Max, CEL#,CEH# = V _{CC} ± 0.2V, RESET# = V _{CC} ± 0.2V
V _{CC} Deep Power-Down Current	I _{CCD}	1, 3	—	190	μ A	RESET# = GND ± 0.2V, I _{OUT} (BUSY#)=0 mA
V _{CC} Read Current	I _{CCR}	1, 3, 4, 5	—	126	mA	V _{CC} = V _{CC} Max, CEL#,CEH#= GND±0.2V, t _{cycle} = 100ns, I _{OUT} = 0 mA
V _{CC} Word Write Current	I _{CCW}	1, 5	—	236	mA	
V _{CC} Block Erase Current	I _{CCB}	1, 5	—	146	mA	
V _{CC} Word Write or Block Erase Suspend Current	I _{CCWS} I _{CCES}	1, 2, 5	—	26	mA	CEL# = CEH# = V _{IH}

PARAMETER	SYMBOL	NOTES	V _{CC} = 5.0V		UNIT	TEST CONDITIONS
			MIN	MAX		
Input Low Voltage	V _{IL}	—	–0.5	0.8	V	
Input High Voltage	V _{IH}	—	0.7 V _{CC}	V _{CC} +0.5	V	
Output Low Voltage	V _{OL}	—	—	0.1V _{CC}	V	V _{CC} = V _{CC} Min, I _{OL} = 5.8mA
Output High Voltage	V _{OH}	—	0.9V _{CC}	—	V	V _{CC} = V _{CC} Min I _{OH} = –100μA
V _{CC} Lockout Voltage	V _{LKO}	—	2.0	—	V	

NOTES:

1. All currents are in RMS unless otherwise noted.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V.
4. Automatic Power Savings (APS) reduces typical I_{CCR} to 1mA at 5V V_{CC} in static operation (addresses not switching).
5. All values are based on word accesses. Values for byte accesses are 50% of the specification listed.

11. AC Characteristics (Ta = 0~60°C)

Testing Conditions :

- 1) Input Pulse Level : 0.0V~3.0V
- 2) Input Rise/Fall Time : 10ns
- 3) Input/Output Timing Reference Level : 1.5V
- 4) Output Load : 30pF (including scope and jig capacitance)

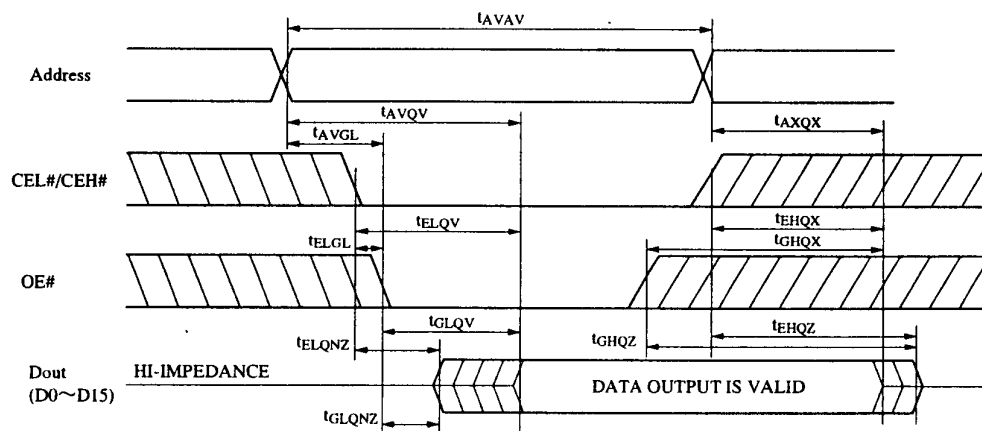
11.1 Read Operations

(Ta = 0 ~ 60°C)

PARAMETER	SYMBOL	V _{CC} = 5.0V		UNIT
	IEEE	MIN	MAX	
Read Cycle Time	t _{AVAV}	100	—	ns
Address Access Time	t _{AVQV}	—	100	
Card Enable Access Time	t _{ELQV}	—	100	
Output Enable Access Time	t _{GLQV}	—	40	
Output Disable Time from CEL#/CEH#*	t _{EHQZ}	—	10	
Output Disable Time from OE#*	t _{GHQZ}	—	10	
Output Enable Time from CEL#/CEH#	t _{ELQNZ}	5	—	
Output Enable Time from OE#	t _{GLQNZ}	5	—	
Data Hold from Address	t _{AXQX}	0	—	
Data Hold from CEL#/CEH#	t _{EHQX}	0	—	
Data Hold from OE#	t _{GHQX}	0	—	
CE# Setup Time to OE# Active	t _{ELGL}	0	—	
Address Setup Time to OE# Active	t _{AVGL}	0	—	
Power-Down Recovery to Output Delay	t _{PHQV}	—	400	

* Time until output becomes floating. (The output voltage is not defined.)

11.2 AC Waveforms for Read Operations



- Note) 1. WE# = "HIGH", during a read cycle.
 2. Either "HIGH" or "LOW" in diagonal areas.
 3. The output data becomes valid when last interval, t_{AXQV}, t_{ELQV} or t_{GLQV} have concluded.

11.3 Write Operations

11.3.1 WE# Controlled Write Operations

(Ta = 0~60°C)

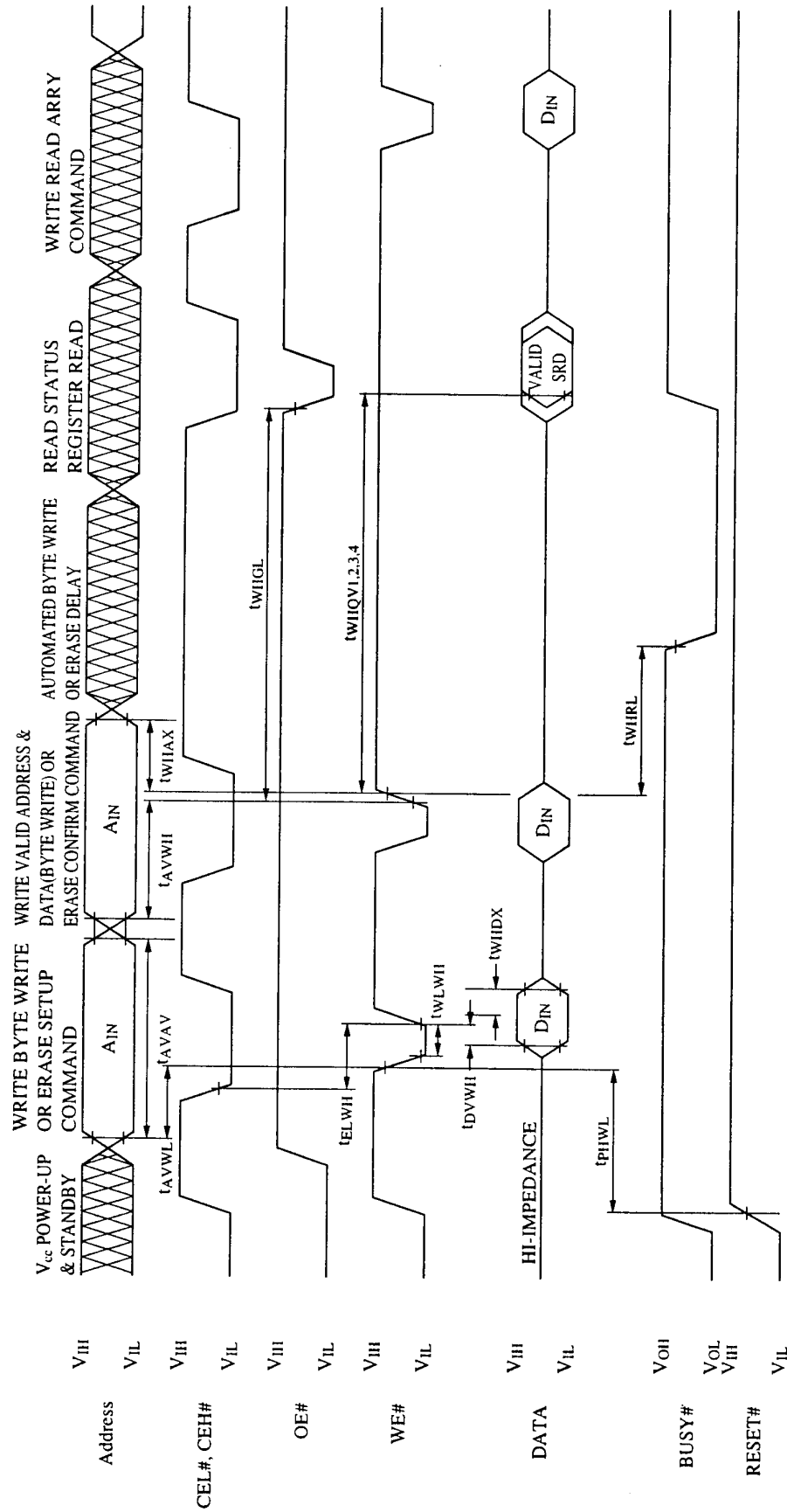
PARAMETER	SYMBOL	V _{CC} = 5.0V		UNIT
	IEEE	MIN	MAX	
Write Cycle Time	t _{AVAV}	100	—	ns
Address Setup Time	t _{AVWL}	10	—	
Write Recovery Time	t _{WHAX}	5	—	
Data Setup Time for WE#	t _{DVWH}	40	—	
Data Hold Time	t _{WHDX}	15	—	
Output Enable Hold from WE#	t _{WHGL}	10	—	
Card Enable Setup time for WE#	t _{ELWH}	70	—	
Address Setup for WE#	t _{AVWH}	70	—	
Write Pulse Width	t _{WLWH}	60	—	
WE# High to RDY/BSY# Going Low	t _{WHRL}	—	150	
Power-Down Recovery to WE# Going Low	t _{PHWL}	1	—	μs

11.3.2 CE# Controlled Write Operations

(Ta = 0~60°C)

PARAMETER	SYMBOL	V _{CC} = 5.0V		UNIT
	IEEE	MIN	MAX	
Write Cycle Time	t _{AVAV}	10	—	ns
Address Setup Time	t _{AVEL}	10	—	
Write Recovery Time	t _{EHAX}	5	—	
Data Setup Time for CE#	t _{DVEH}	15	—	
Data Hold Time	t _{EHDX}	15	—	
Output Enable Hold from CE#	t _{EHGL}	10	—	
Write Enable Setup time for CE#	t _{WLEH}	70	—	
Address Setup for CE#	t _{AVEH}	70	—	
Card Enable Pulse Width	t _{ELEH}	60	—	
CE# High to RDY/BSY# Going Low	t _{EHRL}	—	150	
Power-Down Recovery to CE# Going Low	t _{PHL}	1	—	μs

11.3.3 AC Waveforms for Write Operations (WE# Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11.4 Erase and Data Write Performance⁽³⁾

(Ta = 0~60°C)

PARAMETER	SYMBOL	NOTES	V _{CC} = 5.0V			UNIT
			MIN	TYP ⁽¹⁾	MAX	
Byte Write Time	t _{WHQV1} t _{EHQV1}	2	—	9.24	TBD	μs
Block Write Time		2	—	0.61	7.5	s
Multi Word/Byte Write Time			—	2	TBD	μs
Block Erase Time	t _{WHQV2} t _{EHQV2}	2	—	0.34	10	s
Full Chip Erase Time			—	21.8	TBD	s
Byte Write Suspend Latency Time to Read	t _{WHRH1} t _{EHRH1}	—	—	5.6	7	μs
Erase Suspend Latency Time to Read	t _{WHRH2} t _{EHRH2}	—	—	9.4	13.1	μs

NOTES:

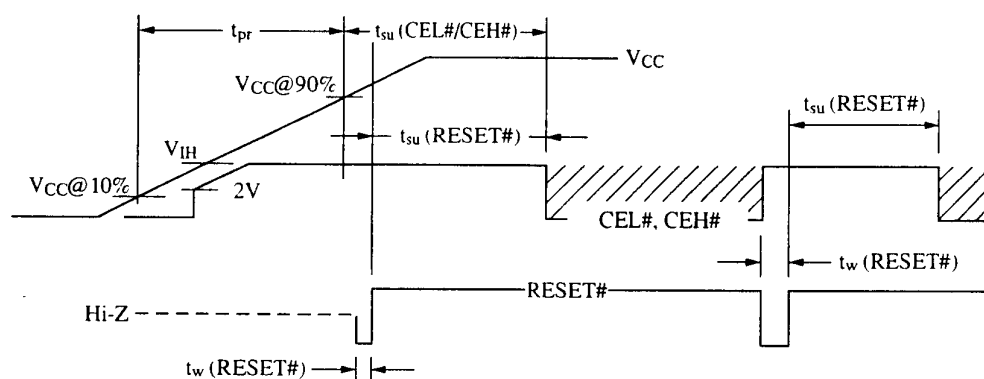
1. Typical values measured at Ta = 25°C and nominal voltages. Assumes corresponding lock-bits are not set.
Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.

11.5 Power-Up

PARAMETER	SYMBOL	NOTES	MIN	MAX	UNITS
CE# Setup Time	$t_{su}(\text{CEL\# / CEH\#})$	—	1	—	ms
RESET# Setup Time	$t_{su}(\text{RESET\#})$	—	1	—	ms
V _{CC} Rising Time	t_{pr}	1	0.1	100	ms
RESET# Width	$t_w(\text{RESET\#})$	—	1	—	μs

NOTES:

1. The t_{pr} is defined as “linear waveform” in the period of 10% to 90%. Even if the waveform is not a “linear waveform,” its rising time must meet this specification.



Power-Up Timing for Systems Supporting RESET#

12. Specification Changes

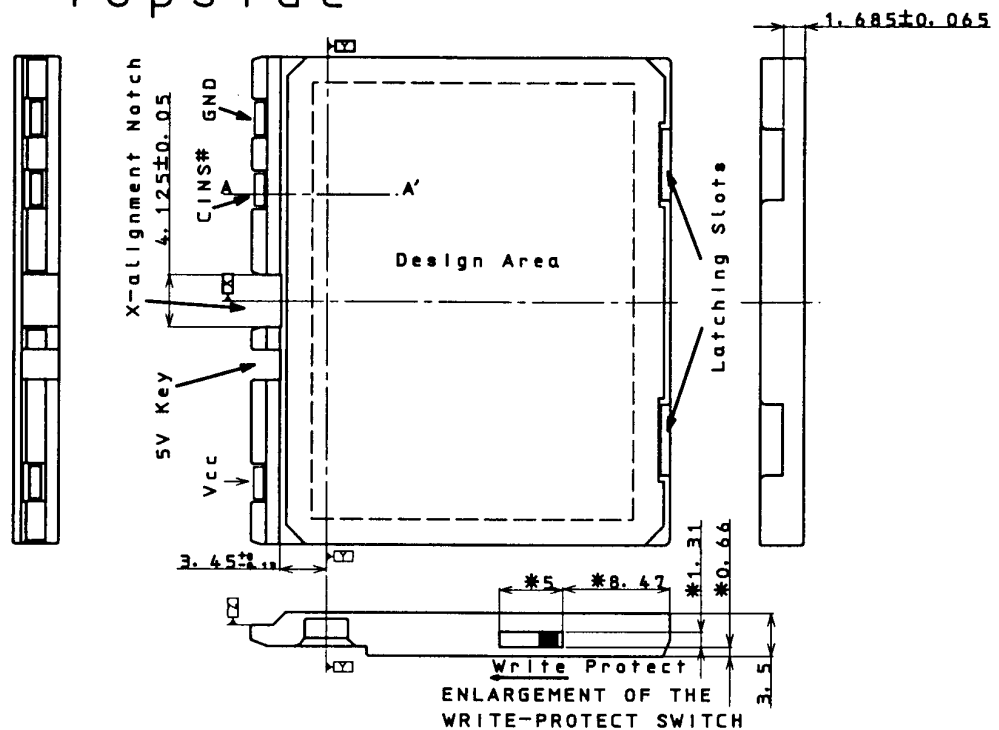
Specifications may be changed upon discussion and agreement between both parties.

13. Other Precautions

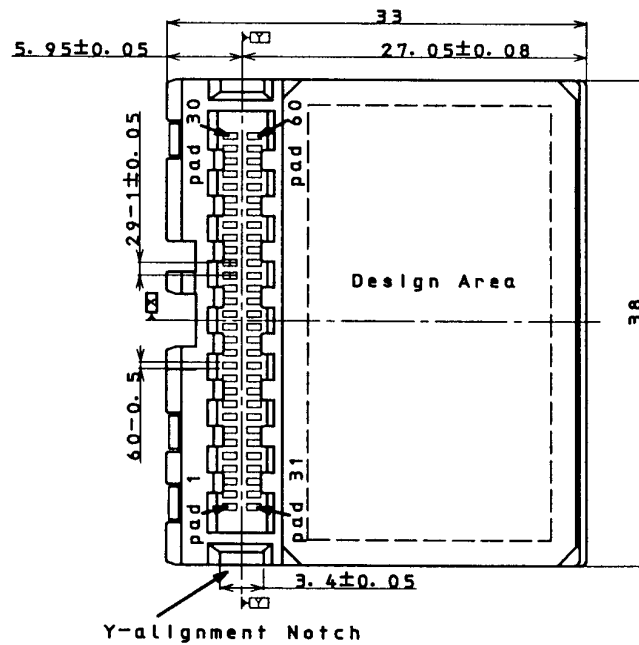
- Permanent damage occurs if the Miniature card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the Miniature card can be prevented by switching on the write protect switch on the side of the Miniature card.
- Avoid allowing the Miniature card Pads to come in contact with metals and avoid touching the Pads, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the Miniature card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the Miniature card is not being used, return it to its protective case.
- Do not allow the Miniature card to come in contact with fire.

14. External Dimensions

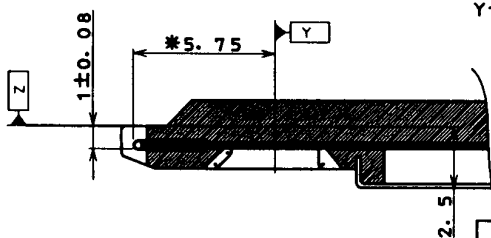
T o p s i d e



Bottomside



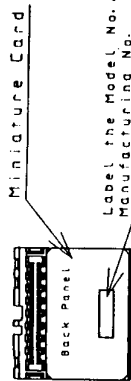
SECTION A-A'



APPLICABLE		SCALE		UNIT		<input type="checkbox"/> INCHES <input checked="" type="checkbox"/> MILLIMETERS			
				mm		CH. DATE		REVISE	
THICKNESS		TOLERANCES		MATERIAL		FINISH		CHARGE	
		DECIMALS . XX = ± 0.13 *X. XX = ± 0.25						NAME Miniature Card External Dimensions 5.0 Voltage-key	
DATE		1998. 10. 28						NAME Miniature Card Release 1. 1	
DESIGN/ DRAW		CHECK		APPROVE		IMAGE DEVICE ENGINEERING DEPT. 2 INTEGRATED CIRCUITS GROUP SHARP CORPORATION		DRAWING NO. IMC219-A100	

15. Packing Specification

Bottom side



Note 4

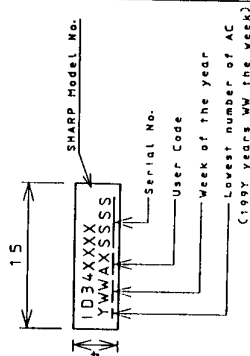
Parts List

Parts Name
A Flexible Plastic Bag
B Inner Carton
C Outer Carton
D Outer Case

Packing Specification

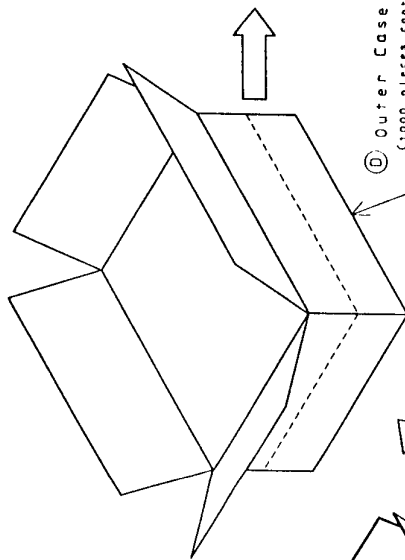
1. Label on which the Model No. and Manufacturing No. are printed is attached on the back panel of the card.
2. Each Miniature Card is contained in the Flexible plastic bag. (The term is "A" and is attached on the opposite side of the place where the card is released from the bag. That the terminals are not touched by finger, as shown in the figure.)
3. The inner carton contains 100 pieces of the card. (Note 1.)
4. The product name, lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is attached on inner carton.
5. The outer carton contains 5 inner cartons. (Note 2.)
6. The product name, lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is attached on the outer carton.
7. The outer carton is put into the outer case, which contains 2 outer cartons. (Note 3.)
8. The product name, lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is attached on the case.

1. The least packing unit is 100 pieces, which is contained in the inner carton.
2. The inner space of the outer carton is filled with card boards.
3. Other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 2 outer cartons.
4. The size and descriptions of the label on the back panel of the card are follows. [Unit:mm]



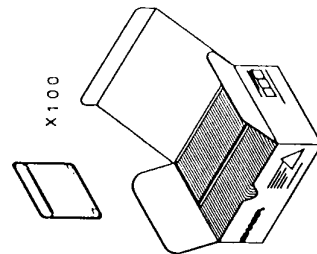
Flexible Plastic Bag

(A)



(D) Outer Case
(1000 pieces contained)

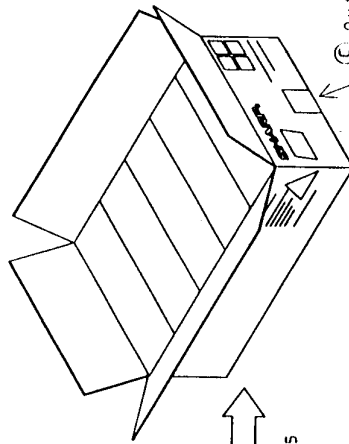
Note 3



X100

(B) Inner Carton
(100 pieces contained)

Note 1



X5

(C) Outer Carton
(500 pieces contained)

Note 2

APPLICABLE MODEL	ID34XXXX	SCALE	UNIT	mm
THICKNESS	DIFFERENCE	MATERIAL	FINISH	NAME
DATE	1999.10.30	DESIGNED BY	SALES PROJECT TEAM	DESIGNED BY
DATE	1999.10.30	DESIGNED BY	SALES PROJECT TEAM	DESIGNED BY
SHARP CORPORATION				DRAWING NO.
				IMC2-9-J100

Flash, 16 MB, Non-Volatile Memory, Miniature Card, PCMCIA Card, ID343K01