

LH1548

DESCRIPTION

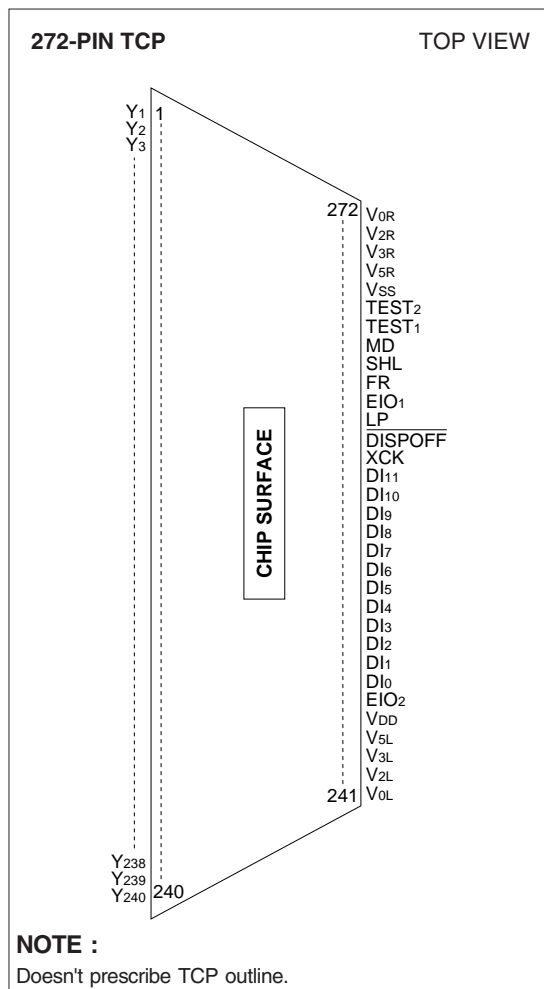
The LH1548 is a 240-output segment driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of UST (Ultra Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. When combined with the LH1530 common driver, it can create a low power consuming, high-resolution LCD.

FEATURES

- Number of LCD drive outputs : 240
- Supply voltage for LCD drive : +10.0 to +42.0 V
- Supply voltage for the logic system : +2.5 to +5.5 V
- Shift clock frequency
 - 25 MHz (Max.) : $V_{DD} = +5.0 \pm 0.5$ V
 - 15 MHz (Max.) : $V_{DD} = +3.0$ to $+4.5$ V
 - 12 MHz (Max.) : $V_{DD} = +2.5$ to $+3.0$ V
- Low power consumption
- Low output impedance
- Adopts a data bus system
- 8-bit/12-bit parallel input modes are selectable with a mode (MD) pin.
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Package : 272-pin TCP (Tape Carrier Package)

240-output LCD Segment Driver IC

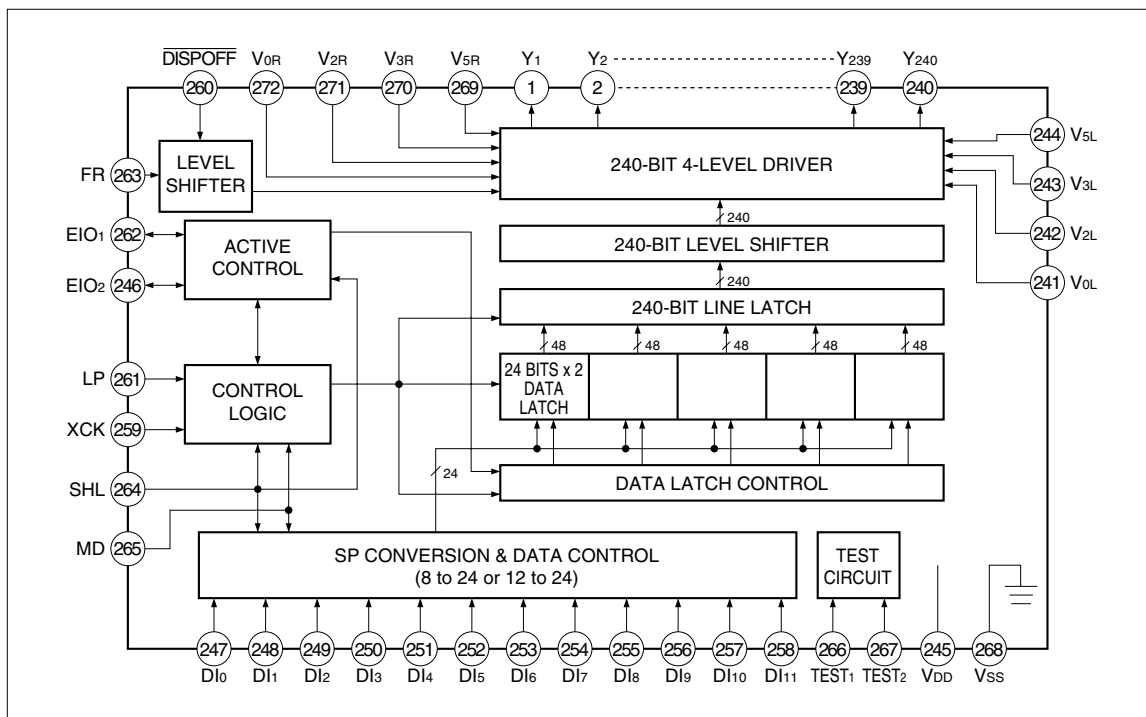
PIN CONNECTIONS



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 240	Y1-Y240	O	LCD drive output
241, 272	V _{0L} , V _{0R}	—	Power supply for LCD drive
242, 271	V _{2L} , V _{2R}	—	Power supply for LCD drive
243, 270	V _{3L} , V _{3R}	—	Power supply for LCD drive
244, 269	V _{5L} , V _{5R}	—	Power supply for LCD drive
245	V _{DD}	—	Power supply for logic system (+2.5 to +5.5 V)
264	SHL	I	Input for selecting the reading direction of display data
265	MD	I	Mode selection input
246, 262	EIO ₂ , EIO ₁	I/O	Input/output for chip selection
247 to 258	DI ₀ -DI ₁₁	I	Display data input
259	XCK	I	Clock input for taking display data
260	DISPOFF	I	Control input for output of non-select level
261	LP	I	Latch pulse input for display data
263	FR	I	AC-converting signal input for LCD drive waveform
266, 267	TEST ₁ , TEST ₂	I	Test mode selection input
268	V _{SS}	—	Ground (0 V)

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	Controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected.
SP Conversion & Data Control	Data is retained until 24 bits have been completely input, after which they are put on the internal data bus 24 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 48 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 10 sets of 24 bits.
Line Latch	All 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the latch data, and selects one of 4 levels (V ₀ , V ₂ , V ₃ or V ₅) based on the FR and $\overline{\text{DISPOFF}}$ signals.
Control Logic	Controls the operation of each block. When an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected.
Test Circuit	The circuit for testing. During normal operation, it isn't activated.

INPUT/OUTPUT CIRCUITS

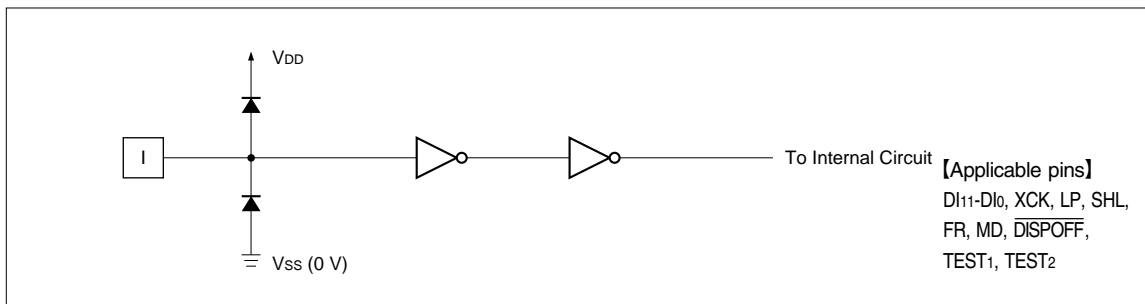


Fig. 1 Input Circuit

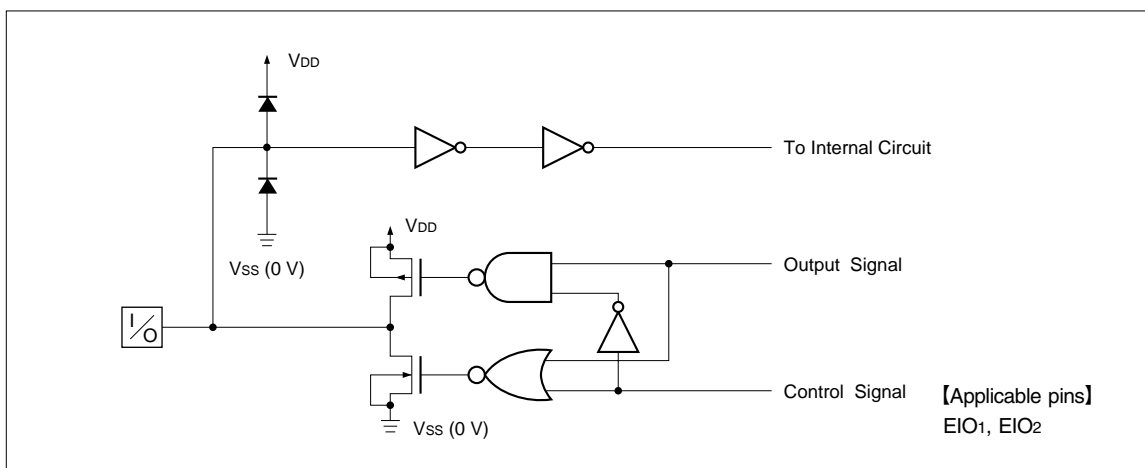


Fig. 2 Input/Output Circuit

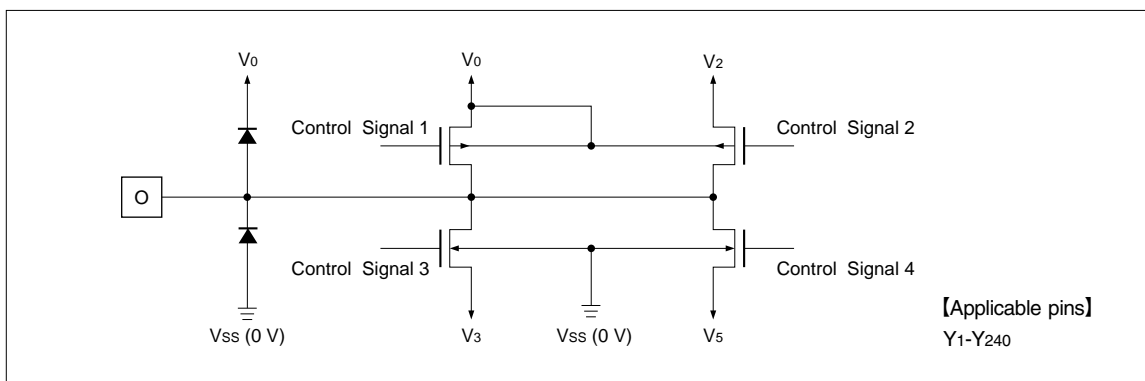


Fig. 3 LCD Drive Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
VDD	Logic system power supply pin, connected to +2.5 to +5.5 V.
VSS	Ground pin, connected to 0 V.
V0L, V0R V2L, V2R V3L, V3R V5L, V5R	<p>Bias power supply pins for LCD drive voltage</p> <ul style="list-style-type: none"> • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_3 < V_2 < V_0$. • V_{iL} and V_{iR} ($i = 0, 2, 3, 5$) aren't connected with inside IC. Therefore, it is necessary that these pins connect with an external power supply.
DI11-DI0	<p>Input pins for display data</p> <ul style="list-style-type: none"> • In 8-bit parallel input mode, input data into the 8 pins, DI7-DI0. Connect DI11-DI8 to VSS or VDD. • In 12-bit parallel input mode, input data into the 12 pins, DI11-DI0. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	<p>Clock input pin for taking display data</p> <ul style="list-style-type: none"> • Data is read at the falling edge of the clock pulse.
LP	<p>Latch pulse input pin for display data</p> <ul style="list-style-type: none"> • Data is latched at the falling edge of the clock pulse.
SHL	<p>Input pin for selecting the reading direction of display data</p> <ul style="list-style-type: none"> • When set to VSS level "L", data is read sequentially from Y240 to Y1. • When set to VDD level "H", data is read sequentially from Y1 to Y240. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
$\overline{\text{DISPOFF}}$	<p>Control input pin for output of non-select level</p> <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to VSS level "L", the LCD drive output pins (Y1-Y240) are set to level V5. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	<p>AC signal input pin for LCD driving waveform</p> <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	<p>Mode selection pin</p> <ul style="list-style-type: none"> • When set to VSS level "L", 8-bit parallel input mode is set. • When set to VDD level "H", 12-bit parallel input mode is set. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.

SYMBOL	FUNCTION
EIO1 EIO2	<p>Input/output pins for chip selection</p> <ul style="list-style-type: none"> • When SHL input is at Vss level "L", EIO1 is set for output, and EIO2 is set for input. • When SHL input is at VDD level "H", EIO1 is set for input, and EIO2 is set for output. • During output, set to "H" while $LP \cdot \overline{XCK}$ is "H", and after 240 bits of data have been read, set to "L" for one cycle (from rising edge to rising edge of XCK), after which it returns to "H". • During input, the chip is selected while $\overline{EI} \cdot \overline{XCK}$ is "H" after the LP signal is input. The chip is non-selected after 240 bits of data have been read. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
TEST1 TEST2	<p>Test mode selection pins</p> <ul style="list-style-type: none"> • During normal operation, fix to Vss level "L".
Y1-Y240	<p>LCD drive output pins</p> <ul style="list-style-type: none"> • Corresponding directly to each bit of the data latch, one level (V0, V2, V3, or V5) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

Functional Operations

TRUTH TABLE

FR	LATCH DATA	$\overline{\text{DISPOFF}}$	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V ₃
L	H	H	V ₅
H	L	H	V ₂
H	H	H	V ₀
X	X	L	V ₅

NOTES :

- $V_{SS} \leq V_5 < V_3 < V_2 < V_0$, L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(a) 8-bit Parallel Input Mode

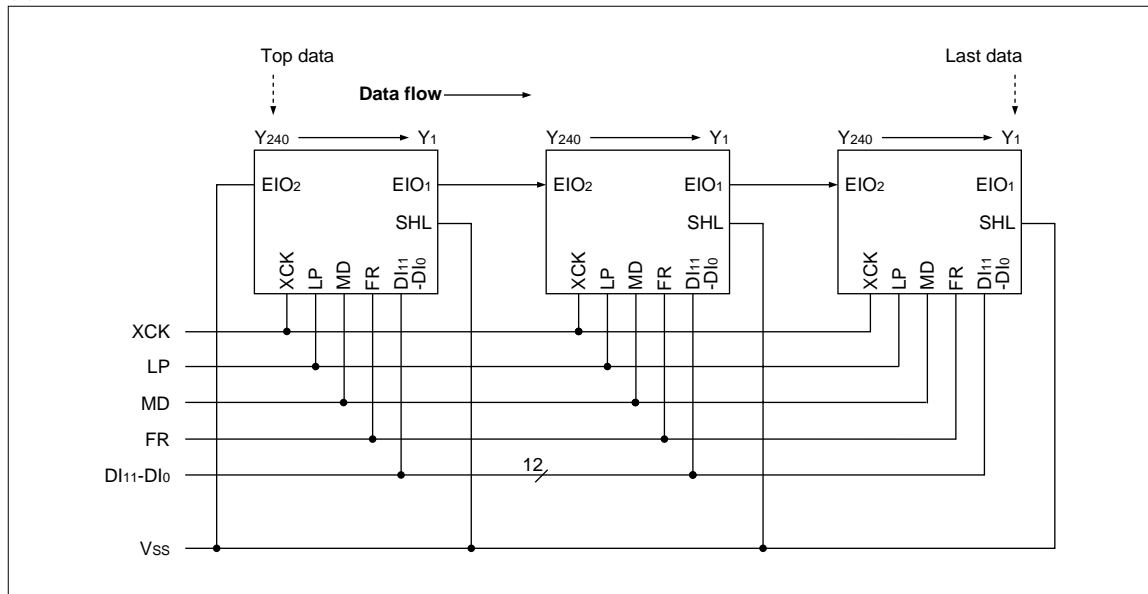
MD	SHL	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI0	Y1	Y9	Y17	...	Y217	Y225	Y233
				DI1	Y2	Y10	Y18	...	Y218	Y226	Y234
				DI2	Y3	Y11	Y19	...	Y219	Y227	Y235
				DI3	Y4	Y12	Y20	...	Y220	Y228	Y236
				DI4	Y5	Y13	Y21	...	Y221	Y229	Y237
				DI5	Y6	Y14	Y22	...	Y222	Y230	Y238
				DI6	Y7	Y15	Y23	...	Y223	Y231	Y239
				DI7	Y8	Y16	Y24	...	Y224	Y232	Y240
L	H	Input	Output	DI0	Y240	Y232	Y224	...	Y24	Y16	Y8
				DI1	Y239	Y231	Y223	...	Y23	Y15	Y7
				DI2	Y238	Y230	Y222	...	Y22	Y14	Y6
				DI3	Y237	Y229	Y221	...	Y21	Y13	Y5
				DI4	Y236	Y228	Y220	...	Y20	Y12	Y4
				DI5	Y235	Y227	Y219	...	Y19	Y11	Y3
				DI6	Y234	Y226	Y218	...	Y18	Y10	Y2
				DI7	Y233	Y225	Y217	...	Y17	Y9	Y1

(b) 12-bit Parallel Input Mode

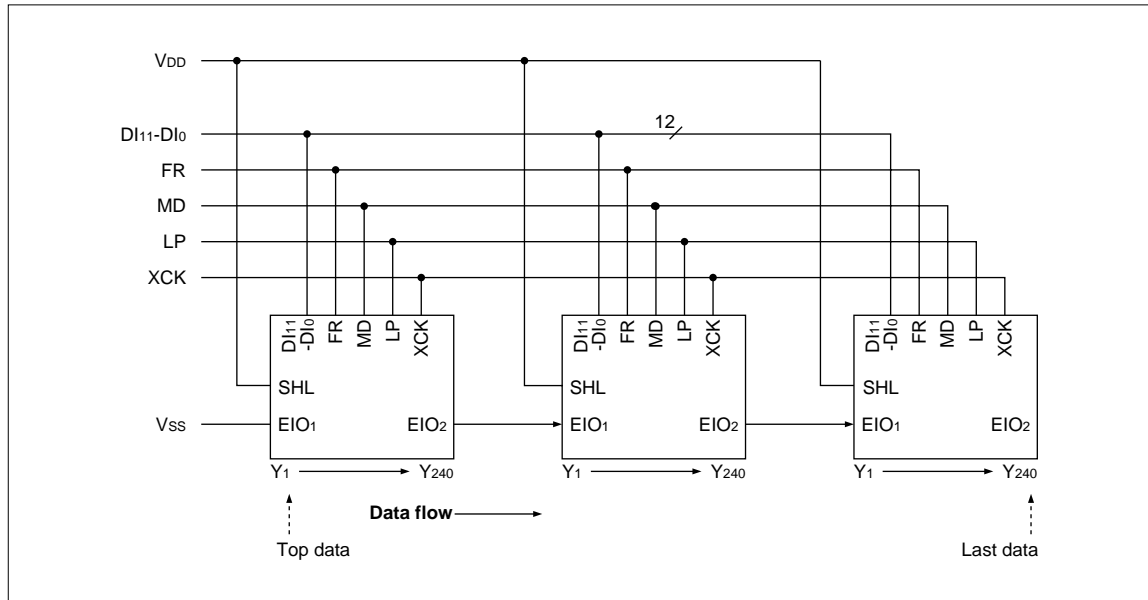
MD	SHL	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					20 CLOCK	19 CLOCK	18 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI ₀	Y ₁	Y ₁₃	Y ₂₅	...	Y ₂₀₅	Y ₂₁₇	Y ₂₂₉
				DI ₁	Y ₂	Y ₁₄	Y ₂₆	...	Y ₂₀₆	Y ₂₁₈	Y ₂₃₀
				DI ₂	Y ₃	Y ₁₅	Y ₂₇	...	Y ₂₀₇	Y ₂₁₉	Y ₂₃₁
				DI ₃	Y ₄	Y ₁₆	Y ₂₈	...	Y ₂₀₈	Y ₂₂₀	Y ₂₃₂
				DI ₄	Y ₅	Y ₁₇	Y ₂₉	...	Y ₂₀₉	Y ₂₂₁	Y ₂₃₃
				DI ₅	Y ₆	Y ₁₈	Y ₃₀	...	Y ₂₁₀	Y ₂₂₂	Y ₂₃₄
				DI ₆	Y ₇	Y ₁₉	Y ₃₁	...	Y ₂₁₁	Y ₂₂₃	Y ₂₃₅
				DI ₇	Y ₈	Y ₂₀	Y ₃₂	...	Y ₂₁₂	Y ₂₂₄	Y ₂₃₆
				DI ₈	Y ₉	Y ₂₁	Y ₃₃	...	Y ₂₁₃	Y ₂₂₅	Y ₂₃₇
				DI ₉	Y ₁₀	Y ₂₂	Y ₃₄	...	Y ₂₁₄	Y ₂₂₆	Y ₂₃₈
				DI ₁₀	Y ₁₁	Y ₂₃	Y ₃₅	...	Y ₂₁₅	Y ₂₂₇	Y ₂₃₉
				DI ₁₁	Y ₁₂	Y ₂₄	Y ₃₆	...	Y ₂₁₆	Y ₂₂₈	Y ₂₄₀
H	H	Input	Output	DI ₀	Y ₂₄₀	Y ₂₂₈	Y ₂₁₆	...	Y ₃₆	Y ₂₄	Y ₁₂
				DI ₁	Y ₂₃₉	Y ₂₂₇	Y ₂₁₅	...	Y ₃₅	Y ₂₃	Y ₁₁
				DI ₂	Y ₂₃₈	Y ₂₂₆	Y ₂₁₄	...	Y ₃₄	Y ₂₂	Y ₁₀
				DI ₃	Y ₂₃₇	Y ₂₂₅	Y ₂₁₃	...	Y ₃₃	Y ₂₁	Y ₉
				DI ₄	Y ₂₃₆	Y ₂₂₄	Y ₂₁₂	...	Y ₃₂	Y ₂₀	Y ₈
				DI ₅	Y ₂₃₅	Y ₂₂₃	Y ₂₁₁	...	Y ₃₁	Y ₁₉	Y ₇
				DI ₆	Y ₂₃₄	Y ₂₂₂	Y ₂₁₀	...	Y ₃₀	Y ₁₈	Y ₆
				DI ₇	Y ₂₃₃	Y ₂₂₁	Y ₂₀₉	...	Y ₂₉	Y ₁₇	Y ₅
				DI ₈	Y ₂₃₂	Y ₂₂₀	Y ₂₀₈	...	Y ₂₈	Y ₁₆	Y ₄
				DI ₉	Y ₂₃₁	Y ₂₁₉	Y ₂₀₇	...	Y ₂₇	Y ₁₅	Y ₃
				DI ₁₀	Y ₂₃₀	Y ₂₁₈	Y ₂₀₆	...	Y ₂₆	Y ₁₄	Y ₂
				DI ₁₁	Y ₂₂₉	Y ₂₁₇	Y ₂₀₅	...	Y ₂₅	Y ₁₃	Y ₁

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

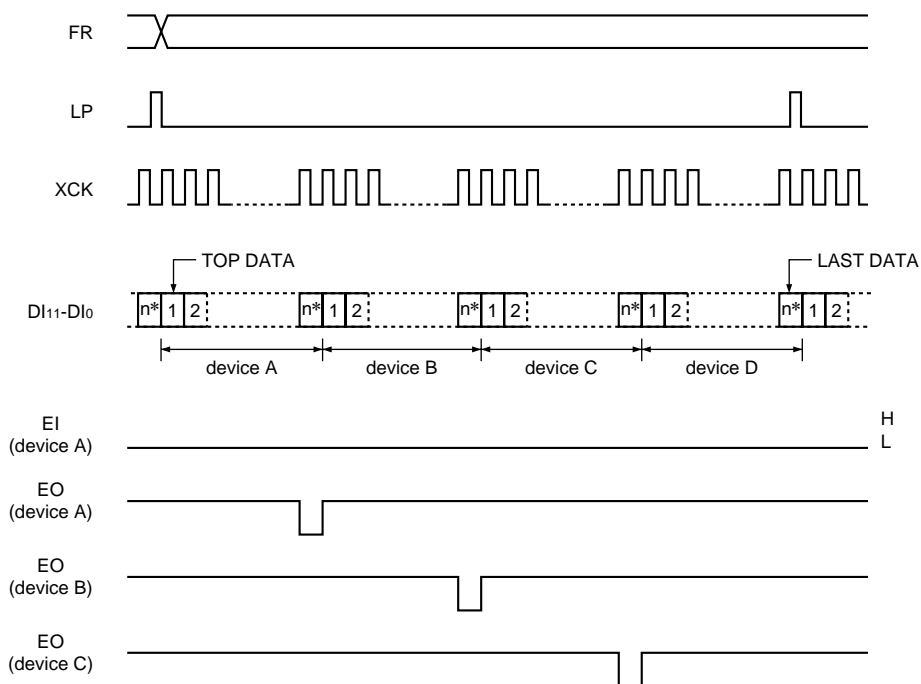
(a) When SHL = "L"



(b) When SHL = "H"



TIMING CHART OF 4-DEVICE CASCADE CONNECTION



* $n = 30$ in 8-bit parallel input mode.
 $n = 20$ in 12-bit parallel input mode.

PRECAUTIONS

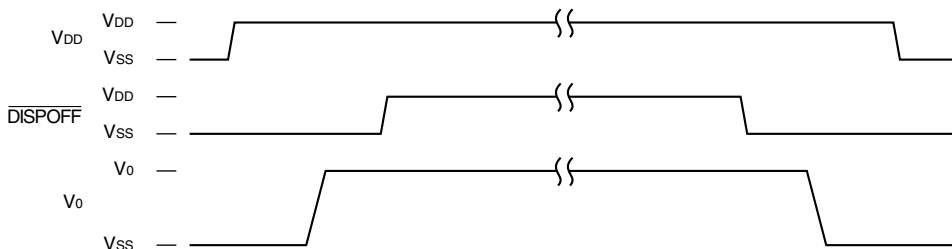
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on $\overline{\text{DISPOFF}}$ function. After that, cancel the $\overline{\text{DISPOFF}}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on $\overline{\text{DISPOFF}}$ function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V _{DD}	V _{DD}	−0.3 to +7.0	V	1, 2
Supply voltage (2)	V ₀	V _{0L} , V _{0R}	−0.3 to +45.0	V	
	V ₂	V _{2L} , V _{2R}	−0.3 to V ₀ + 0.3	V	
	V ₃	V _{3L} , V _{3R}	−0.3 to V ₀ + 0.3	V	
	V ₅	V _{5L} , V _{5R}	−0.3 to V ₀ + 0.3	V	
Input voltage	V _I	DI ₁₁ -DI ₀ , XCK, LP, SHL, FR, MD, EIO ₁ , EIO ₂ , $\overline{\text{DISPOFF}}$, TEST ₁ , TEST ₂	−0.3 to V _{DD} + 0.3	V	
Storage temperature	T _{STG}		−45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V _{DD}	V _{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V ₀	V _{0L} , V _{0R}	+10.0		+42.0	V	
Operating temperature	T _{OPR}		−20		+85	°C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that V_{SS} ≤ V₅ < V₃ < V₂ < V₀.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{SS} = V_S = 0 V, V_{DD} = +2.5 to +5.5 V, V_O = +10.0 to +42.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		DI11-DI0, XCK, LP, SHL, FR,			0.3V _{DD}	V	
Input "High" voltage	V _{IH}		MD, EIO1, EIO2, DISPOFF	0.7V _{DD}			V	
Output "Low" voltage	V _{OL}	I _{OL} = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} - 0.4			V	
Input leakage current	I _{LI}	V _{SS} ≤ V _I ≤ V _{DD}	All input pins			±10.0	μA	
I/O leakage current	I _{LI/O}	V _{SS} ≤ V _I ≤ V _{DD}	EIO1, EIO2			±10.0	μA	
Output resistance	R _{ON}	ΔV _{ON} = 0.5 V	Y1-Y240		1.0	1.5	kΩ	
					1.5	2.0		
					2.0	2.5		
Standby current	I _{STB}		V _{SS}			75.0	μA	1
Supply current (1) (Non-selection)	I _{DD1}		V _{DD}			2.4	mA	2
Supply current (2) (Selection)	I _{DD2}		V _{DD}			14.4	mA	3
Supply current (3)	I _O		V _{OL} , V _{OR}			2.0	mA	4

NOTES :

- V_{DD} = +5.0 V, V_O = +40.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}.
- V_{DD} = +5.0 V, V_O = +40.0 V, f_{XCK} = 25 MHz, no-load, E_I = V_{DD}.
The input data is turned over by data taking clock (8-bit parallel input mode).
- V_{DD} = +5.0 V, V_O = +40.0 V, f_{XCK} = 25 MHz, no-load, E_I = V_{SS}.
The input data is turned over by data taking clock (8-bit parallel input mode).
- V_{DD} = +5.0 V, V_O = +40.0 V, f_{XCK} = 25 MHz, f_{LP} = 38.4 kHz, f_{FR} = 80 Hz, no-load.
The input data is turned over by data taking clock (8-bit parallel input mode).

AC Characteristics

(Mode 1)

($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +5.0 \pm 0.5\text{ V}$, $V_0 = +10.0$ to $+42.0\text{ V}$, $T_{OPR} = -20$ to $+85\text{ }^{\circ}\text{C}$,
the figure in parenthesis applies when $T_{OPR1} = -20$ to $+60\text{ }^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	twCK	$t_R, t_F \leq 7\text{ (5) ns}$	40 (36)			ns	1
Shift clock "H" pulse width	twCKH		12			ns	
Shift clock "L" pulse width	twCKL		14			ns	
Data setup time	tDS		5			ns	
Data hold time	tDH		15			ns	
Latch pulse "H" pulse width	twLPH		15			ns	
Shift clock rise to latch pulse rise time	tLD		5			ns	
Shift clock fall to latch pulse fall time	tSL		25			ns	
Latch pulse rise to shift clock rise time	tLS		25			ns	
Latch pulse fall to shift clock fall time	tLH		25			ns	
Enable setup time	tS		5 (4)			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
Output delay time (1)	tD	$C_L = 15\text{ pF}$			28 (27)	ns	
Output delay time (2)	tPD1	$C_L = 15\text{ pF}$			1.2	μs	
Output delay time (3)	tPD2	$C_L = 15\text{ pF}$			1.2	μs	

NOTES :

1. Takes the cascade connection into consideration.
2. $(twCK - twCKH - twCKL)/2$ is maximum in the case of high speed operation.

(Mode 2)

($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +3.0$ to $+4.5\text{ V}$, $V_0 = +10.0$ to $+42.0\text{ V}$, $T_{OPR} = -20$ to $+85\text{ }^{\circ}\text{C}$,
the figure in parenthesis applies when $T_{OPR1} = -20$ to $+60\text{ }^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	twCK	$t_R, t_F \leq 10\text{ ns}$	66 (60)			ns	1
Shift clock "H" pulse width	twCKH		23 (20)			ns	
Shift clock "L" pulse width	twCKL		23 (20)			ns	
Data setup time	tDS		10			ns	
Data hold time	tDH		25 (20)			ns	
Latch pulse "H" pulse width	twLPH		30			ns	
Shift clock rise to latch pulse rise time	tLD		10			ns	
Shift clock fall to latch pulse fall time	tSL		30			ns	
Latch pulse rise to shift clock rise time	tLS		30			ns	
Latch pulse fall to shift clock fall time	tLH		30			ns	
Enable setup time	tS		12 (10)			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
Output delay time (1)	tD	$C_L = 15\text{ pF}$			44 (40)	ns	
Output delay time (2)	tPD1	$C_L = 15\text{ pF}$			1.2	μs	
Output delay time (3)	tPD2	$C_L = 15\text{ pF}$			1.2	μs	

NOTES :

1. Takes the cascade connection into consideration.
2. $(twCK - twCKH - twCKL)/2$ is maximum in the case of high speed operation.

(Mode 3) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+3.0\text{ V}$, $V_0 = +10.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -20\text{ to }+85\text{ }^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	twCK	$t_R, t_F \leq 10\text{ ns}$	82			ns	1
Shift clock "H" pulse width	twCKH		28			ns	
Shift clock "L" pulse width	twCKL		28			ns	
Data setup time	tDS		10			ns	
Data hold time	tDH		30			ns	
Latch pulse "H" pulse width	twLPH		30			ns	
Shift clock rise to latch pulse rise time	tLD		10			ns	
Shift clock fall to latch pulse fall time	tSL		30			ns	
Latch pulse rise to shift clock rise time	tLS		30			ns	
Latch pulse fall to shift clock fall time	tLH		30			ns	
Enable setup time	tS		15			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
Output delay time (1)	tD	$C_L = 15\text{ pF}$			57	ns	
Output delay time (2)	tPD1	$C_L = 15\text{ pF}$			1.2	μs	
Output delay time (3)	tPD2	$C_L = 15\text{ pF}$			1.2	μs	

NOTES :

1. Takes the cascade connection into consideration.
2. $(twCK - twCKH - twCKL)/2$ is maximum in the case of high speed operation.

Timing Chart

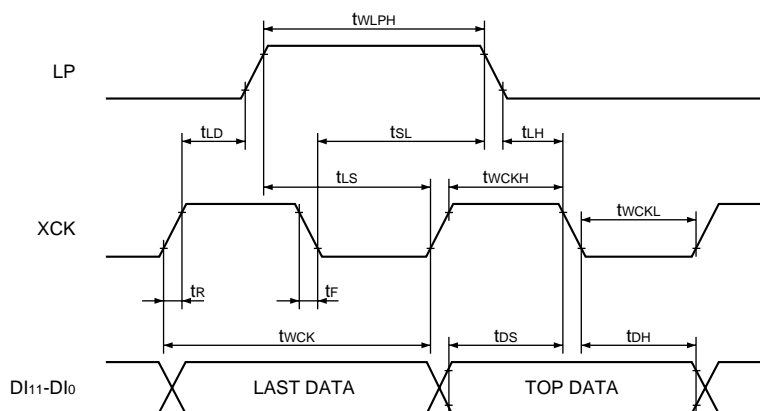
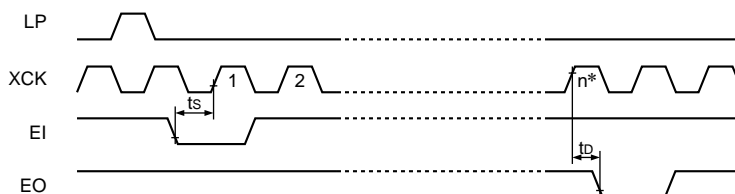


Fig. 4 Timing Characteristics (1)



* $n = 30$ in 8-bit parallel input mode.
 $n = 20$ in 12-bit parallel input mode.

Fig. 5 Timing Characteristics (2)

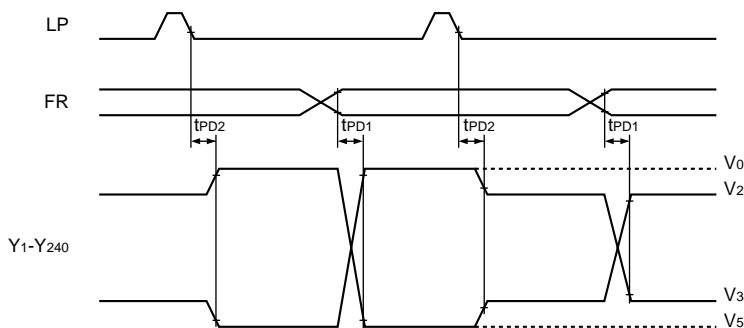
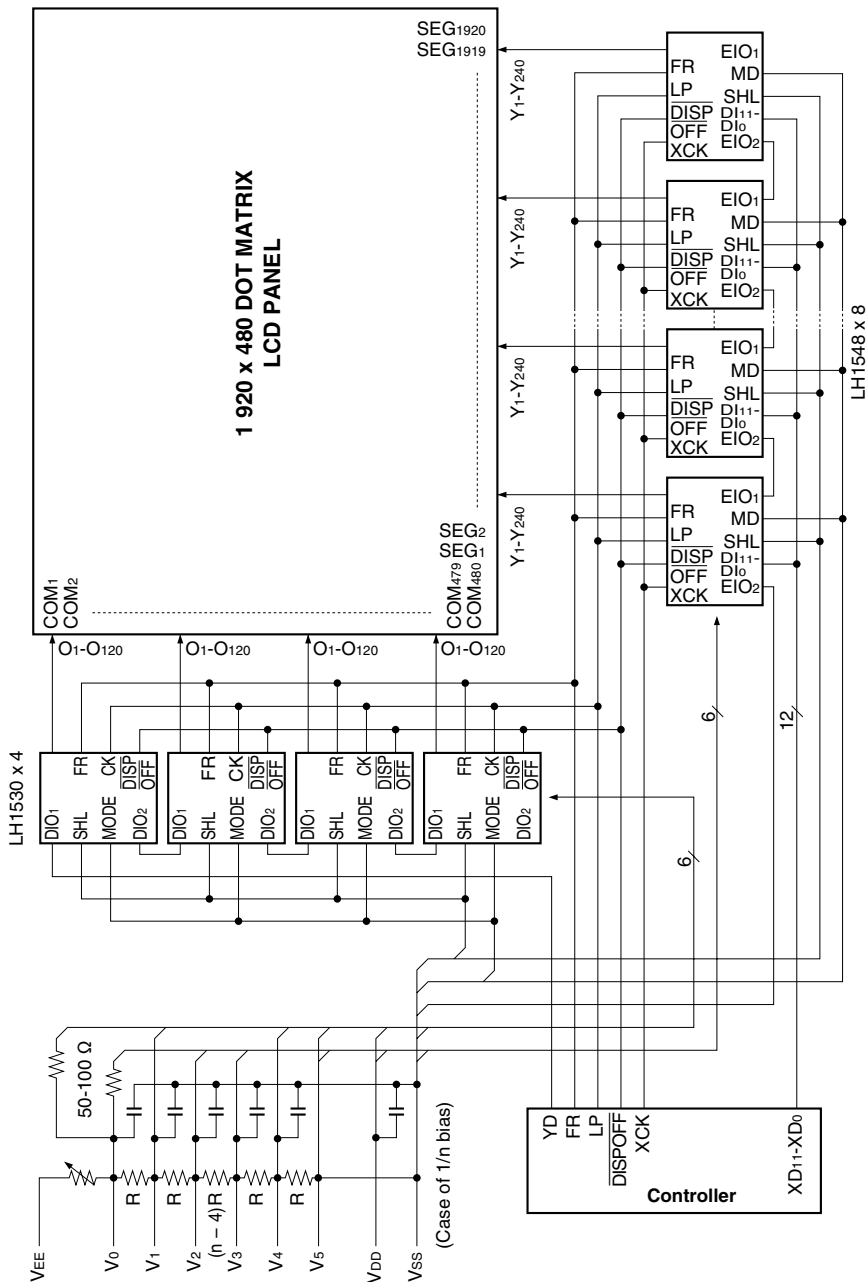
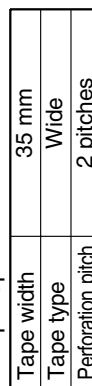


Fig. 6 Timing Characteristics (3)

SYSTEM CONFIGURATION EXAMPLE



(Unit : mm)



UIPELEX is a trademark of UBE INDUSTRIES, LTD..