

# LH5164A/AH

CMOS 64K (8K × 8) Static RAM

## FEATURES

- 8,192 × 8 bit organization
- Access times: 80/100 ns (MAX.)
- Low-power consumption:
  - Operating:
    - 303 mW (MAX.) LH5164A/D/N @ 80 ns
    - 248 mW (MAX.) LH5164A/D/N/T @ 100 ns
    - 275 mW (MAX.) LH5164AH/HD/HN/HT @ 100 ns
  - Standby:
    - LH5164A/D/N/T: 5.5 μW (MAX.)
    - LH5164AH/HD/HN/HT:
      - T<sub>A</sub> ≤ 85°C: 16.5 μW (MAX.)
      - T<sub>A</sub> ≤ 70°C: 5.5 μW (MAX.)
- Fully-static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Wide temperature range available
  - LH5164A: -10 to +70°C
  - LH5164AH: -40 to +85°C
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)

## DESCRIPTION

The LH5164A/AH are static RAMs organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5164AH is designed for wide temperature range from -40 to +85°C.

## PIN CONNECTIONS

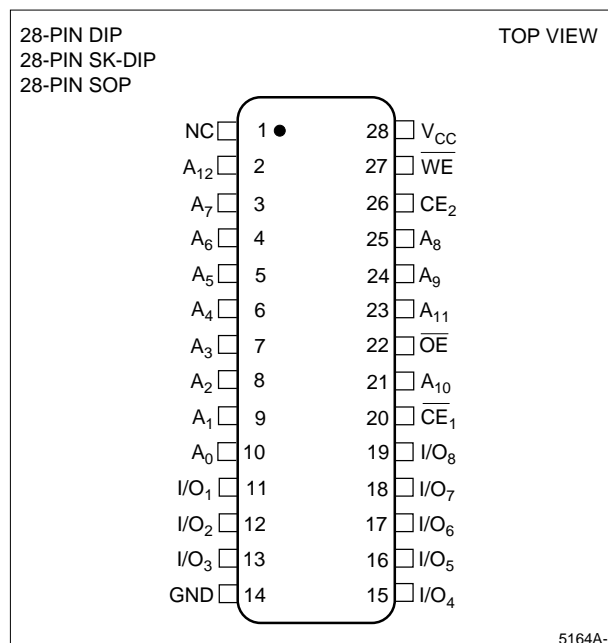


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

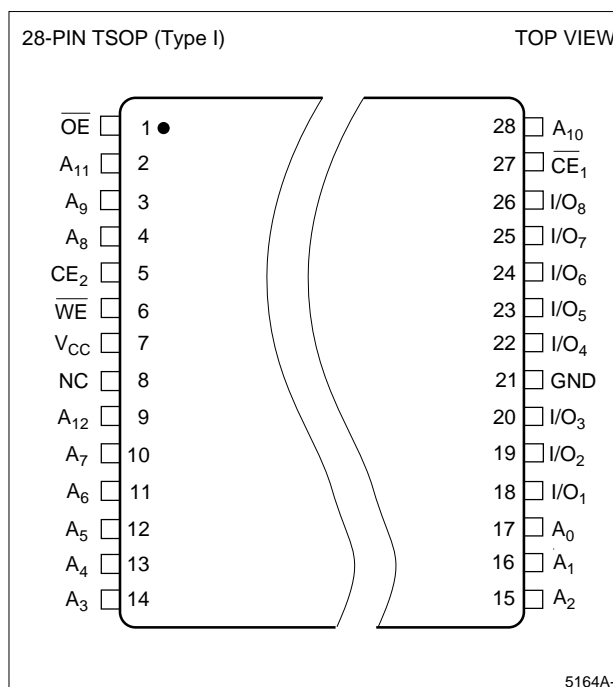


Figure 2. Pin Connections for TSOP Package

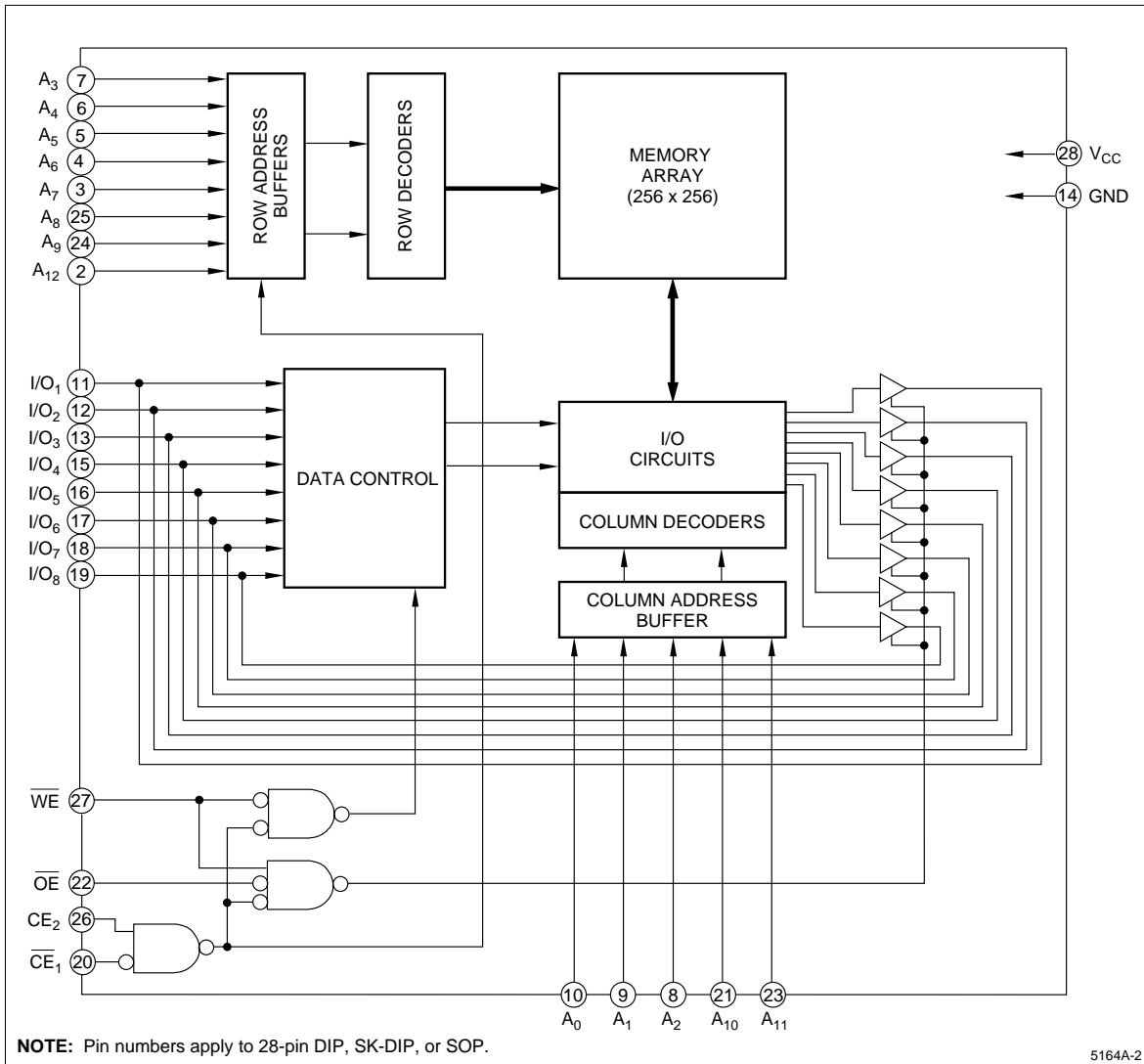


Figure 3. LH5164A/AH Block Diagram

# PIN DESCRIPTION

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>12</sub>	Address inputs
CE <sub>1</sub> - CE <sub>2</sub>	Chip Enable input
WE	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O <sub>1</sub> - I/O <sub>8</sub>	Data inputs and outputs
V <sub>CC</sub>	Power supply
GND	Ground
NC	No connection

# TRUTH TABLE

$\overline{CE}_1$	CE <sub>2</sub>	$\overline{WE}$	$\overline{OE}$	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
X	L	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
L	H	L	X	Write	D <sub>IN</sub>	Operating (I <sub>CC</sub> )	1
L	H	H	L	Read	D <sub>OUT</sub>	Operating (I <sub>CC</sub> )	
L	H	H	H	Output disable	High-Z	Operating (I <sub>CC</sub> )	

**NOTE:**  
1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	80 ns	100 ns	UNIT	NOTE
		RATING	RATING		
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> + 0.3	-0.3 to V <sub>CC</sub> + 0.3	V	1, 2
Operating temperature	T <sub>opr</sub>	-10 to +70	-10 to +70	°C	3
			-40 to +85	°C	4
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C	

## NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. V<sub>IN</sub> (MIN.) = -3.0 V for pulse width ≤ 50 ns.
3. LH5164A/AD/AN/AT
4. LH5164AH/AHD/AHN/AHT

RECOMMENDED OPERATING CONDITIONS <sup>1</sup>

PARAMETER	SYMBOL	80 ns			100 ns			UNIT	NOTE
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	4.5	5.0	5.5	V	
Input voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V	
	V <sub>IL</sub>	-0.3		0.8	-0.3		0.8	V	2

## NOTES:

1. T<sub>A</sub> = -10 to +70°C (LH5164A/AD/AN/AT), T<sub>A</sub> = -40 to +85°C (LH5164AH/AHD/AHN/AHT).
2. V<sub>IN</sub> (MIN.) = -3.0 V for pulse width ≤ 50 ns.

DC CHARACTERISTICS <sup>1</sup> (V<sub>CC</sub> = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1.0	1.0	μA	
Output leakage current	I <sub>LO</sub>	CE <sub>1</sub> = V <sub>IH</sub> or CE <sub>2</sub> = V <sub>IL</sub> or OE = V <sub>IH</sub> or WE = V <sub>IL</sub> V <sub>IO</sub> = 0 to V <sub>CC</sub>	-1.0	1.0	μA	
Operating current	I <sub>CC</sub>	CE <sub>1</sub> = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , Outputs open		55	mA	
		CE <sub>1</sub> = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , Outputs open		45	mA	2
		CE <sub>1</sub> = V <sub>IL</sub> , V <sub>IN</sub> = 0.2 V or V <sub>CC</sub> - 0.2 V CE <sub>2</sub> = V <sub>IH</sub> , Outputs open		10		3
Standby current	I <sub>SB1</sub>	CE <sub>1</sub> = V <sub>IH</sub> or CE <sub>2</sub> = V <sub>IL</sub>		5	mA	
		CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2 V	T <sub>A</sub> ≤ 70°C	1.0	μA	2, 3, 4
			T <sub>A</sub> ≤ 85°C	3.0	μA	3, 4
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA		0.4	V	
	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4		V	

## NOTES:

1. T<sub>A</sub> = -10 to 70°C (LH5164A/AD/AN/AT), T<sub>A</sub> = -40 to +85°C (LH5164AH/AHD/AHN/AHT)
2. LH5164A/AD/AN/AT
3. LH5164AH/AHD/AHN/AHT
4. CE<sub>2</sub> should be ≥ V<sub>CC</sub> - 0.2 V or ≤ 0.2 V when CE<sub>1</sub> ≥ V<sub>CC</sub> - 0.2 V

## AC CHARACTERISTICS <sup>1</sup>

### (1) READ CYCLE ( $V_{CC} = 5\text{ V} \pm 10\%$ )

PARAMETER		SYMBOL	80 ns		100 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Read cycle time		t <sub>RC</sub>	80		100		ns	
Address access time		t <sub>AA</sub>		80		100	ns	
Chip enable access time	(CE <sub>1</sub> )	t <sub>ACE1</sub>		80		100	ns	
	(CE <sub>2</sub> )	t <sub>ACE2</sub>		80		100	ns	
Output enable access time		t <sub>OE</sub>		40		40	ns	
Output hold time		t <sub>OH</sub>	10		10		ns	
Chip enable to output in Low-Z	(CE <sub>1</sub> )	t <sub>LZ1</sub>	10		10		ns	1
	(CE <sub>2</sub> )	t <sub>LZ2</sub>	10		10		ns	1
Output enable to output in Low-Z		t <sub>OLZ</sub>	5		5		ns	1
Chip enable to output in High-Z	(CE <sub>1</sub> )	t <sub>HZ1</sub>	0	30	0	30	ns	1
	(CE <sub>2</sub> )	t <sub>HZ2</sub>	0	30	0	30	ns	1
Output disable to output in High-Z		t <sub>OHZ</sub>	0	20	0	20	ns	1

### (2) WRITE CYCLE ( $V_{CC} = 5\text{ V} \pm 10\%$ )

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	$t_{WC}$	80		100		ns	
Chip enable to end of write	$t_{CW}$	70		80		ns	
Address valid to end of write	$t_{AW}$	70		80		ns	
Address setup time	$t_{AS}$	0		0		ns	
Write pulse width	$t_{WP}$	60		60		ns	
Write recovery time	$t_{WR}$	0		0		ns	
Data valid to end of write	$t_{DW}$	40		40		ns	
Data hold time	$t_{DH}$	0		0		ns	
Output active from end of write	$t_{OW}$	10		10		ns	2
WE to output in High-Z	$t_{WZ}$	0	30	0	30	ns	2
OE to output in High-Z	$t_{OHZ}$	0	20	0	20	ns	2

#### NOTES:

- $T_A = -10$  to  $+70^\circ\text{C}$  (LH5164A/AD/AN/AT),  $T_A = -40$  to  $+85^\circ\text{C}$  (LH5164AH/AHD/AHN/AHT)
- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 200$  mV transition from steady state levels into the test load.

## AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL + $C_L$ (100 pF)	1

#### NOTE:

- Includes scope and jig capacitance.

**CAPACITANCE <sup>1</sup> ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$			7	pF
Input/output capacitance	$C_{I/O}$	$V_{IO} = 0\text{ V}$			10	pF

**NOTE:**

1. This parameter is sampled and not production tested.

**DATA RETENTION CHARACTERISTICS <sup>1</sup>**

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	$V_{CCDR}$	$CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CCDR} - 0.2\text{ V}$	2.0	5.5	V	2
Data retention current	$I_{CCDR}$	$V_{CCDR} = 3\text{ V}$ , $CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CCDR} - 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	0.2	$\mu\text{A}$	2, 3
			$T_A = 40^\circ\text{C}$	0.4	$\mu\text{A}$	2, 3
				0.6	$\mu\text{A}$	2, 3
		$V_{CCDR} = 3\text{ V}$ , $CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CCDR} - 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	0.2	$\mu\text{A}$	2, 4
			$T_A = 70^\circ\text{C}$	0.6	$\mu\text{A}$	2, 4
				1.5	$\mu\text{A}$	2, 4
Chip disable to data retention	$t_{CDR}$		0		ns	
Recovery time	$t_R$		$t_{RC}$		ns	5

**NOTES:**

- $T_A = -10$  to  $+70^\circ\text{C}$  (LH5164A/AD/AN/AT),  $T_A = -40$  to  $+85^\circ\text{C}$  (LH5164AH/AHD/AHN/AHT)
- $CE_2$  should be  $\geq V_{CCDR} - 0.2\text{ V}$  or  $\leq 0.2\text{ V}$  when  $CE_1 \geq V_{CCDR} - 0.2\text{ V}$
- LH5164A/AD/AN/AT
- LH5164AH/AHD/AHN/AHT
- $t_{RC}$  = Read cycle time

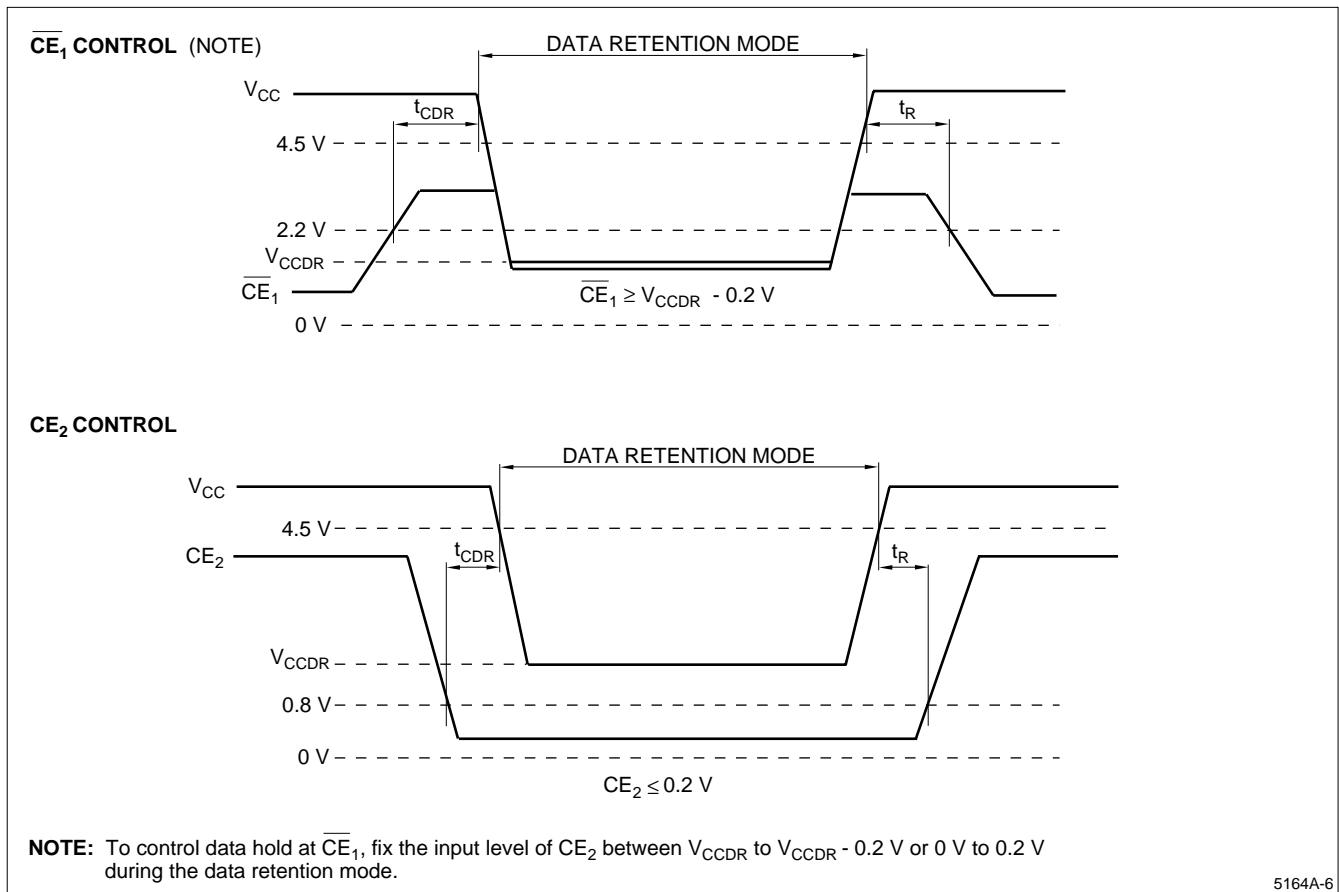


Figure 4. Low Voltage Data Retention

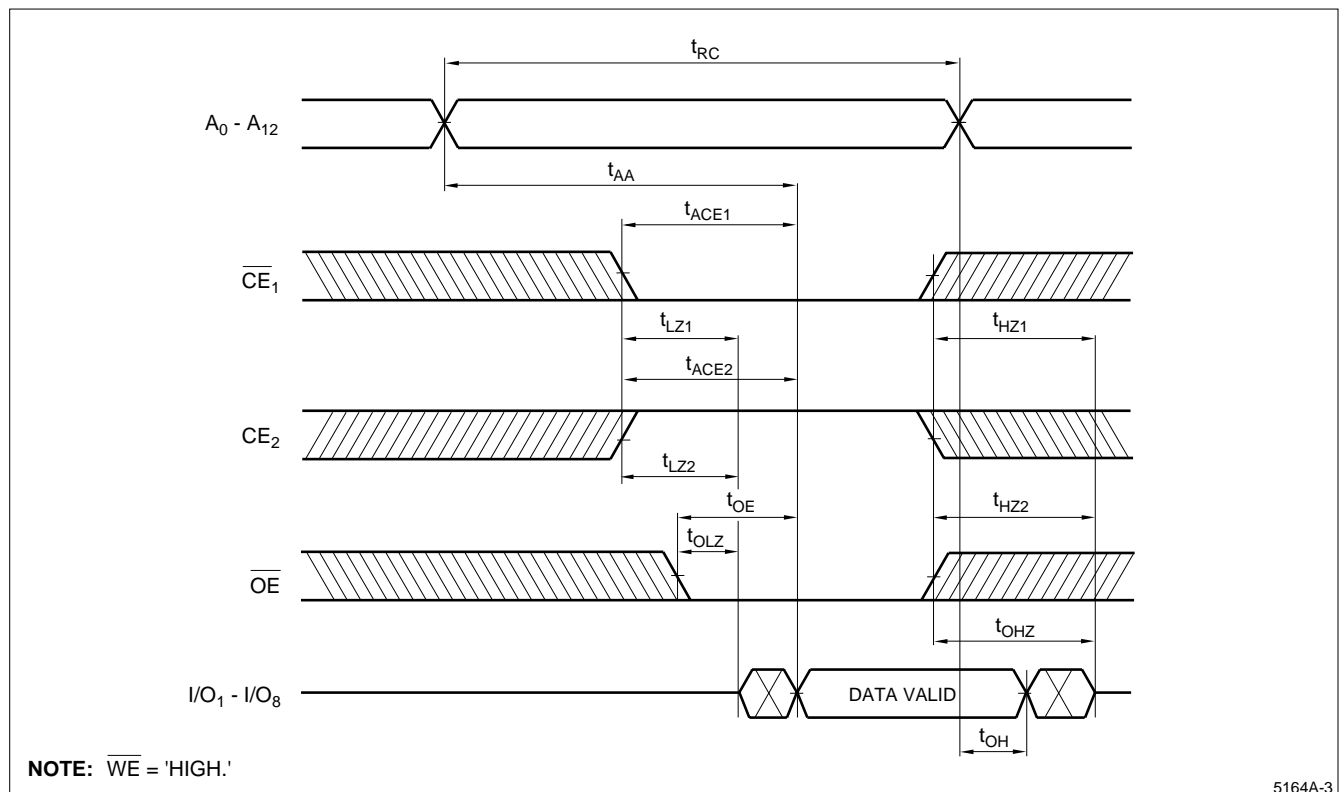
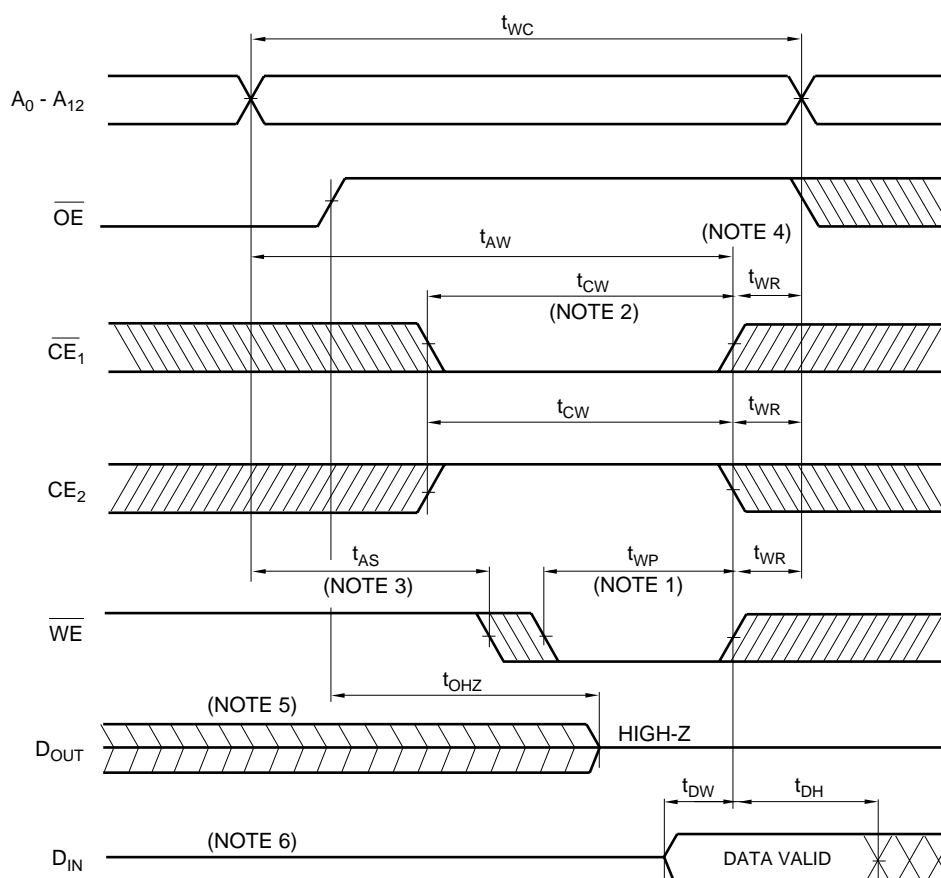


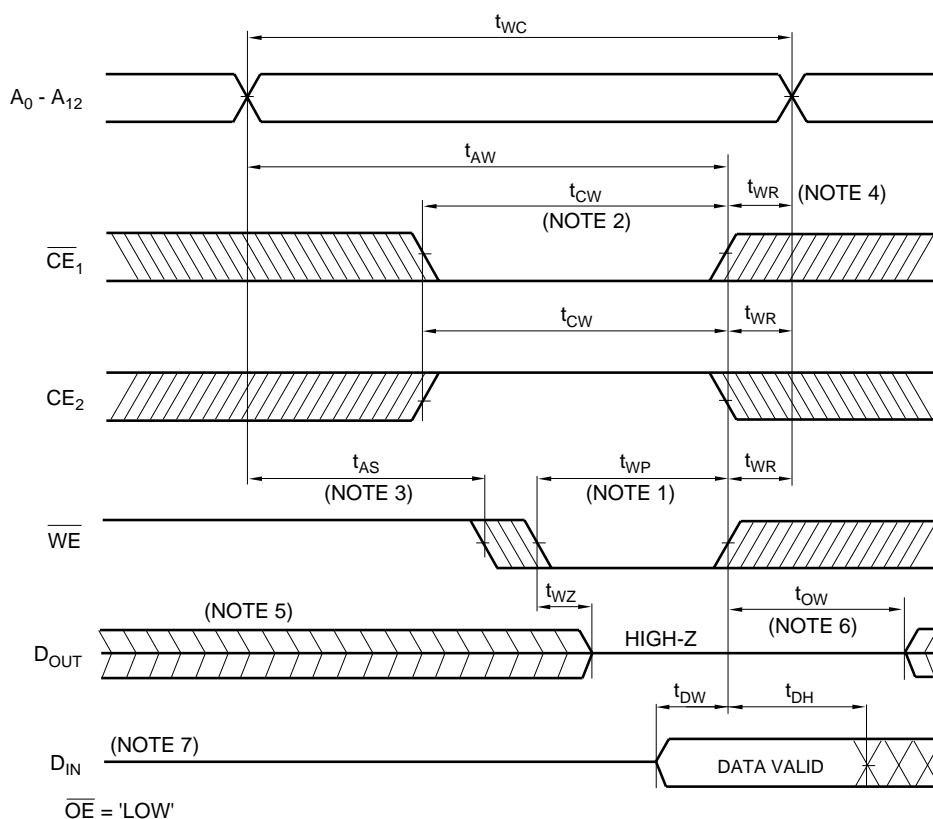
Figure 5. Read Cycle

**NOTES:**

1. The writing occurs during an overlapping period of  $\overline{CE_1}$  = 'LOW,'  $CE_2$  = 'HIGH,' and  $\overline{WE}$  = 'LOW' ( $t_{WP}$ ).
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE_1}$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.
5. If  $\overline{CE_1}$  LOW transition or  $CE_2$  HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the outputs will remain high-impedance.
6. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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**Figure 6. Write Cycle 1**

**NOTES:**

1. The writing occurs during an overlapping period of  $\overline{CE}_1$  = 'LOW,' CE<sub>2</sub> = 'HIGH,' and  $\overline{WE}$  = 'LOW' ( $t_{WP}$ ).
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or CE<sub>2</sub> HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.
5. If  $\overline{CE}_1$  LOW transition or CE<sub>2</sub> HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the outputs will remain high-impedance.
6. If  $\overline{CE}_1$  HIGH transition or CE<sub>2</sub> LOW transition occurs at the same time or before  $\overline{WE}$  HIGH transition, the outputs will remain high-impedance.
7. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

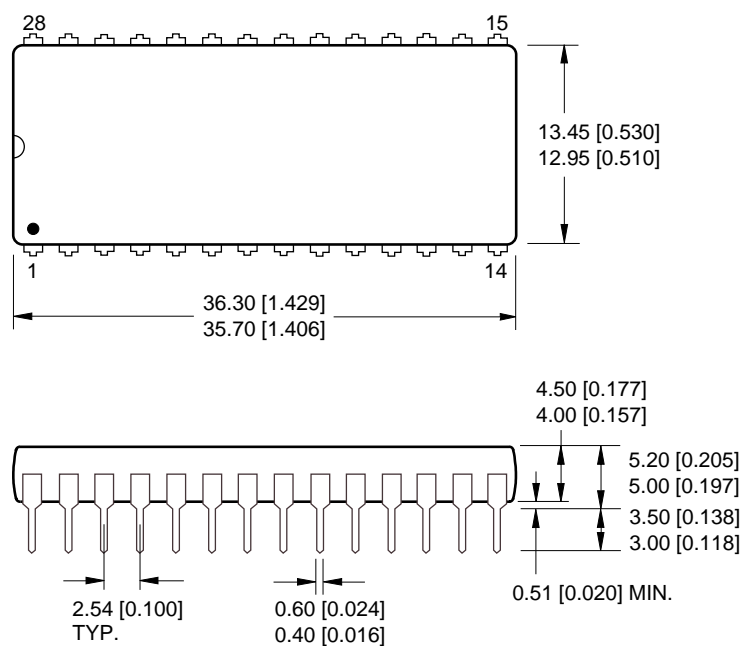
5164A-5

**Figure 7. Write Cycle 2**

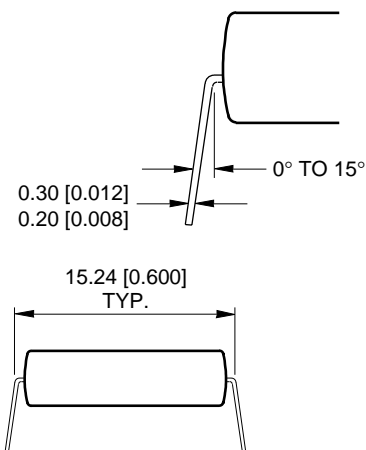


## PACKAGE DIAGRAMS

## 28DIP (DIP028-P-0600)



## DETAIL

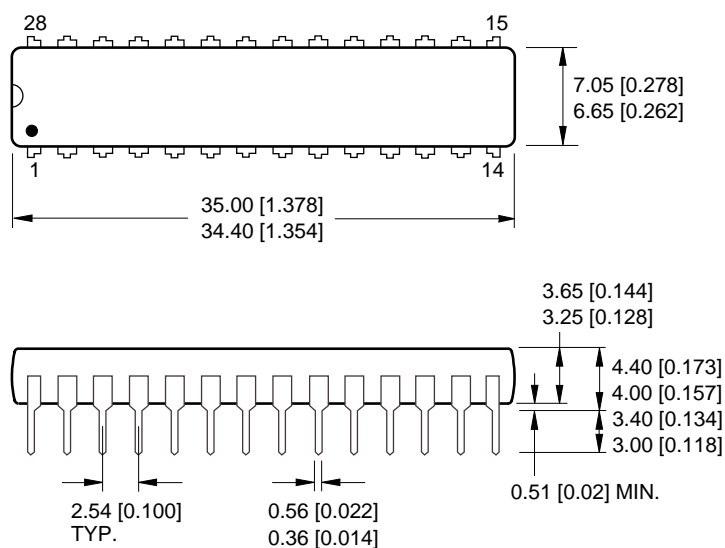


DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

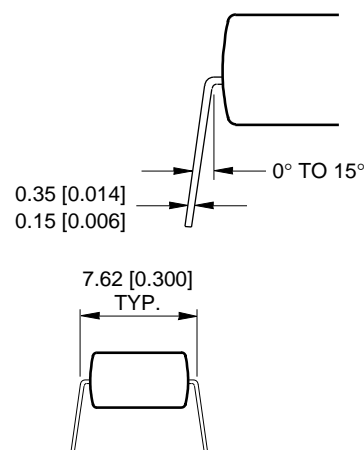
28DIP-2

## 28-pin, 600-mil DIP

## 28DIP (DIP028-P-0300)



## DETAIL

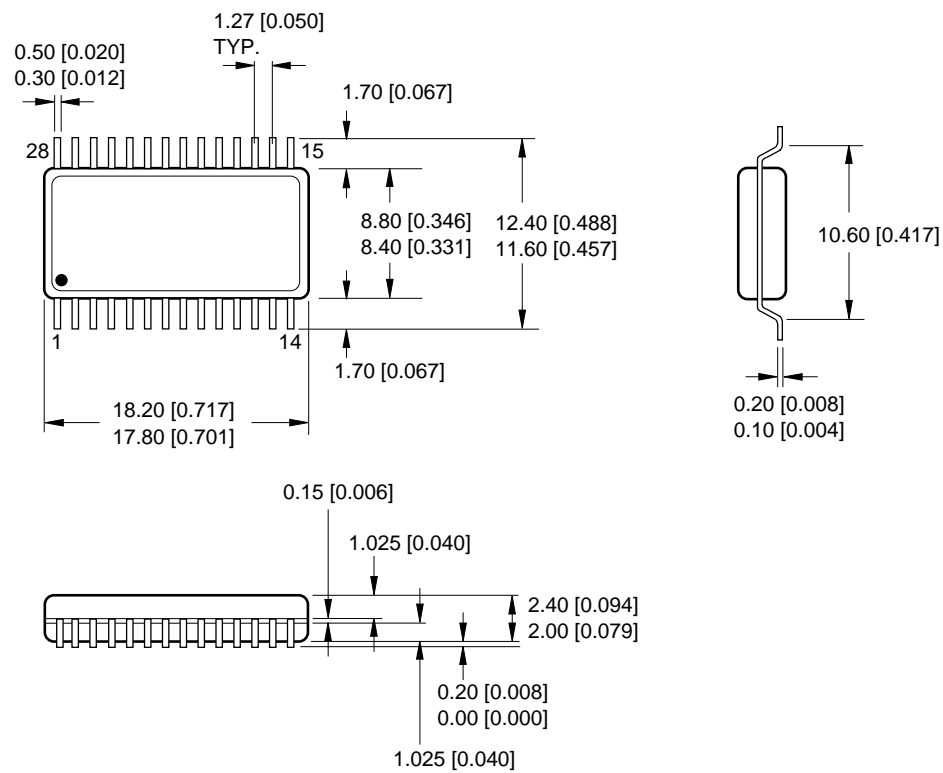


DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

28DIP-6

## 28-pin, 300-mil SK-DIP

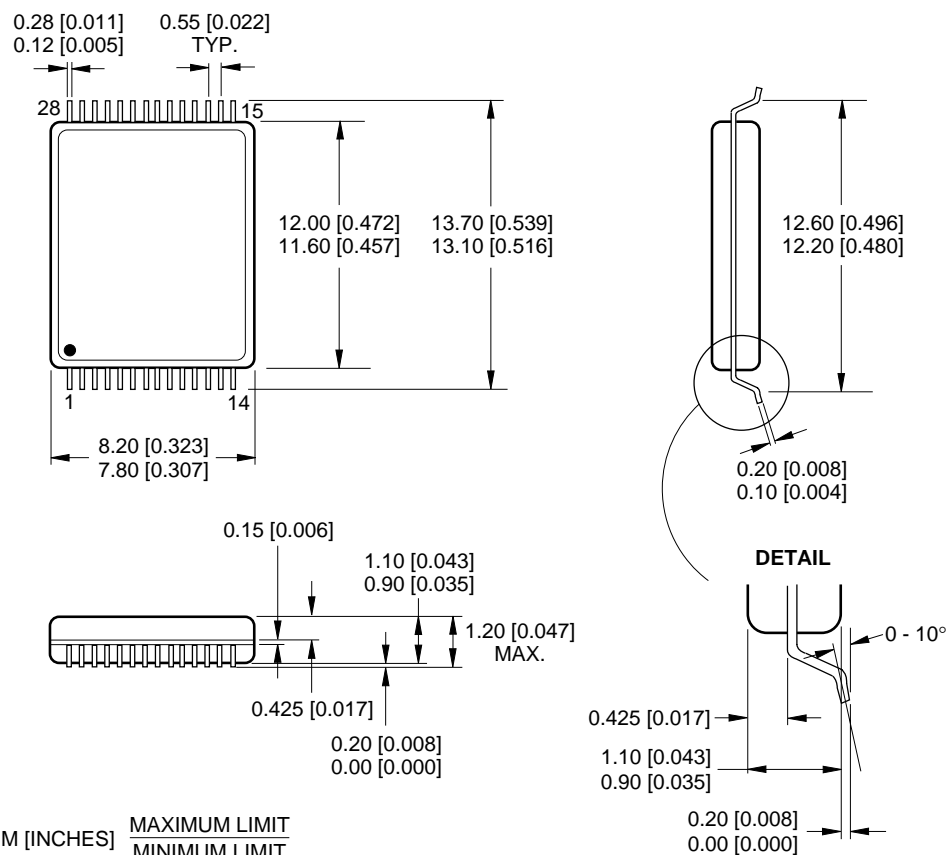
**28SOP (SOP028-P-0450)**



DIMENSIONS IN MM [INCHES]      MAXIMUM LIMIT  
MINIMUM LIMIT

28SOP

## 28-pin, 450-mil SOP

**28TSOP (TSOP028-P-0813)**

28TSOP

**28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)****ORDERING INFORMATION**

LH5164A	X	X	- ##	L
Device Type	Operating Temperature	Package	Speed	Power
				Low-power standby
				{ 10 100 80 80 Access Time (ns)
				{ Blank 28 pin, 600-mil DIP (DIP028-P-0600) D 28-pin, 300-mil SK-DIP (SK-DIP028-P-0300) N 28-pin, 450-mil SOP (SOP028-P-0450) T 28-pin, 8 x 13 mm <sup>2</sup> TSOP (Type I) (TSOP028-P-0813)
				{ Blank -10 to 70°C H -40 to +85°C
				CMOS 64K (8K x 8) Static RAM
<b>Example:</b> LH5164AD-10L (CMOS 64K (8K x 8) Static RAM, 100 ns, Low-power standby, 28-pin, 300-mil SK-DIP)				

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