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1. General Description

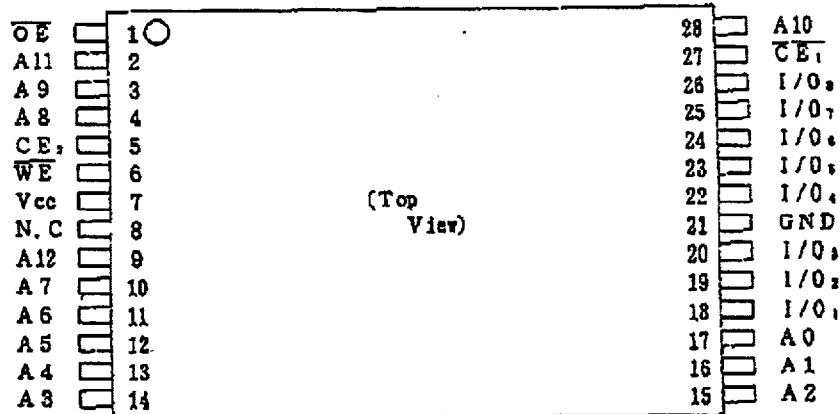
LH5168VT is a static RAM organized as 8,192 word \times 8 bit fabricated with a CMOS silicon gate process.

It's main features include:

Features

- Access time 200ns (MAX.)
- Current consumption
 - Operating 45mA (MAX.)
 - 10mA ($t_{\text{acc}}, t_{\text{wc}} = 1\mu\text{s}$)
 - Standby 1.0 μA (MAX.)
 - Data retention 0.2 μA ($V_{\text{cc}} = 3\text{V}$, $T_a = 25^\circ\text{C}$)
- Wide operating voltage range 2.7V ~ 5.5V
- Fully static operation
- All input/output TTL compatible
- Three-state output
- Not designed or rated as radiation hardened
- 28pin TSOP (TSOP28-P-0813) plastic package
- P-type bulk silicon
- Operating temperature is -10°C to 70°C

2. Pin Configuration



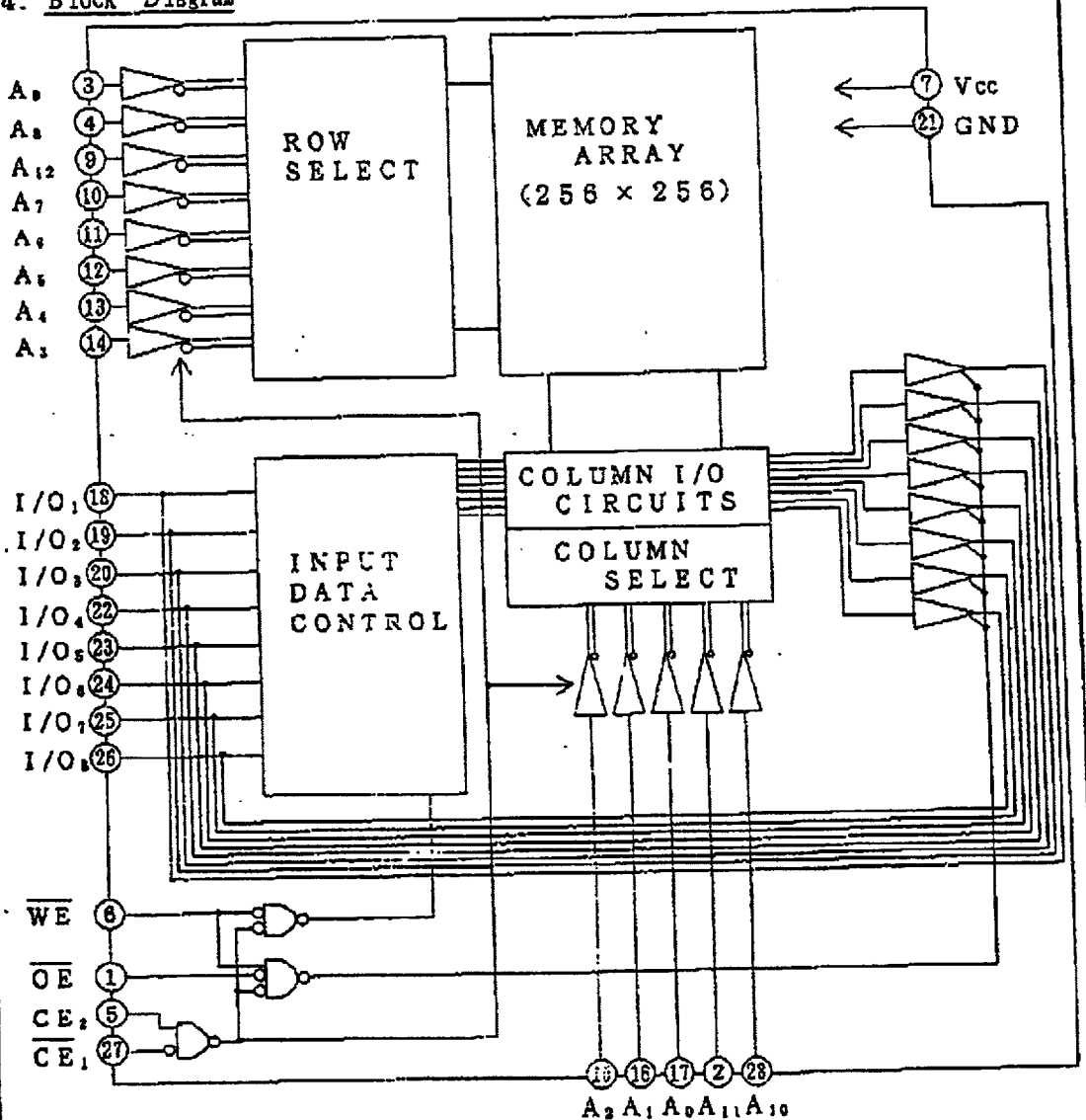
| Pin Name | Signal |
|--------------------------------------|-------------------|
| A ₀ to A ₁₂ | Address input |
| CE ₁ /CE ₂ | Chip enable |
| WE | Write enable |
| OE | Output enable |
| I/O ₀ to I/O ₇ | Data input/output |
| V _{cc} | Power supply |
| GND | Ground |
| N.C. | Non connection |

3. Operating Mode

| CE ₁ | CE ₂ | WE | OE | Mode | I/O ₁ to I/O ₈ | Supply current |
|-----------------|-----------------|----|----|----------------|--------------------------------------|------------------------------|
| H | * | * | * | Standby | High impedance | Standby (I _{ss}) |
| * | L | * | * | | | |
| L | H | L | * | Write | Data input | Operating (I _{cc}) |
| L | H | H | L | Read | Data output | Operating (I _{cc}) |
| L | H | H | H | Output disable | High impedance | Operating (I _{cc}) |

(* = H or L)

4. Block Diagram



5. Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|-----------------------|-----------|--------------------------|------|
| Supply voltage (*1) | V_{CC} | -0.3 to +7.0 | V |
| Input voltage (*1) | V_{IN} | -0.3(*2) to $V_{CC}+0.3$ | V |
| Operating temperature | T_{opr} | -10 to +70 | °C |
| Storage temperature | T_{stg} | -65 to +150 | °C |

Note) *1. Maximum applicable voltage on any pin with respect to GND.

*2. -3.0V for pulse widths ≤ 50ns.

6. Recommended DC Operating Conditions

($T_a = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------------|----------|--------------|------|--------------|------|
| Supply voltage | V_{CC} | 2.7 | | 5.5 | V |
| Input voltage | V_{IH} | $V_{CC}-0.5$ | | $V_{CC}+0.3$ | V |
| ($V_{CC}=2.7$ to 3.6V) | V_{IL} | -0.3(*3) | | 0.2 | V |
| Input voltage | V_{IH} | 2.2 | | $V_{CC}+0.3$ | V |
| ($V_{CC}=4.5$ to 5.5V) | V_{IL} | -0.3(*3) | | 0.8 | V |

Note) *3. -3.0V for pulse widths ≤ 50ns.

7. DC Electrical Characteristics

($T_a = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC}=2.7\text{V}$ to 5.5V)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|--------------------------|-----------|---|--------------------------------------|------|---------------|
| Input leakage current | I_{LI} | $V_{IN}=C\text{V to } V_{CC}$ | -1.0 | 1.0 | μA |
| Output leakage current | I_{LO} | $CE_1=V_{IH}$ or $CE_2=V_{IL}$ or $OE=V_{IH}$ or $WE=V_{IL}$ $V_{I/O}=0$ to V_{CC} | -1.0 | 1.0 | μA |
| Operating Supply current | I_{CC} | $CE_1=0.2\text{V}$, $V_{IN}=0.2\text{V}$ or $V_{CC}-0.2\text{V}$ $CE_2=V_{CC}-0.2\text{V}$, Output open, $V_{CC}=2.7\text{V to } 3.6\text{V}$ | t_{CYCLE} =200ns | 20 | μA |
| | | | t_{CYCLE} =1.0 μs | 8 | |
| | | $CE_1=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH} $CE_2=V_{IH}$, Output open, $V_{CC}=4.5\text{V to } 5.5\text{V}$ | t_{CYCLE} =200ns | 45 | |
| | | | t_{CYCLE} =1.0 μs | 10 | |
| Standby current | I_{SB} | $CE_2 \leq 0.2\text{V}$ or $CE_1 \geq V_{CC}-0.2\text{V}$ (*4) | $V_{CC}=2.7\text{V to } 3.6\text{V}$ | 0.6 | μA |
| | | | $V_{CC}=4.5\text{V to } 5.5\text{V}$ | 1.0 | |
| | I_{SB1} | $CE_1=V_{IN}$ or $CE_2=V_{IL}$ | | 5 | μA |
| Output voltage | V_{OL} | $I_{OL}=500\mu\text{A}$, $V_{CC}=2.7\text{V to } 3.6\text{V}$ | | 0.4 | V |
| | | $I_{OL}=2.1\text{mA}$, $V_{CC}=4.5\text{V to } 5.5\text{V}$ | | 0.4 | |
| | V_{OH} | $I_{OH}=-500\mu\text{A}$, $V_{CC}=2.7\text{V to } 3.6\text{V}$ | $V_{CC}-0.5$ | | V |
| | | $I_{OH}=-1.0\text{mA}$, $V_{CC}=4.5\text{V to } 5.5\text{V}$ | 2.4 | | |

Note) *4. CE_2 should be $\geq V_{CC}-0.2\text{V}$ or $\leq 0.2\text{V}$.

8. AC Electrical Characteristics

Test Condition of AC Characteristics

| | |
|---------------------------|------------------------------|
| Input pulse level | 0.2V to $V_{CC}-0.2\text{V}$ |
| Input rise/fall time | 10ns |
| Input/Output timing level | 1.5V |
| Output load | C_L (100pF) (*5) |

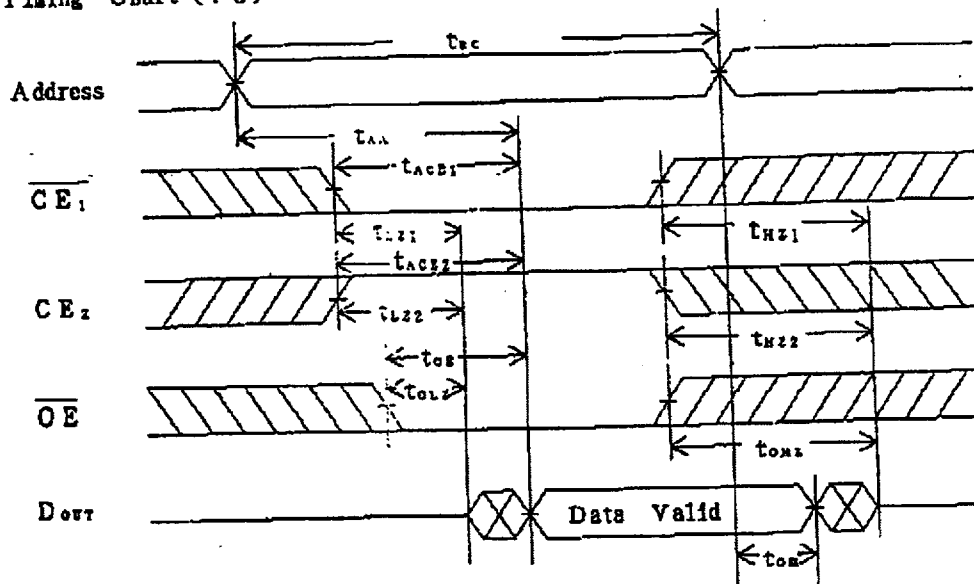
Note) *5. Including scope and jig capacitance.

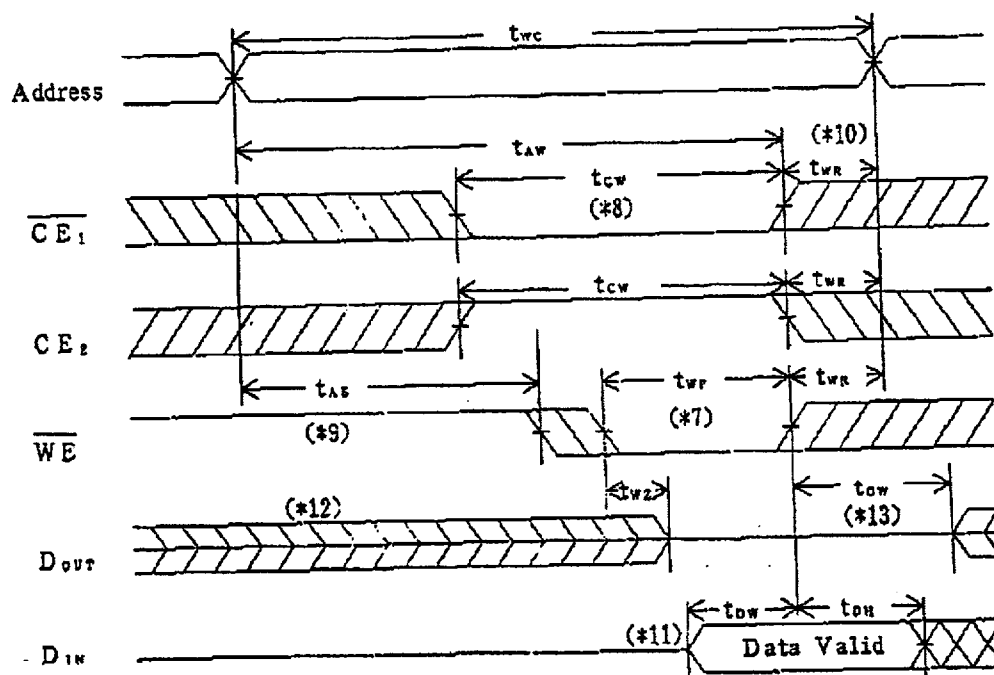
Read cycle

(T_a = -10°C to +70°C, V_{cc} = 2.7 V to 5.5 V)

| Parameter | Symbol | Min. | Max. | Unit |
|--|-------------------|------|------|------|
| Read cycle time | t _{RC} | 200 | | ns |
| Address access time | t _{AA} | | 200 | ns |
| CE ₁ access time | t _{ACE1} | | 200 | ns |
| CE ₂ access time | t _{ACE2} | | 200 | ns |
| Output enable access time | t _{OE} | | 150 | ns |
| Output hold time | t _{OH} | 10 | | ns |
| CE ₁ Low to output in Low impedance | t _{EL1} | 20 | | ns |
| CE ₂ High to output in Low impedance | t _{EL2} | 20 | | ns |
| OE Low to output in Low impedance | t _{OL} | 10 | | ns |
| CE ₁ high to output in High impedance | t _{EH1} | 0 | 60 | ns |
| CE ₂ Low to output in High impedance | t _{EH2} | 0 | 60 | ns |
| OE High to output in High impedance | t _{EH} | 0 | 40 | ns |

Timing Chart (*6)

Note)*6. \overline{WE} is 'High' level during the read cycle.

Timing Chart - (\overline{OE} Low fixed)

- Note)* 7. The writing occurs during a overlapping period of \overline{CE}_1 = 'Low', \overline{CE}_2 = 'High' and \overline{WE} = 'Low' (t_{wr}).
- * 8. t_{cw} is defined as the time from the last occurring transition, either \overline{CE}_1 Low transition or \overline{CE}_2 High transition, to the time when the writing is finished.
 - * 9. t_{as} is defined as the time from address change to writing start.
 - * 10. t_{wr} is defined as the time from writing finish to address change.
 - * 11. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.
 - * 12. If \overline{CE}_1 Low transition or \overline{CE}_2 High transition occurs at the same time or after \overline{WE} Low transition, the outputs will remain High impedance.
 - * 13. If \overline{CE}_1 High transition or \overline{CE}_2 Low transition occurs at the same time or before \overline{WE} High transition, the outputs will remain High impedance.

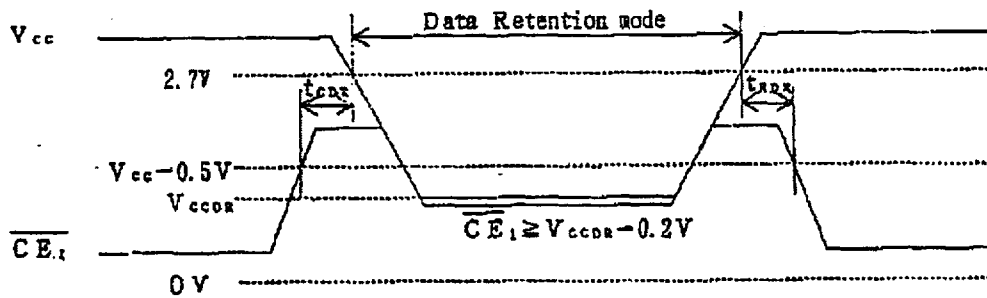
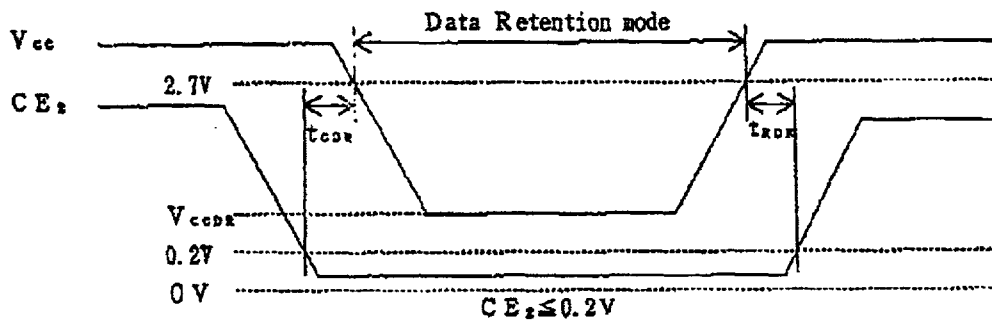
9. Data Retention Characteristics

(Ta = -10°C to +70°C)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|-------------------------------|------------|---|-------------------|-------------------|---------|
| Data Retention supply voltage | V_{CCD2} | $CE_2 \leq 0.2V$ or $CE_1 \geq V_{CCD2} - 0.2V$ (*14) | 2.0 | | V |
| Data Retention supply current | I_{CCD2} | $V_{CCD2} = 3V$ $CE_2 \leq 0.2V$ or $CE_1 \geq V_{CCD2} - 0.2V$ (*14) | | 0.2 0.4 0.6 | μA |
| Chip enable setup time | t_{CD2} | | 0 | | ns |
| Chip enable hold time | t_{HD2} | | (*15) t_{RC} | | ns |

Note)*14. $CE_2 \geq V_{CCD2} - 0.2V$ or $CE_2 \leq 0.2V$

*15. Read cycle time

Timing Chart-[$\overline{CE_1}$ Controlled] (*16)Timing Chart-[CE_2 Controlled]

Note)*16. To control the data retention mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCD2} and $V_{CCD2} - 0.2V$ or $0V$ and $0.2V$ during the data retention mode.

10. Pin Capacitance

(Ta=25°C, f=1MHz)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit | |
|-------------------|------------------|-----------------------|------|------|------|------|-----|
| Input capacitance | C _{ix} | V _{ix} = 0V | | | 7 | pF | *17 |
| I/O capacitance | C _{i/o} | V _{i/o} = 0V | | | 10 | pF | *17 |

Note)*17. This parameter is sample and not 100% tested.

11 Package and packing specification

1. Package Outline Specification

Refer to drawing No. AA1068

2. Markings

2-1. Marking contents

(1) Product name : LH5168VT

(2) Company name : SHARP

(3) Date code

(Example) YY WW XXX

Indicates the product was manufactured in the WWth week of 19YY.

Denotes the production ref. code(1-3)

Denotes the production week. (01,02,03, . . . - 52,53)

Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2-2. Marking layout

Refer drawing No. AA1068

(This layout do not define the dimensions of marking character and marking position.)

3. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

3-1. Soldering conditions(The following conditions are valid only for one time soldering.)

| Mounting Method | Temperature and Duration | Measurement Point |
|-----------------------------------|---|-----------------------|
| Reflow soldering (air) | Peak temperature of 240°C, duration less than 15 seconds above 230°C, temperature increase rate of 1~4°C/second | IC surface |
| Manual soldering (soldering iron) | 260°C or less, duration less than 10 seconds | IC outer lead surface |

3-2. Conditions for removal of residual flux

- (1) Ultrasonic washing power : 25 Watts/liter or less
- (2) Washing time : Total 1 minute maximum
- (3) Solvent temperature : 15~40°C

| | | | | | |
|--------------|-----------|-----------------|------------------|------------------|-------------------------|
| ISSUE DATE | '94.07.29 | <i>T. Maeda</i> | <i>Y. Uchida</i> | <i>M. Uchida</i> | (NOTE) |
| ISSUE NUMBER | R40729-27 | | | | |
| S/C NUMBER | LH5168V2 | | | | (DOCUMENT No: 1068-EDE) |

4. Packing Specification (Embossed Carrier Taping Specification)

This standard apply to the embossed carrier taping specification for ICs to be delivered from SHARP CORPORATION. SHARP's embossed carrier taping specification are generally based on those set forth by the Japanese Industrial Standard JIS C 0806 and the EIA481A.

4-1. Tape Structure

- Embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and covered with a top covering tape to enclose them.

4-2. Taping Reel and Embossed Carrier Tape Size

- For the taping reel and embossed carrier tape sizes, refer to the attached drawings (NO. CV674 and CV521)

4-3. IC Package Enclosure in Embossed Carrier Tape

- The IC package enclosure direction in the embossed portion as it compares to the direction in which the tape is pulled is indicated by an index mark on package (Index mark indicate the NO.1 pin on package) in the attached drawing (NO. CV522).

4-4. Missing IC Packages inside Embossed Carrier Tape

- The number of missing IC packages inside the embossed carrier tape should not exceed 0.1% of the total enclosed in the tape per reel, or 1, whichever may be larger. There should never be more than two consecutive missing IC package.

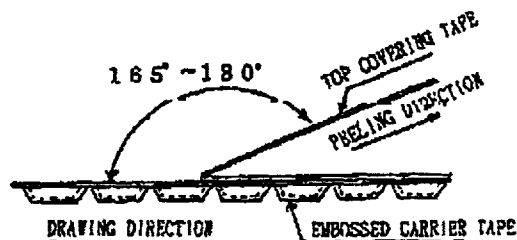
4-5. Tape Joints

- The embossed carrier tape should not have more than one joint per reel.

4-6. Peeling Strength of the Top Covering Tape

- Peeling strength must meet the following conditions.

- 1) Peeling angle
at 165° to 180°
- 2) Peeling speed
at 300mm/min.
- 3) Peeling strength
at 0.2 to 0.7N(20 to 70gf)



4-7. Packing

- The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, shall be held in place with paper adhesive tape exceeding 30mm in length.
- The leading and trailing edges of the embossed carrier tape shall be left empty (with embossed portions not filled with IC packages), in the attached drawing (MO. CV522).
- The number of IC packages enclosed in the embossed carrier tape per reel shall, in principle, be as listed below.

| Package Type | Number of IC Packages/Reel |
|---------------|----------------------------|
| SOP14-P-225 | 2,500 pcs |
| SOP16-P-225 | 2,500 pcs |
| SOP24-P-450 | 1,500 pcs |
| SOP28-P-450 | 1,000 pcs |
| SOP32-P-525 | 1,000 pcs |
| SOP44-P-800 | 750 pcs |
| TSOP28-P-1218 | 1,000 pcs |

4-8. Indications

- The following shall be indicated on the taping reel and the packing case.
 - 1) Part Number (Product Name)
 - 2) Storage Quantity
 - 3) Production Date
 - 4) Manufacture's Name (SHARP)

4-9. Protection While in Transit

Embossed carrier tape should be free from deformed IC leads and deterioration in electrical characteristics.

5. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages. Please conform to the following conditions concerning the storage and opening of dry packing.

5-1. Store under conditions shown below before opening the dry packing

- (1) Temperature range : 5~40°C
 (2) Humidity : 80% RH or less

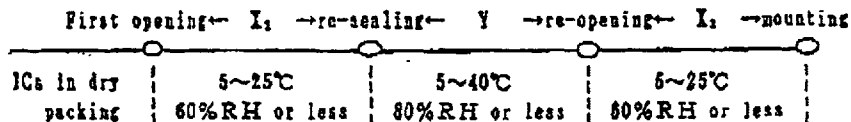
5-2. Notes on opening the dry packing

Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.

5-3. Storage after opening the dry packing

Perform the following to prevent absorption of moisture after opening.

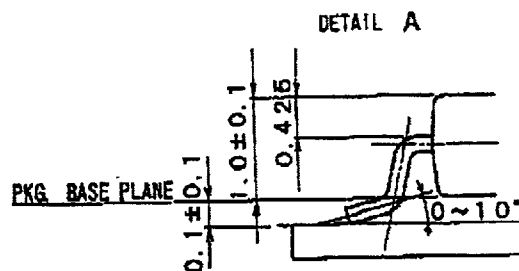
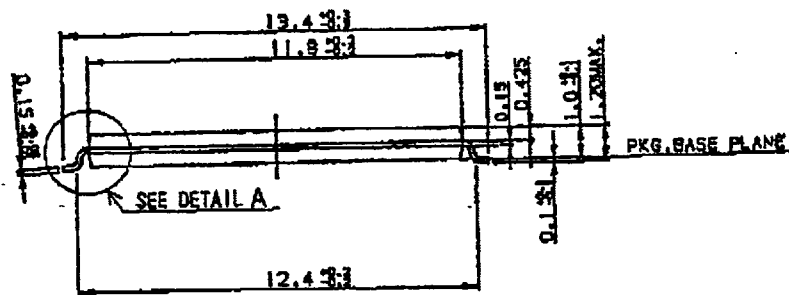
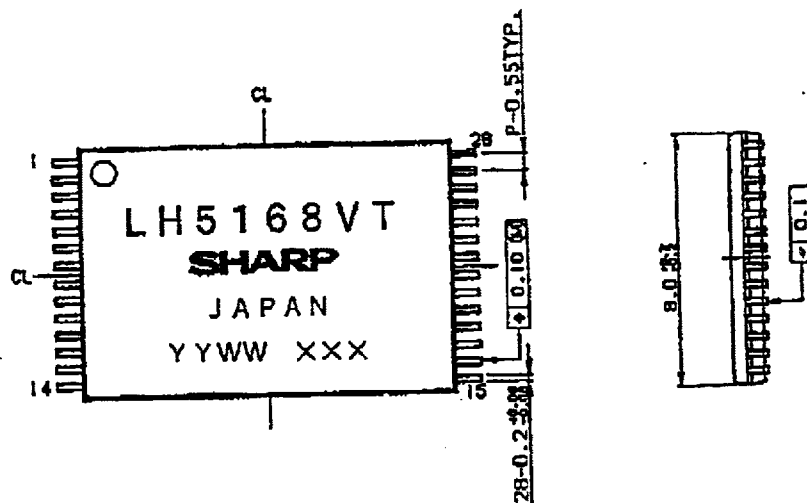
- (1) After opening the dry packing, store the ICs in an environment with a temperature of 5~25°C and a relative humidity of 60% or less and mount ICs within 3 days after opening dry packing.
 (2) To re-store the ICs for an extended period of time within 3 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whose indicator is blue), and store in an environment with a temperature of 5~40°C and a relative humidity of 80% or less, and mount ICs within 2 weeks.
 (3) Total period of storage after first opening and re-opening is within 3 days, and store the ICs in the same environment as section 5-3.(1).



X₁+X₂ : within 3 days
 Y : within 2 weeks

5-4. Baking (drying) before mounting

- (1) Baking is necessary
 (A) If the humidity indicator in the desiccant becomes pink
 (B) If the procedure in section 5-3 could not be performed
 (2) Recommended baking conditions
 If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16~24 hours at 120°C or 5~10 hours at 150°C. Note that the embossed carrier tape can not be baked at the above temperature. Please transfer ICs to heat resistant carrier.
 (3) Storage after baking
 After baking ICs, store the ICs in the same environment as section 5-3.(1).

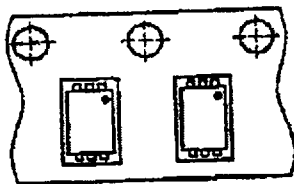


| | | | | | |
|----------------------|-------------|-------------|---------|------|--|
| 名称 | リード仕上 | TIN-LEAD | 単位 | 備考 | プラスチックパッケージは、 バリを除去する。 |
| NAME TSOP28-P-0813 | LEAD FINISH | PLATING | UNIT mm | NOTE | Plastic body dimensions do not include burr of resin. |
| シャープ株式会社 | IC事業本部 | | | | |
| SHARP CORP. IC GROUP | | DRAWING NO. | AA1068 | | |

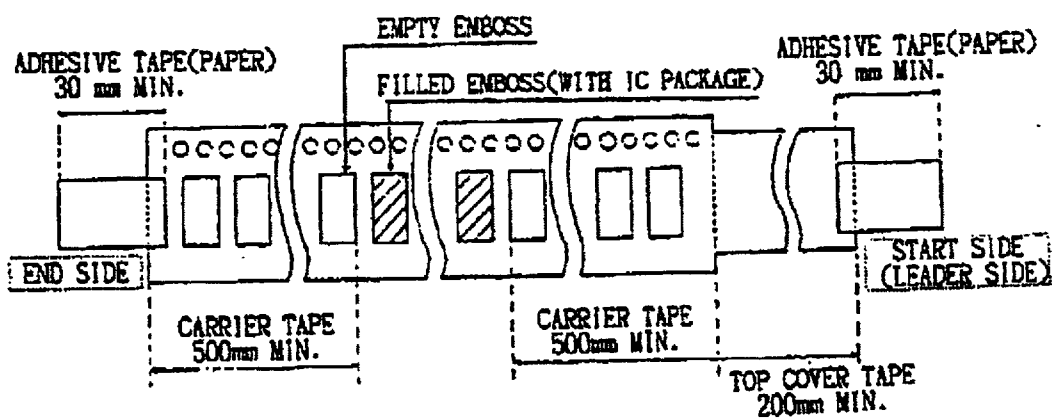
EMBOSS TAPING TYPE

IC TAPING DIRECTION

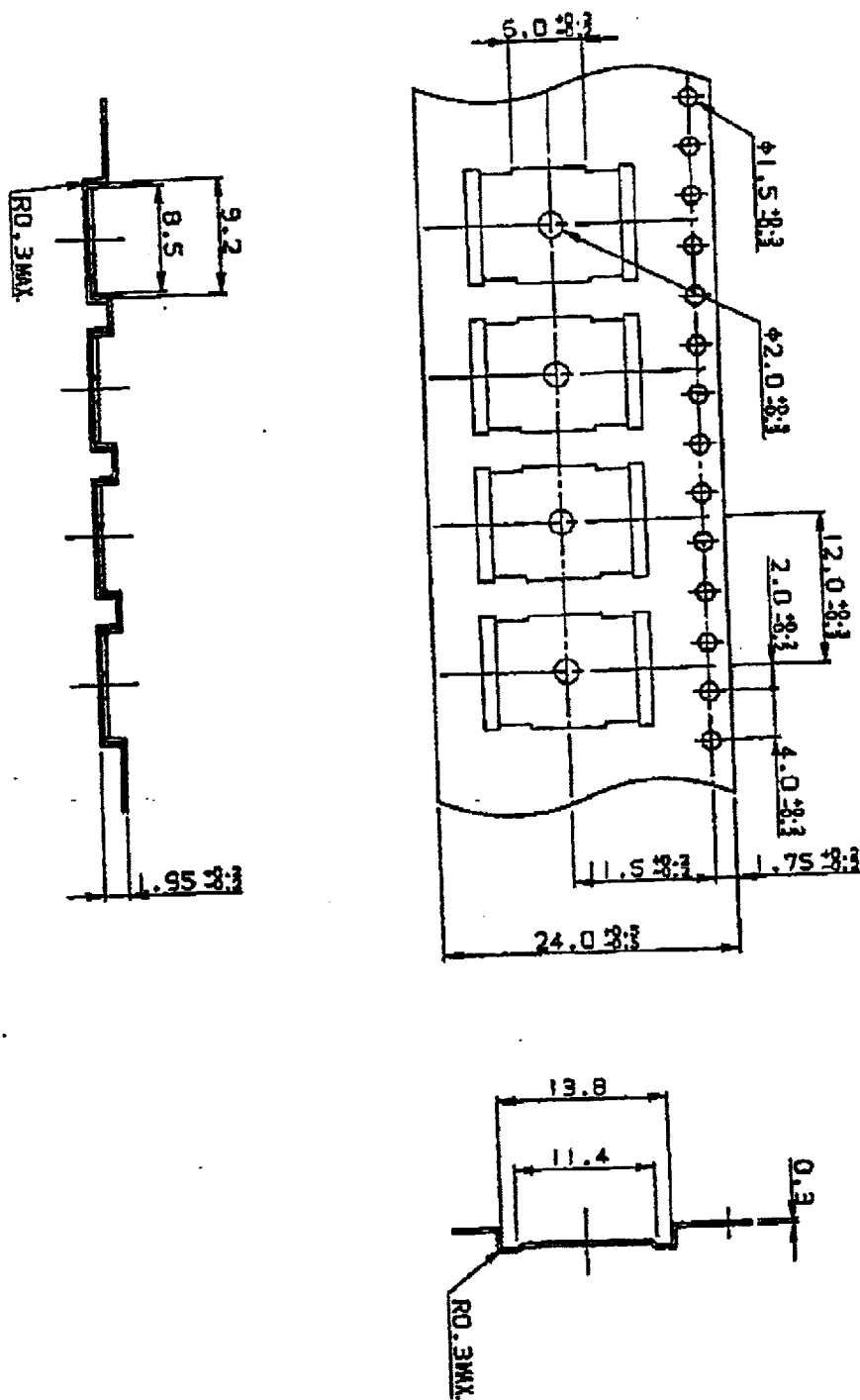
THE DRAWING DIRECTION OF TAPE



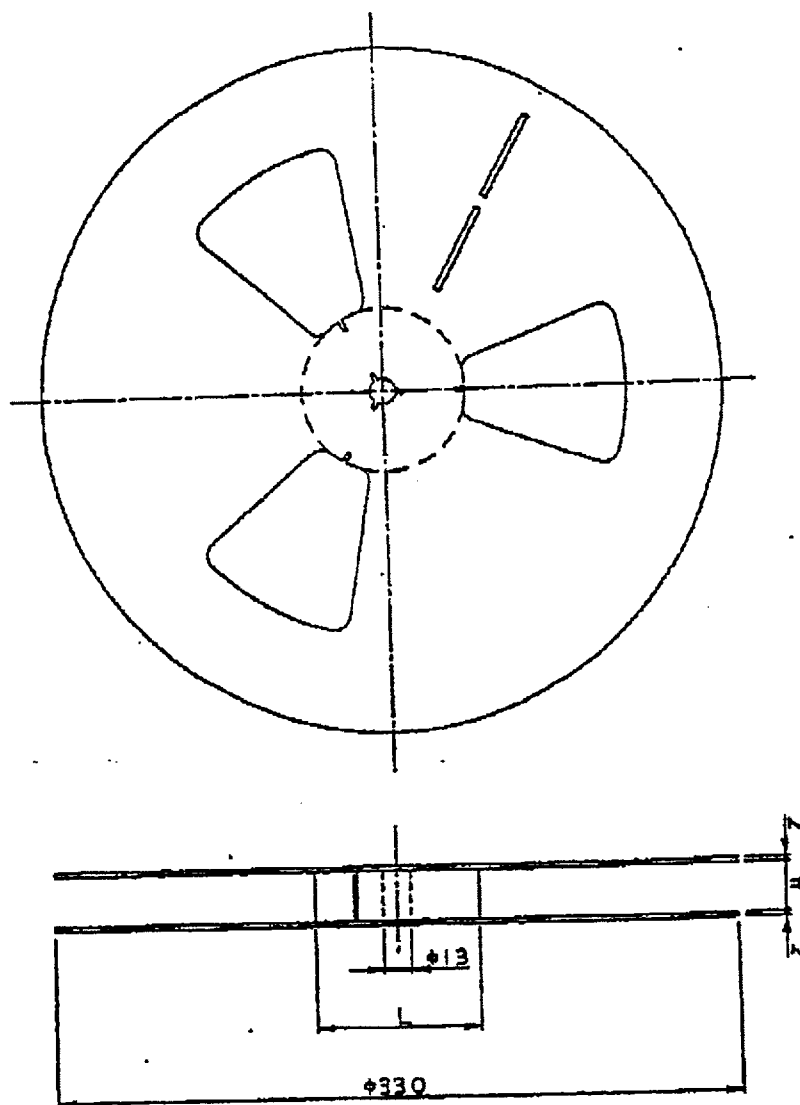
LEADER SIDE AND END SIDE OF TAPE



| | | | | |
|-------------|--------------------|-------------|-------|------------|
| 名称 NAME | EMBOSS TAPING TYPE | 単位 UNIT | mm | 備考 NOTE |
| シャープ株式会社 | IC事業本部 | | | |
| SHARP CORP. | IC GROUP | DRAWING NO. | CV522 | |



| | | | | |
|----------------------|---------------|-------------|----|-------|
| 名称 | EC28-0813T3PS | 単位 | mm | 備考 |
| NAME | | UNIT | | NOTE |
| シャープ株式会社 IC事業本部 | | DRAWING NO. | | CV874 |
| SHARP CORP. IC GROUP | | | | |



| PKG | W (mm) | L (mm) | REEL NUMBER |
|---------------|--------|--------|-------------|
| SOP14-P-225 | 16.4 | φ 80 | ECR16 |
| SOP16-P-225 | " | " | " |
| SOP24-P-450 | 24.4 | " | ECR24 |
| SOP28-P-450 | " | " | " |
| SOP32-P-525 | 32.4 | φ 100 | ECR32 |
| SOP44-P-500 | 44.8 | φ 100 | ECR44-M |
| TSOP28-P-0818 | 24.4 | φ 100 | ECR24-100 |

| | | |
|-------------------------------------|-------------------|------|
| 名称 | 単位 | 備考 |
| NAME REEL FOR BUBOSS CARRIER TAPING | UNIT mm | NOTE |
| シャープ株式会社 IC事業本部 | | |
| SHARP CORP. IC GROUP | DRAWING NO. CV521 | |

