

# LH532000B

CMOS 2M (256K × 8/128K × 16) MROM

## FEATURES

- 262,144 words × 8 bit organization  
(Byte mode)  
131,072 words × 16 bit organization  
(Word mode)
- $\overline{\text{BYTE}}$  input pin selects bit configuration
- Access times: 120/150 ns (MAX.)
- Low-power consumption:  
Operating: 275 mW (MAX.)  
Standby: 550  $\mu\text{W}$  (MAX.)
- Programmable  $\text{OE}/\overline{\text{OE}}$  and  $\text{OE}_1/\overline{\text{OE}}_1/\text{DC}$
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  - 40-pin, 600-mil DIP
  - 40-pin, 525-mil SOP
  - 48-pin,  $12 \times 18 \text{ mm}^2$  TSOP (Type I)
- ×16 word-wide pinout

## DESCRIPTION

The LH532000B is a 2M-bit mask-programmable ROM with two programmable memory organizations, byte and word modes. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

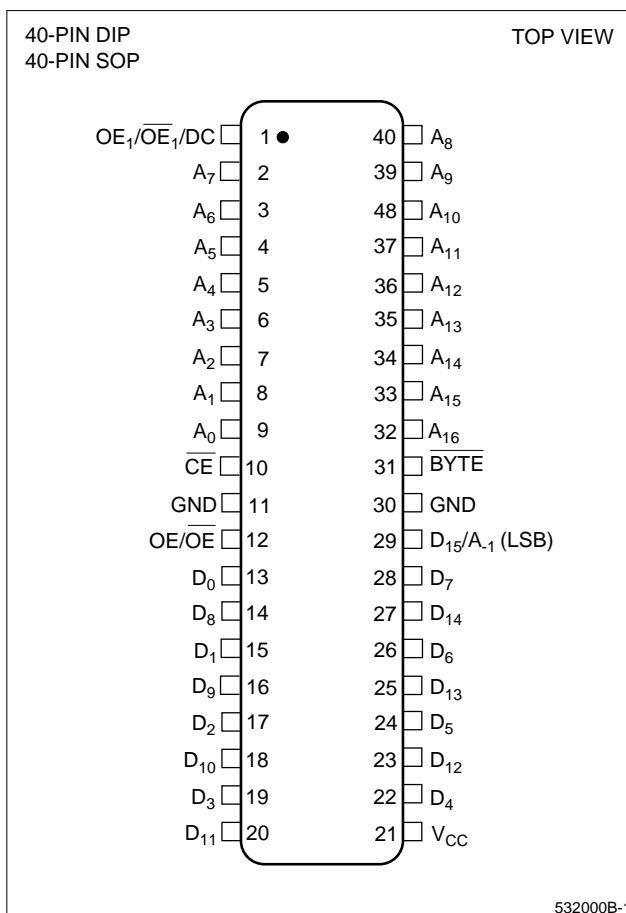


Figure 1. Pin Connections for DIP and SOP Packages

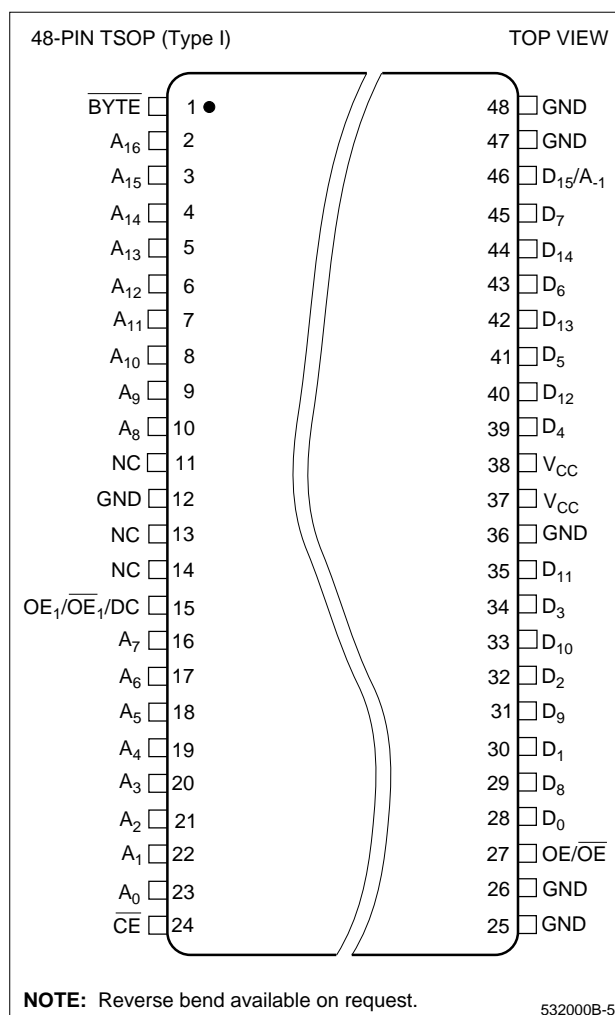
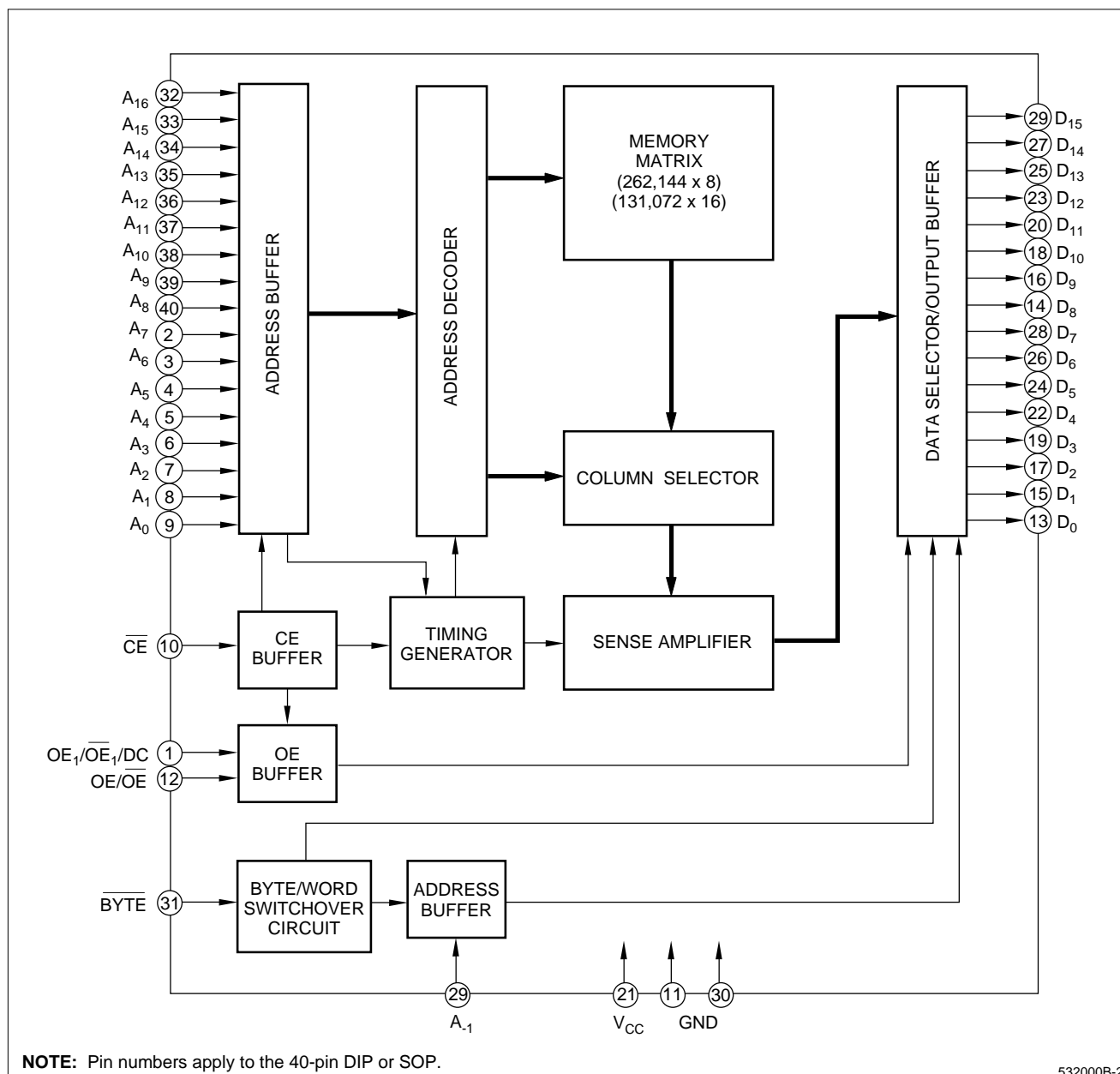


Figure 2. Pin Connections for TSOP Package



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Figure 3. LH532000B Block Diagram

## PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A <sub>-1</sub>	Address input (BYTE mode)	1
A <sub>0</sub> – A <sub>16</sub>	Address input	
D <sub>0</sub> – D <sub>15</sub>	Data output	1
CE	Chip enable input	
OE/OE	Output enable input	2

SIGNAL	PIN NAME	NOTE
OE <sub>1</sub> /OE <sub>1</sub> /DC	Output enable input or Don't care	2
BYTE	Byte/word mode switch	
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

### NOTES:

- D<sub>15</sub>/A<sub>-1</sub> pin becomes LSB address input (A<sub>-1</sub>) when the bit configuration is set in byte mode, and data output (D<sub>15</sub>) when in word mode. BYTE input pin selects bit configuration.
- The active levels of OE/OE and OE<sub>1</sub>/OE<sub>1</sub>/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

## TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}$	$OE_1/\overline{OE}_1$	$\overline{BYTE}$	$A_{-1}$ ( $D_{15}$ )	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	—	—	Standby ( $I_{SB}$ )
L	L/H	X	X	X	High-Z	High-Z	—	—	Operating ( $I_{CC}$ )
L	X	L/H	X	X	High-Z	High-Z	—	—	Operating ( $I_{CC}$ )
L	H/L	H/L	H	Input inhibit	$D_0 - D_7$	$D_8 - D_{15}$	$A_0$	$A_{16}$	Operating ( $I_{CC}$ )
L	H/L	H/L	L	L	$D_0 - D_7$	High-Z	$A_{-1}$	$A_{16}$	Operating ( $I_{CC}$ )
L	H/L	H/L	L	H	$D_8 - D_{15}$	High-Z	$A_{-1}$	$A_{16}$	Operating ( $I_{CC}$ )

## NOTE:

1. X = H or L, High-Z = High-impedance.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	$V_{CC}$	-0.3 to +7.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	V
Output voltage	$V_{OUT}$	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ( $T_A = 0$  to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V

DC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0$  to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	$V_{IL}$		-0.3		0.8	V	
Input 'High' voltage	$V_{IH}$		2.2		$V_{CC} + 0.3$	V	
Output 'Low' voltage	$V_{OL}$	$I_{OL} = 2.0\text{ mA}$			0.4	V	
Output 'High' voltage	$V_{OH}$	$I_{OH} = -400\text{ }\mu\text{A}$	2.4			V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{CC}$			10	$\mu\text{A}$	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$			10	$\mu\text{A}$	1
Operating current	$I_{CC1}$	$t_{RC} = t_{RC}(\text{MIN.})$			50	mA	2
	$I_{CC2}$	$t_{RC} = 1\text{ }\mu\text{s}$			45		
	$I_{CC3}$	$t_{RC} = t_{RC}(\text{MIN.})$			45	mA	3
	$I_{CC4}$	$t_{RC} = 1\text{ }\mu\text{s}$			40		
Standby current	$I_{SB1}$	$CE = V_{IH}$			3	mA	
	$I_{SB2}$	$CE = V_{CC} - 0.2\text{ V}$			100		
Input capacitance	$C_{IN}$	$f = 1\text{ MHz}$			10	pF	
Output capacitance	$C_{OUT}$	$T_A = 25^\circ\text{C}$			10	pF	

## NOTES:

- $OE/\overline{OE}_1 = V_{IL}$ ,  $CE/\overline{OE}/\overline{OE}_1 = V_{IH}$
- $V_{IN} = V_{IH}$  or  $V_{IL}$ ,  $CE = V_{IL}$ , outputs open
- $V_{IN} = (V_{CC} - 0.2\text{ V})$  or  $0.2\text{ V}$ ,  $CE = 0.2\text{ V}$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to }+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	120 ns		150 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	$t_{RC}$	120		150		ns	
Address access time	$t_{AA}$		120		150	ns	
Chip enable access time	$t_{ACE}$		120		150	ns	
Output enable delay time	$t_{OE}$		55		70	ns	
Output hold time	$t_{OH}$	5		10		ns	
CE to output in High-Z	$t_{CHZ}$		55		70	ns	1
OE to output in High-Z	$t_{OHZ}$		55		70	ns	

**NOTE:**

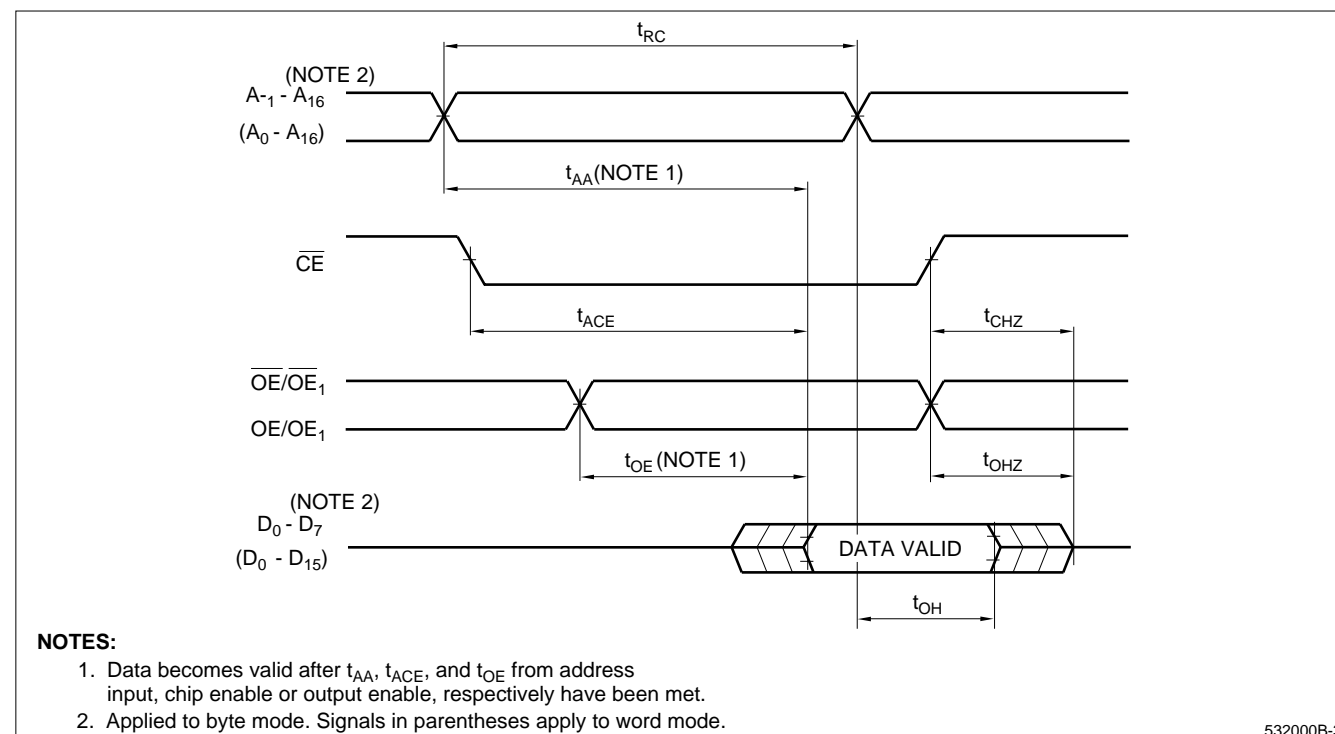
1. This is the time required for the output to become high-impedance.

**AC TEST CONDITIONS**

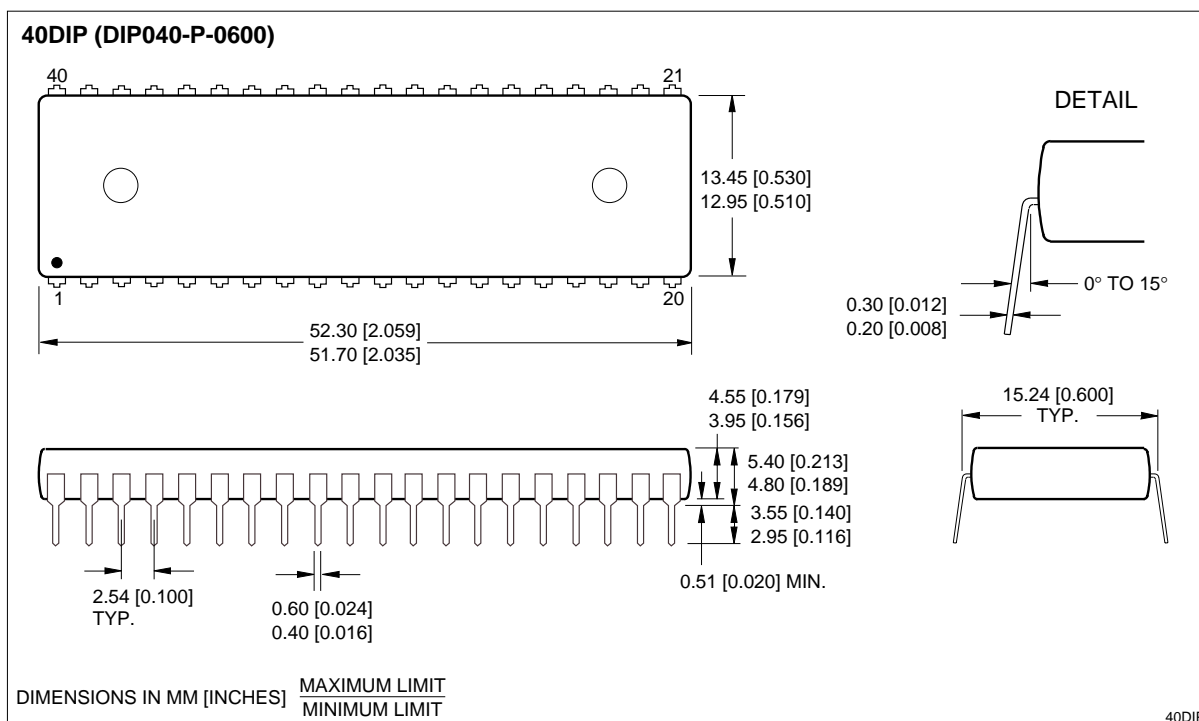
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

**CAUTION**

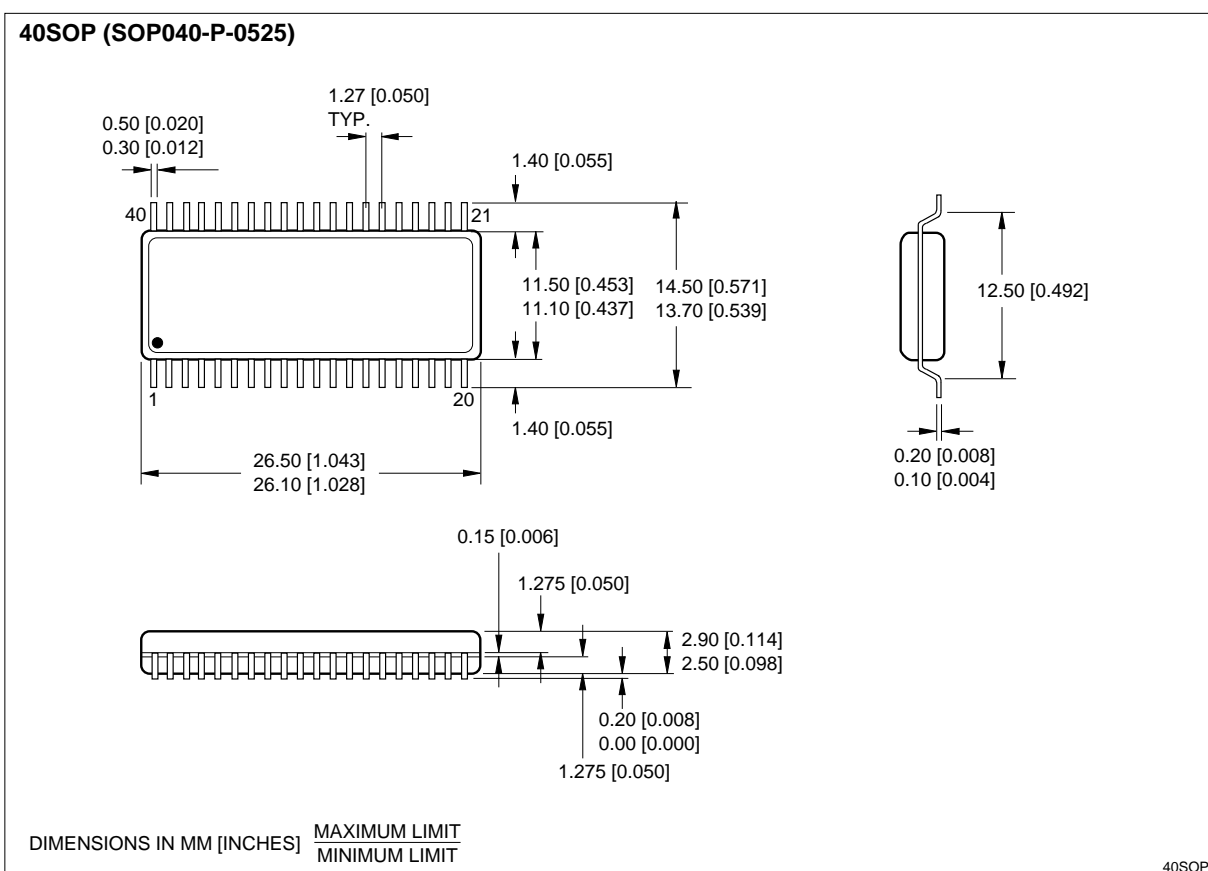
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.

**Figure 4. Timing Diagram**

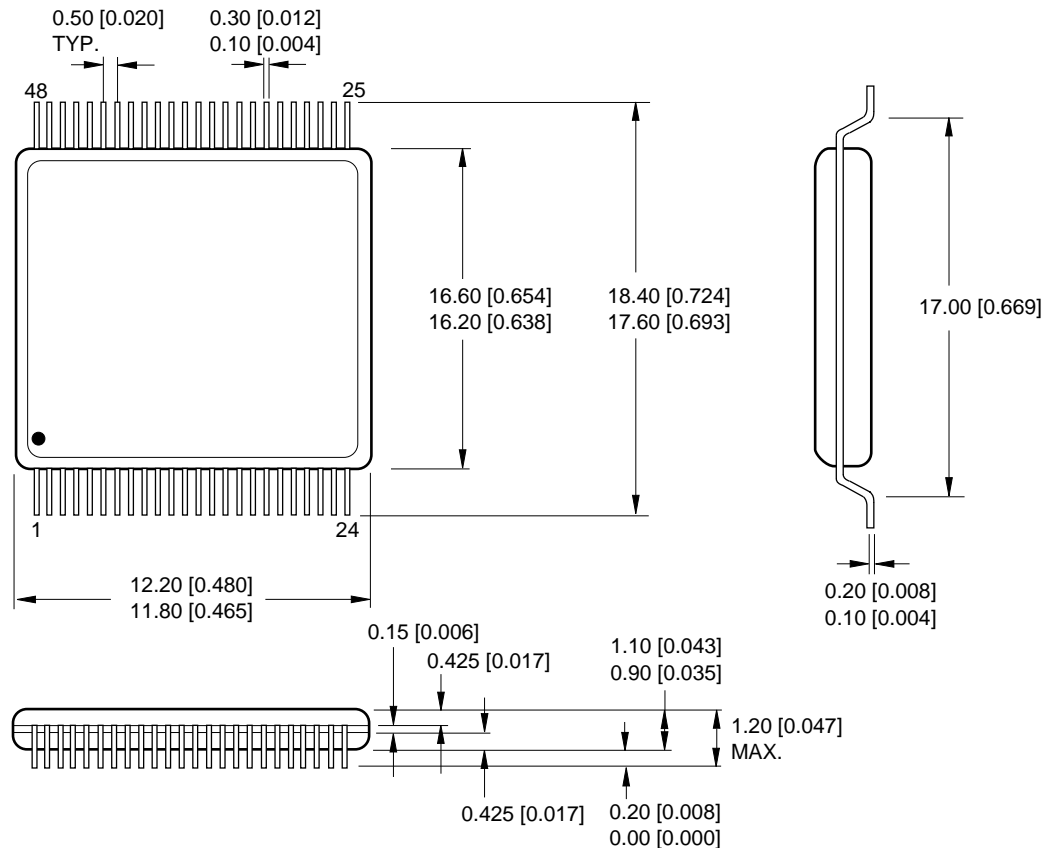
## PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP

**48TSOP (TSOP048-P-1218)**

DIMENSIONS IN MM [INCHES]      MAXIMUM LIMIT  
MINIMUM LIMIT

48TSOP

**48-pin, 12 × 18 mm<sup>2</sup> TSOP (Type I)**

**ORDERING INFORMATION**

LH532000B  
 Device Type

X  
 Package

- { D 40-pin, 600-mil DIP (DIP040-P-0600)
- { N 40-pin, 525-mil SOP (SOP040-P-0525)
- { T 48-pin, 12 x 18 mm<sup>2</sup> TSOP (Type I) (TSOP048-P-1218)
- { TR 48-pin, 12 x 18 mm<sup>2</sup> TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 2M (256K x 8 or 128K x 16) Mask Programmable ROM

**Example:** LH532000BD (CMOS 2M (256K x 8 or 128K x 16) Mask Programmable ROM, 40-pin, 600-mil DIP)

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