

# LH5324500

CMOS 24M (3M × 8/1.5M × 16) MROM

## FEATURES

- 3,145,728 words × 8 bit organization (Byte mode)  
1,572,864 words × 16 bit organization (Word mode)
- Access time: 150 ns (MAX.)
- Power consumption:  
Operating: 357.5 mW (MAX.)  
Standby: 550 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package: 44-pin, 600-mil SOP

## DESCRIPTION

The LH5324500 is a 24M-bit mask-programmable ROM organized as 3,145,728 × 8 bits (Byte mode) or 1,572,864 × 16 bits (Word mode) that can be selected by a BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

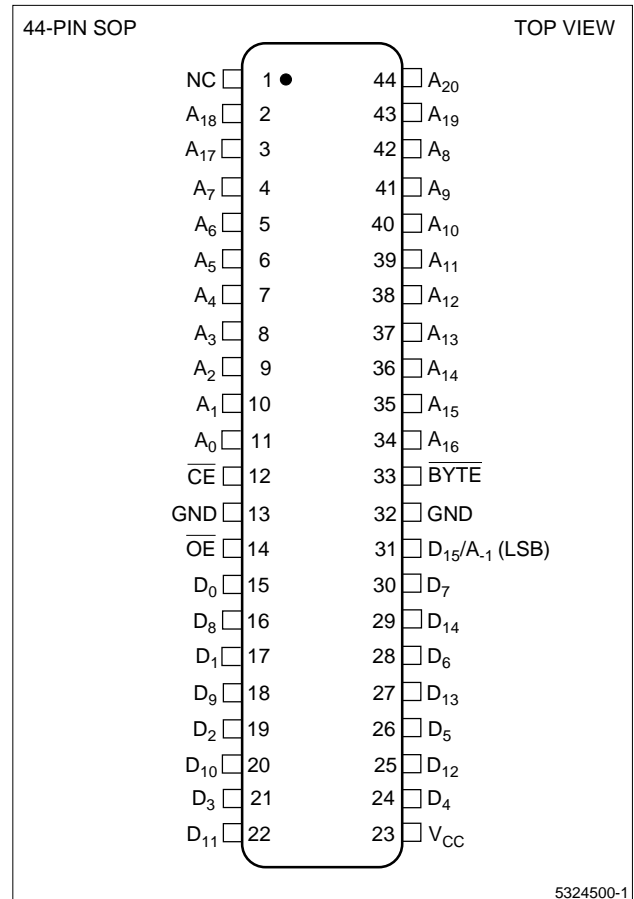


Figure 1. Pin Connections for SOP Package

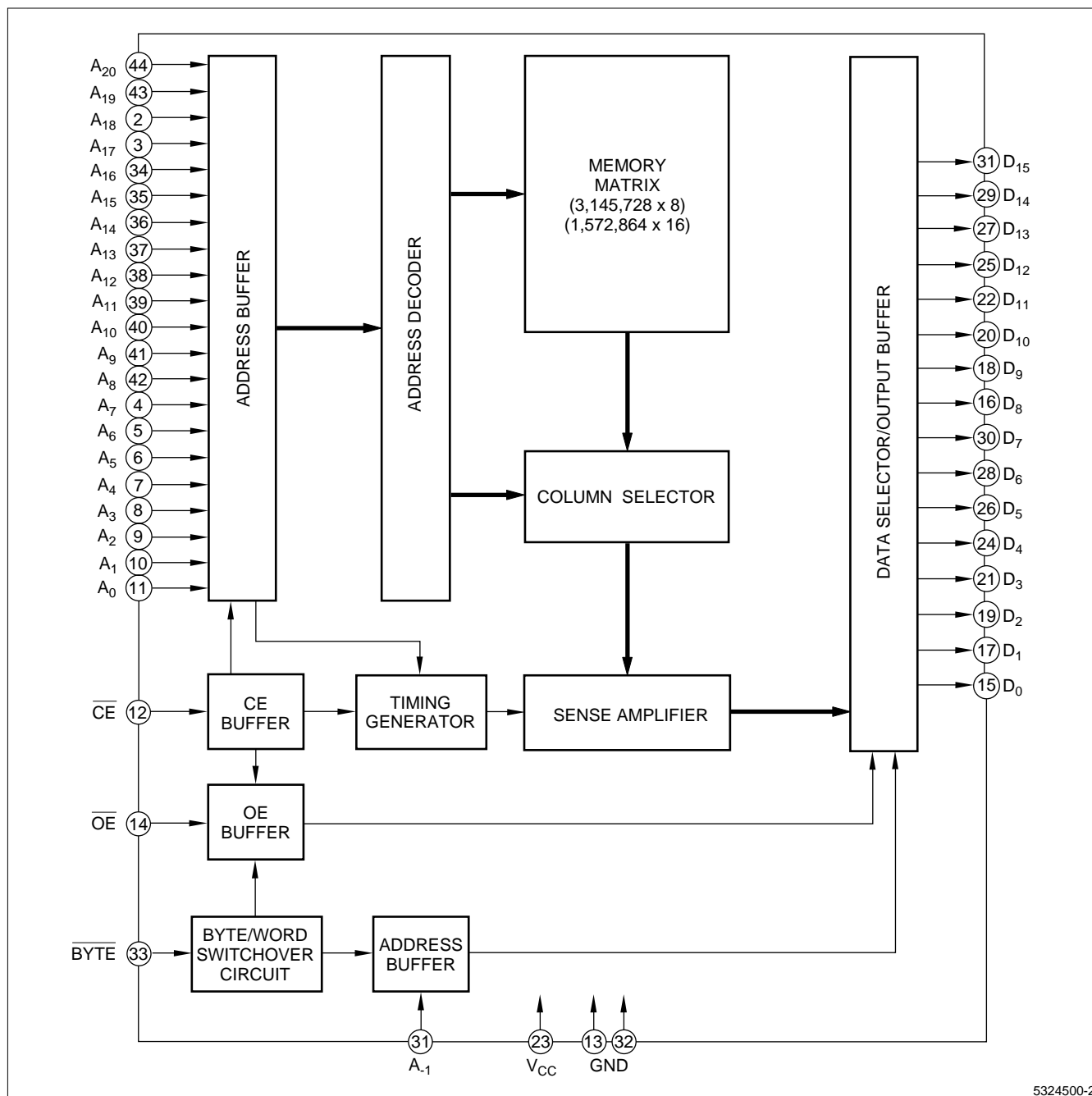


Figure 2. LH5324500 Block Diagram

## PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A <sub>-1</sub> – A <sub>20</sub>	Address input	1
D <sub>0</sub> – D <sub>15</sub>	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE	Output Enable input	
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	
NC	No connection	

### NOTE:

1. The D<sub>15</sub>/A<sub>-1</sub> pin becomes LSB address input (A<sub>-1</sub>) when the  $\overline{\text{BYTE}}$  pin is set to be LOW in byte mode, and data output (D<sub>15</sub>) when set to be HIGH in word mode. When the address inputs become 'High' to both A<sub>19</sub> and A<sub>20</sub>, the data outputs become 'Unspecified' since the data does not exist in this address area.

## TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	$A_{-1}$ ( $D_{15}$ )	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	High-Z	High-Z	—	—	Standby ( $I_{SB}$ )
L	H	X	X	High-Z	High-Z	—	—	Operating ( $I_{CC}$ )
L	L	H	—	$D_0 - D_7$	$D_8 - D_{15}$	$A_0$	$A_{20}$	Operating ( $I_{CC}$ )
L	L	L	L	$D_0 - D_7$	High-Z	$A_{-1}$	$A_{20}$	Operating ( $I_{CC}$ )
L	L	L	H	$D_8 - D_{15}$	High-Z	$A_{-1}$	$A_{20}$	Operating ( $I_{CC}$ )

## NOTE:

X = H or L; High-Z = High-impedance

The  $D_{15}/A_{-1}$  pin becomes LSB address input ( $A_{-1}$ ) when the  $\overline{BYTE}$  pin is set to be LOW in byte mode, and data output ( $D_{15}$ ) when set to be HIGH in word mode. When the address input at both  $A_{19}$  and  $A_{20}$  is HIGH level, the data outputs become high-impedance because this data does not have data.

TRUTH TABLE WHEN BOTH  $A_{20}$  ADN  $A_{19}$  ARE HIGH

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	$A_{-1}$ ( $D_{15}$ )	$A_{20}$	$A_{19}$	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
						$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	X	High-Z	High-Z	—	—	Standby ( $I_{SB}$ )
L	X	H	—	H	H	High-Z	High-Z	$A_0$	$A_{20}$	Operating ( $I_{CC}$ )
L	X	H	—	H	H	High-Z	High-Z	$A_{-1}$	$A_{20}$	Operating ( $I_{CC}$ )

## NOTE:

X = H or L; High-Z = High-impedance

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	$V_{CC}$	−0.3 to +7.0	V
Input voltage	$V_{IN}$	−0.3 to $V_{CC} + 0.3$	V
Output voltage	$V_{OUT}$	−0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V

DC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	$V_{IH}$		2.2	$V_{CC} + 0.3$	V	
Input 'Low' voltage	$V_{IL}$		−0.3	0.8	V	
Output 'High' voltage	$V_{OH}$	$I_{OH} = -400\ \mu\text{A}$	2.4		V	
Output 'Low' voltage	$V_{OL}$	$I_{OL} = 2.0\ \text{mA}$		0.4	V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\ \text{V}$ to $V_{CC}$		10	$\mu\text{A}$	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\ \text{V}$ to $V_{CC}$		10	$\mu\text{A}$	1
Operating current	$I_{CC1}$	$t_{RC} = 150\ \text{ns}$		65	mA	2
	$I_{CC2}$	$t_{RC} = 1\ \mu\text{s}$		55		
Standby current	$I_{SB1}$	$\overline{CE} = V_{IH}$		2	mA	
	$I_{SB2}$	$\overline{CE} = V_{CC} - 0.2\ \text{V}$		100		
Input capacitance	$C_{IN}$	$f = 1\ \text{MHz}$		10	pF	
Output capacitance	$C_{OUT}$	$T_A = 25^\circ\text{C}$		10	pF	

## NOTES:

- $\overline{CE}/\overline{OE} = V_{IH}$
- $V_{IN} = V_{IH}$  or  $V_{IL}$ ,  $\overline{CE} = V_{IL}$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	150		ns	
Address access time	$t_{AA}$		150	ns	
Chip enable access time	$t_{ACE}$		150	ns	
Output enable delay time	$t_{OE}$		70	ns	
Output hold time	$t_{OH}$	5		ns	
Output floating time	$t_{CHZ}$		60	ns	1
	$t_{OHZ}$		60	ns	
	$t_{AHZ}$		70	ns	

**NOTE:**

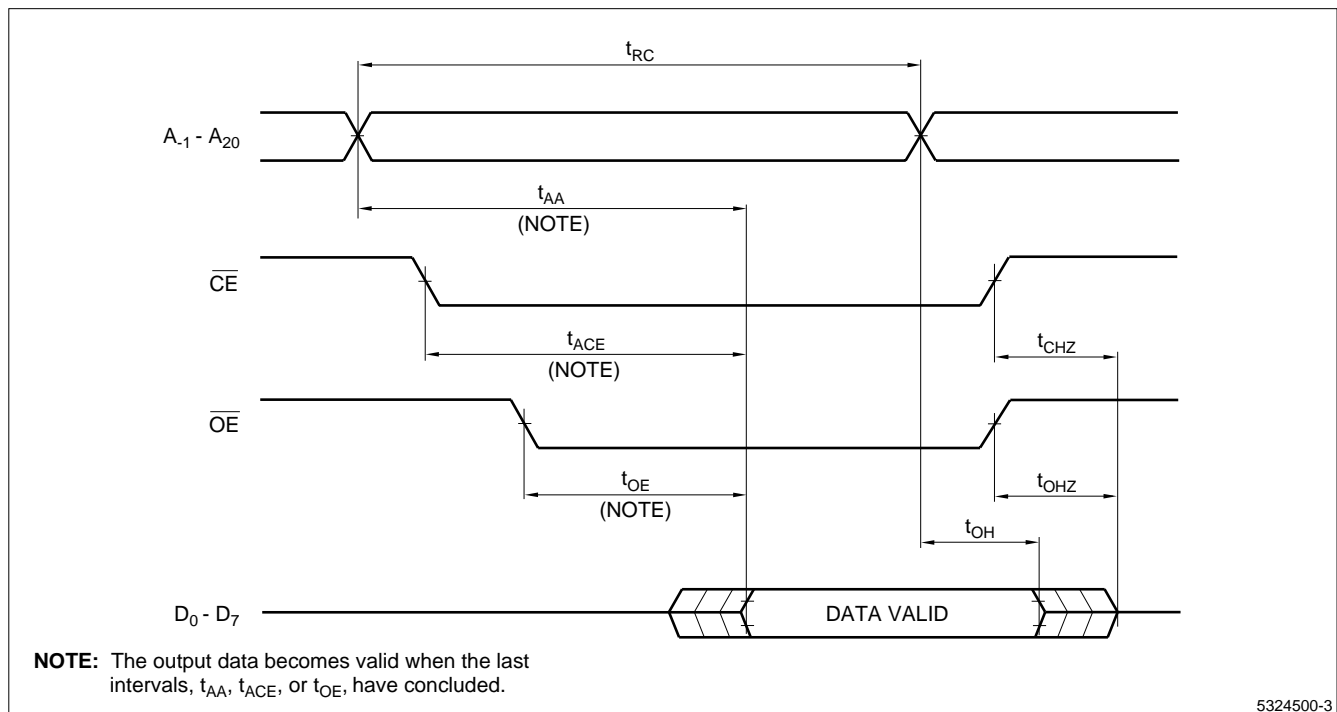
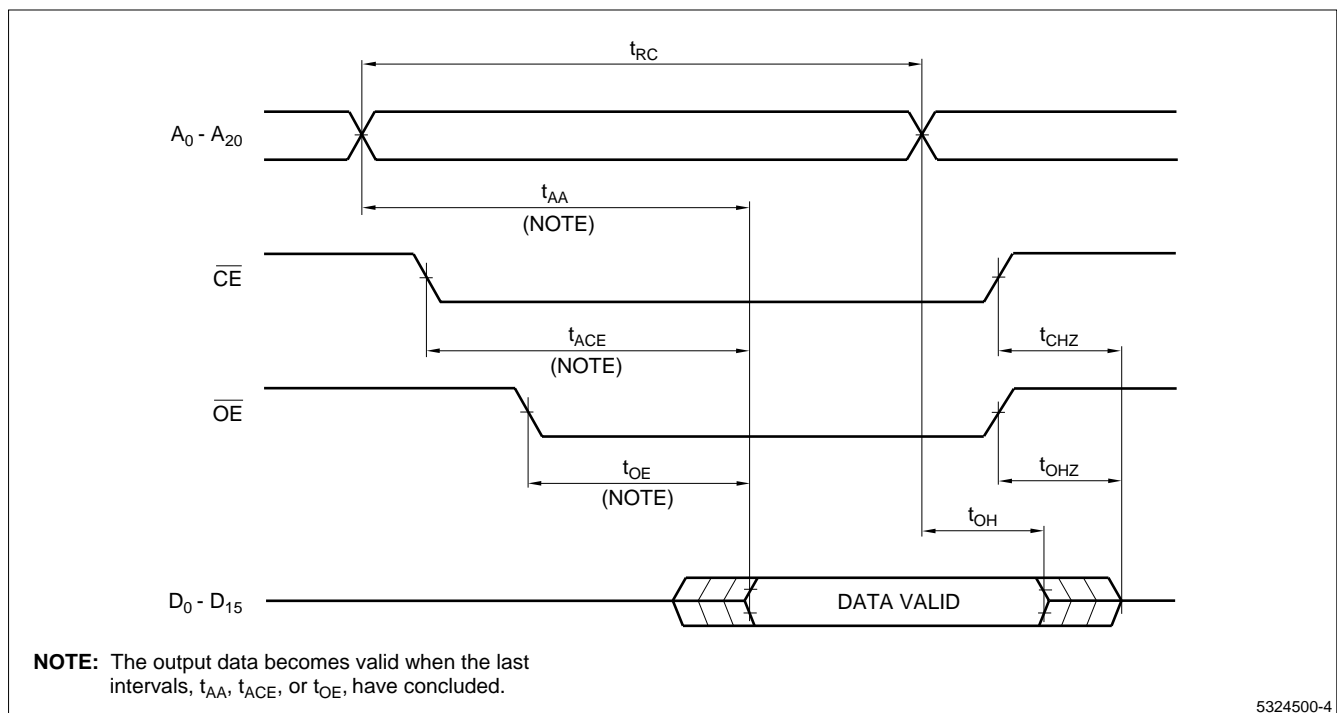
1. This is the time required for the outputs to become high-impedance.

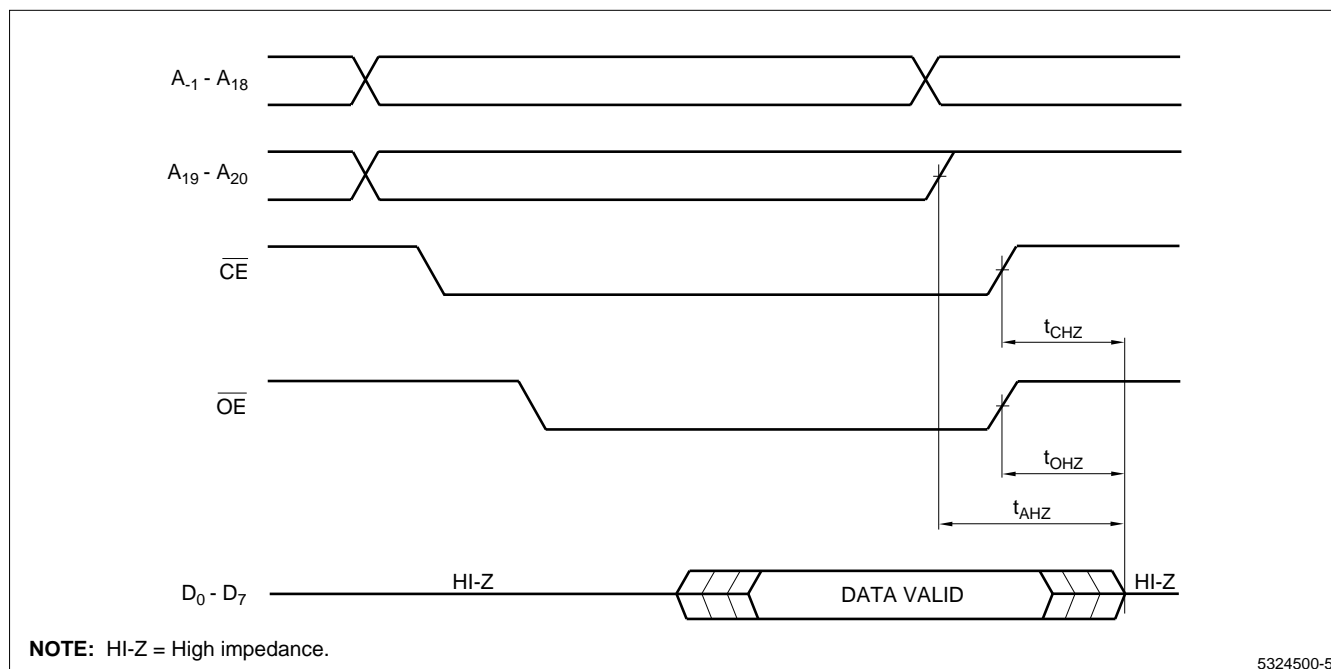
**AC TEST CONDITIONS**

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input signal rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

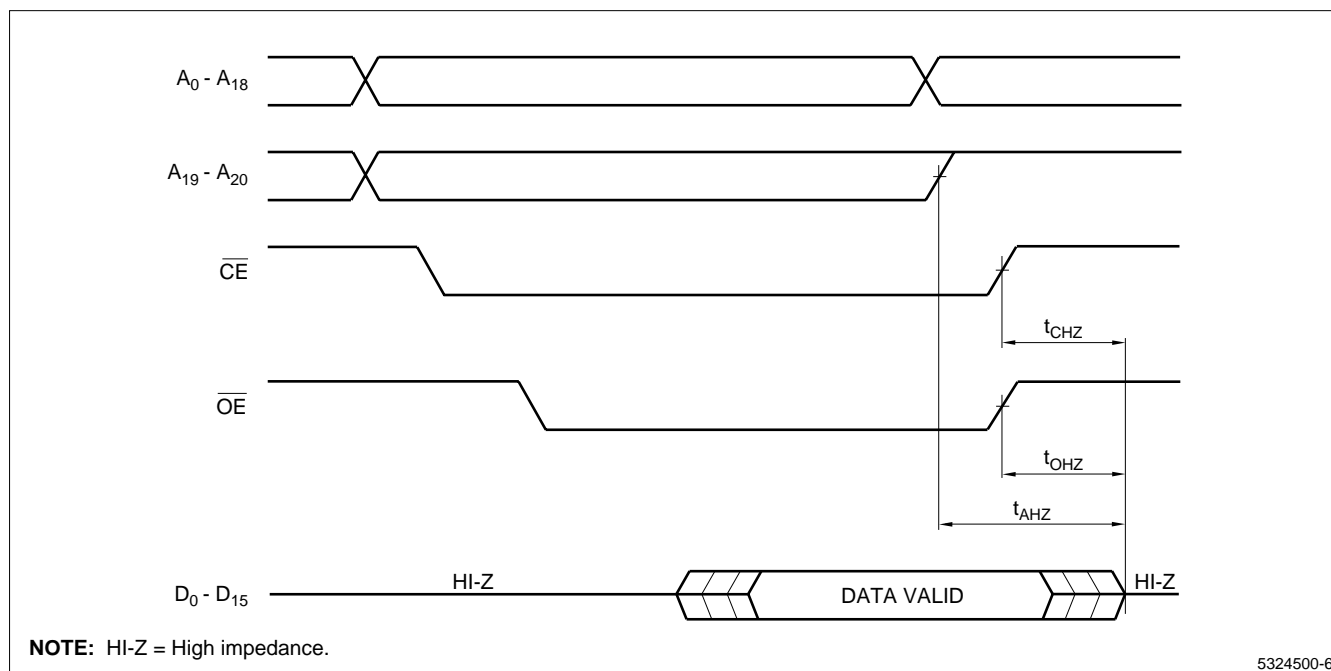
**CAUTION**

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.

Figure 3. Byte Mode ( $\text{BYTE} = V_{IL}$ )Figure 4. Word Mode ( $\text{BYTE} = V_{IH}$ )

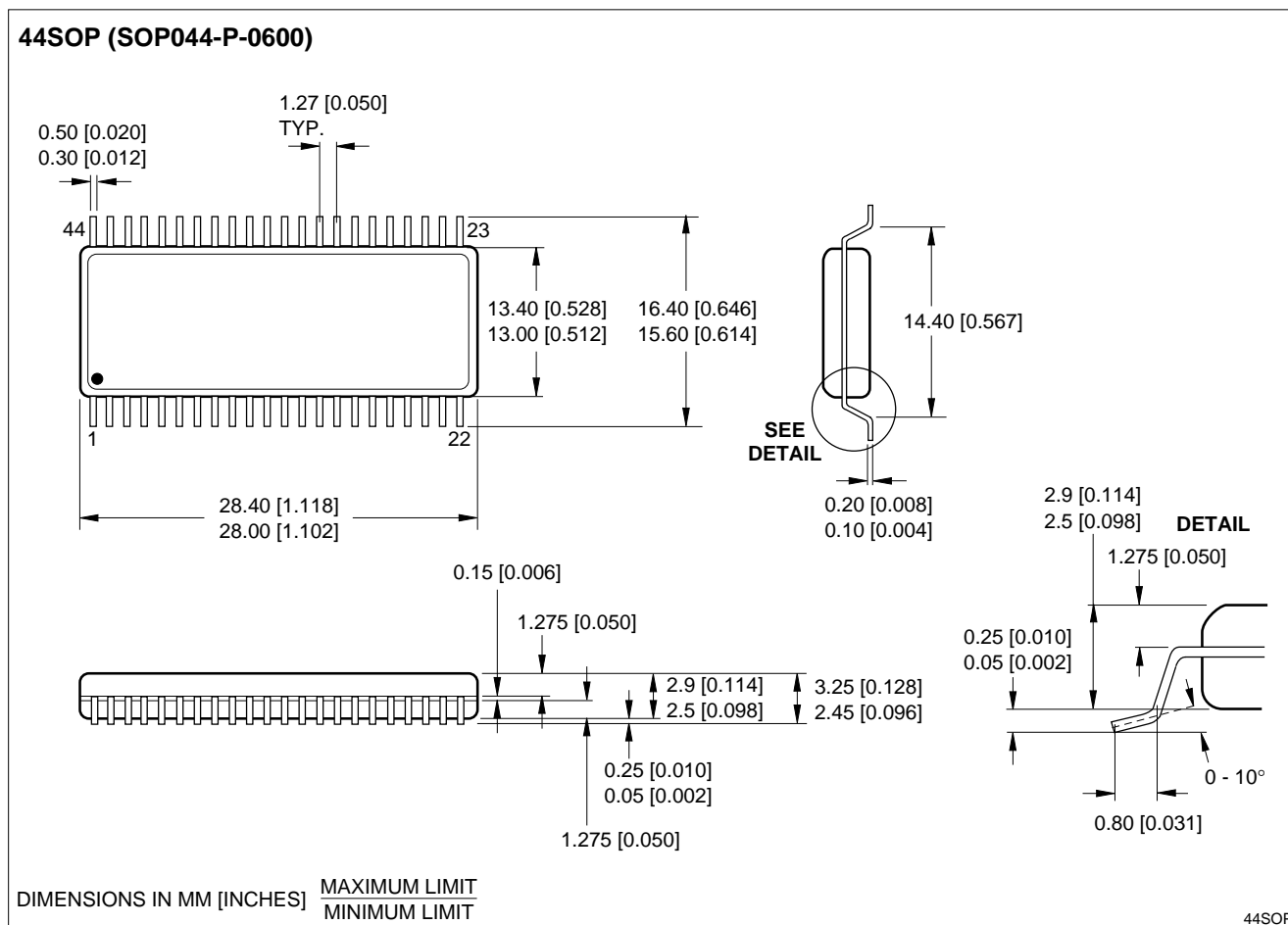


**Figure 5. Byte Mode (BYTE = V<sub>IL</sub>)**  
**When the address inputs become 'High' to both A<sub>19</sub> and A<sub>20</sub>**



**Figure 6. Word Mode (BYTE = V<sub>IH</sub>)**  
**When the address inputs become 'High' to both A<sub>19</sub> and A<sub>20</sub>**

## PACKAGE DIAGRAM



44-pin, 600-mil SOP

## ORDERING INFORMATION

LH5324500  
Device Type

N  
Package

44-pin, 600-mil SOP (SOP044-P-0600)

CMOS 24M (3M x 8 or 1.5M x 16) Mask-Programmable ROM

**Example:** LH5324500N (CMOS 24M (3M x 8 or 1.5M x 16) Mask-Programmable ROM, 44-pin, 600-mil SOP)

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