

LH53517

CMOS 512K (64K × 8) MROM

FEATURES

- 65,536 words × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
 - Operating: 165 mW (MAX.)
 - Standby: 550 μ W (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Mask-programmable OE/ $\overline{\text{OE}}$
- Packages:
 - 28-pin, 600-mil DIP
 - 28-pin, 450-mil SOP
 - 28-pin, $8 \times 13.4 \text{ mm}^2$ TSOP (Type I)

DESCRIPTION

The LH53517 is a mask-programmable ROM organized as $65,536 \times 8$ bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

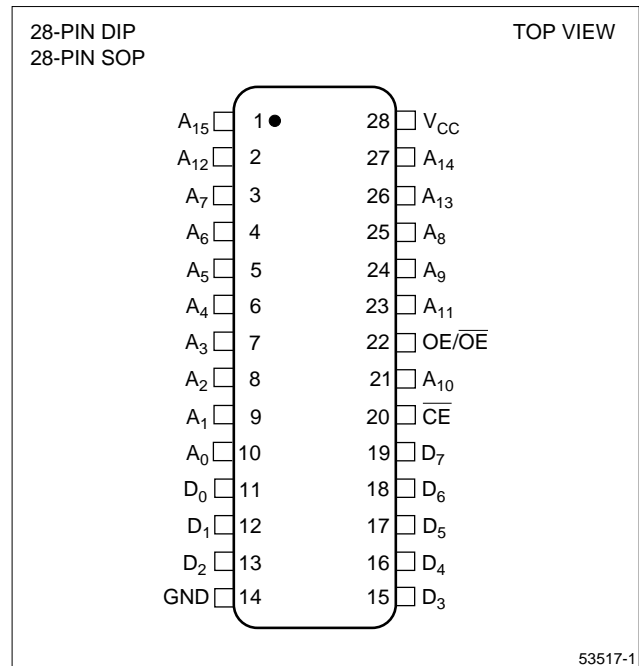


Figure 1. Pin Connections for DIP and SOP Packages

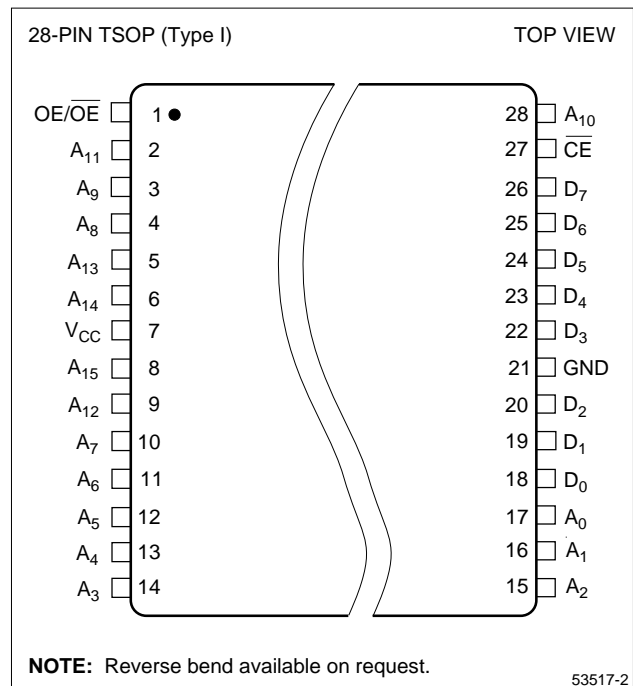


Figure 2. Pin Connections for TSOP Package

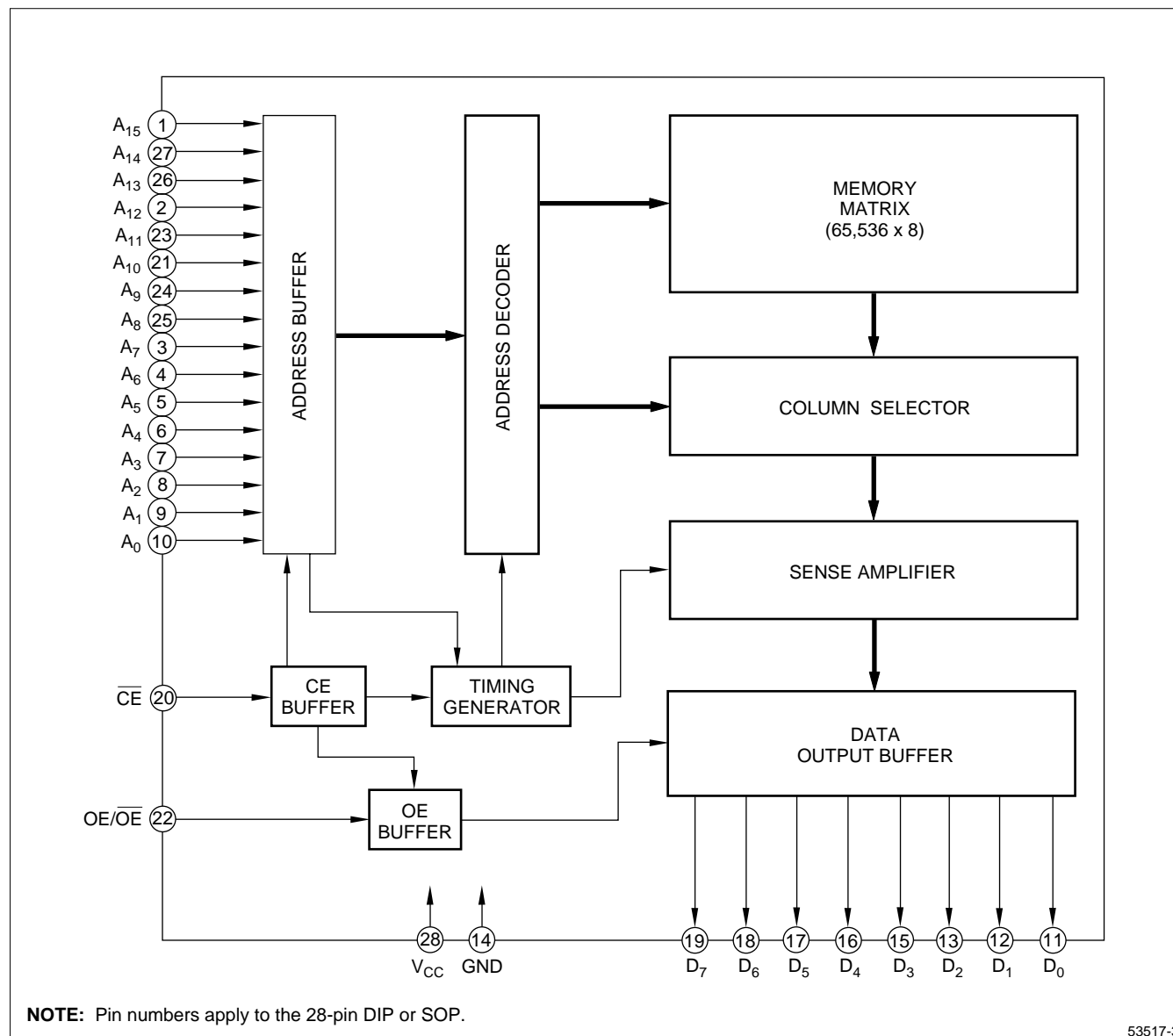


Figure 3. LH53517 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₀ – A ₁₅	Address input	
D ₀ – D ₇	Data output	
CE	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/OE	Output enable input	1
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

- Active level of OE/OE is mask-programmable.

TRUTH TABLE

CE	OE/OE	DATA OUTPUT	CURRENT CONSUMPTION
H	X	High-Z	Standby
L	L/H	Output	Operating
	H/L		

NOTE:

X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Input 'High' voltage	V_{IH}		2.2	$V_{CC} + 0.3$	V	
Output 'Low' voltage	V_{OL}	$I_{OL} = 1.6\text{ mA}$		0.4	V	
Output 'High' voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4		V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{CC}$		10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$		10	μA	1
Operating current	I_{CC1}	$t_{RC} = 150\text{ ns}$		30	mA	2
	I_{CC2}	$t_{RC} = 1\text{ }\mu\text{s}$		15		
	I_{CC3}	$t_{RC} = 150\text{ ns}$		25	mA	3
	I_{CC4}	$t_{RC} = 1\text{ }\mu\text{s}$		12		
Standby current	I_{SB1}	$CE = V_{IH}$		2	mA	
	I_{SB2}	$CE = V_{CC} - 0.2\text{ V}$		100	μA	
Input capacitance	C_{IN}	$f = 1\text{ MHz}$		10	pF	
Output capacitance	C_{OUT}	$T_A = 25^\circ\text{C}$		10	pF	

NOTES:

1. $CE/OE = V_{IH}$, $OE = V_{IL}$
2. $V_{IN} = V_{IH}/V_{IL}$, $CE = V_{IL}$, outputs open
3. $V_{IN} = (V_{CC} - 0.2\text{ V})$, 0.2 V , $CE = 0.2\text{ V}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	1

NOTE:

1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

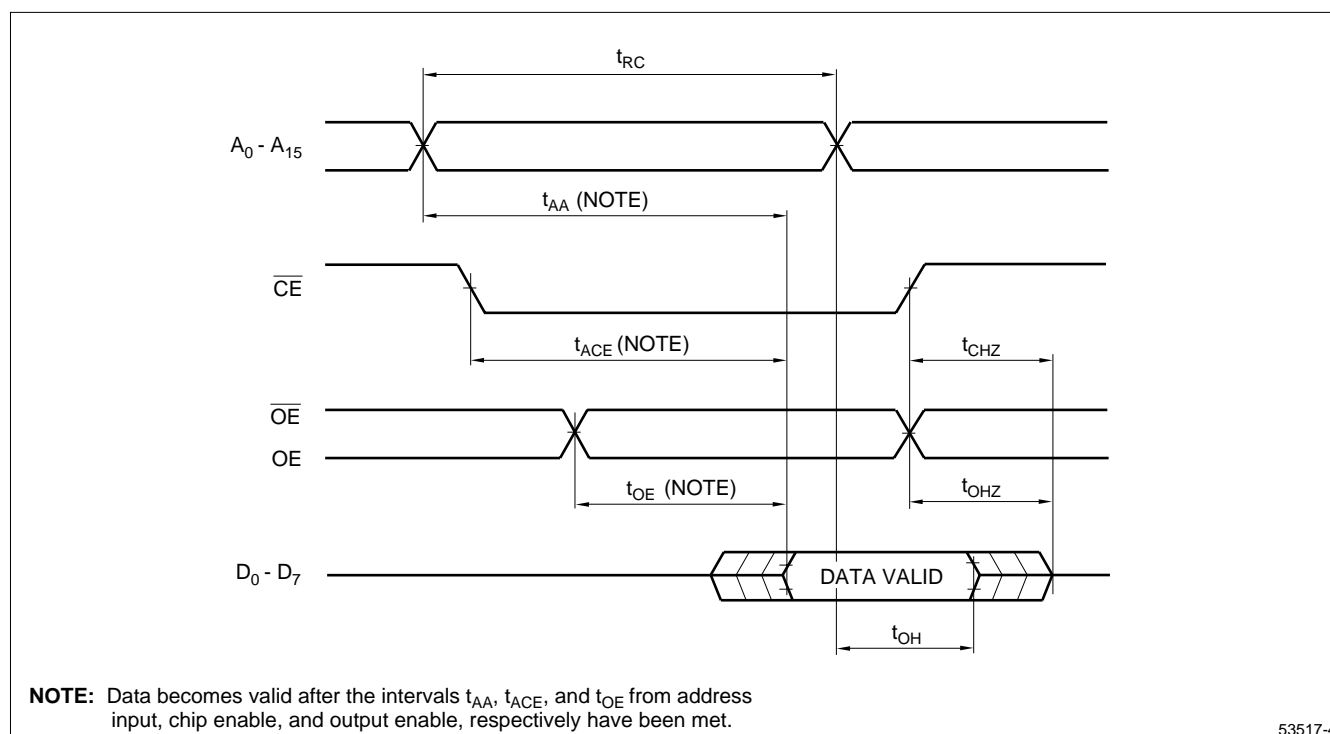
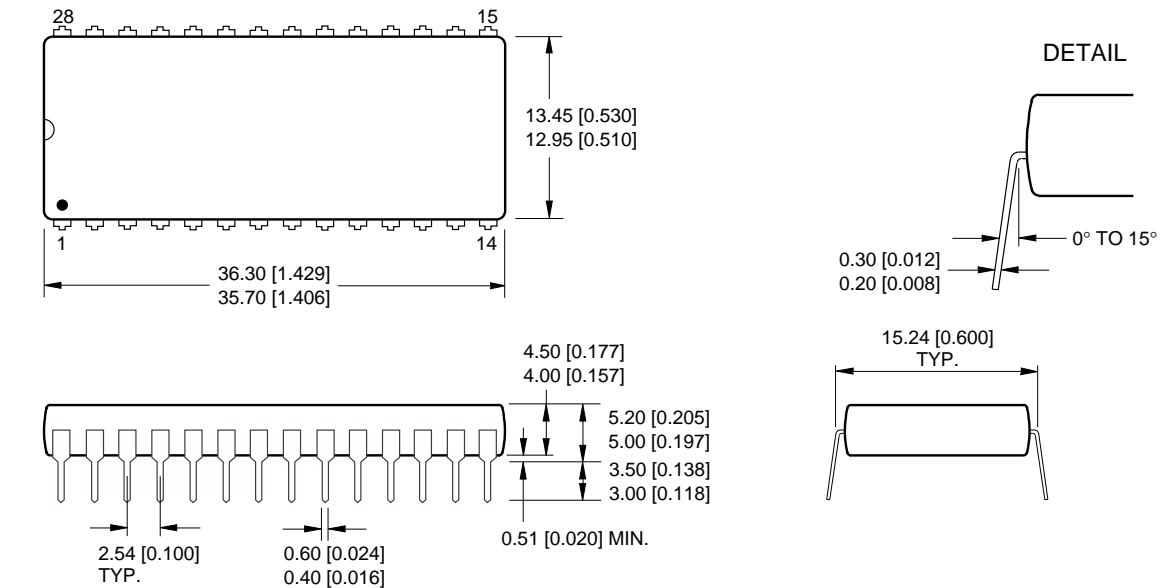


Figure 4. Timing Diagram

PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)

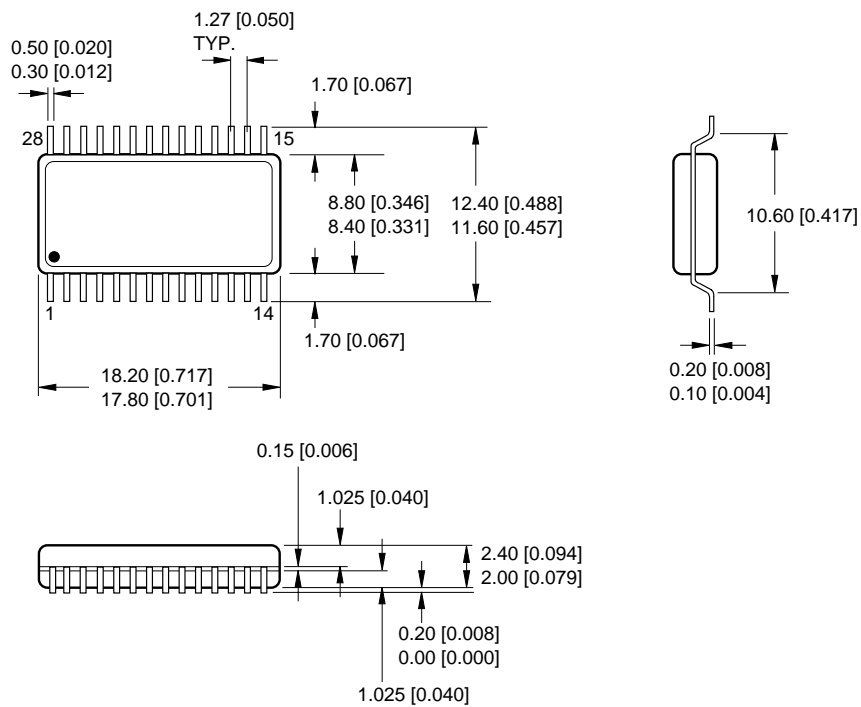


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

28DIP-2

28-pin, 600-mil DIP

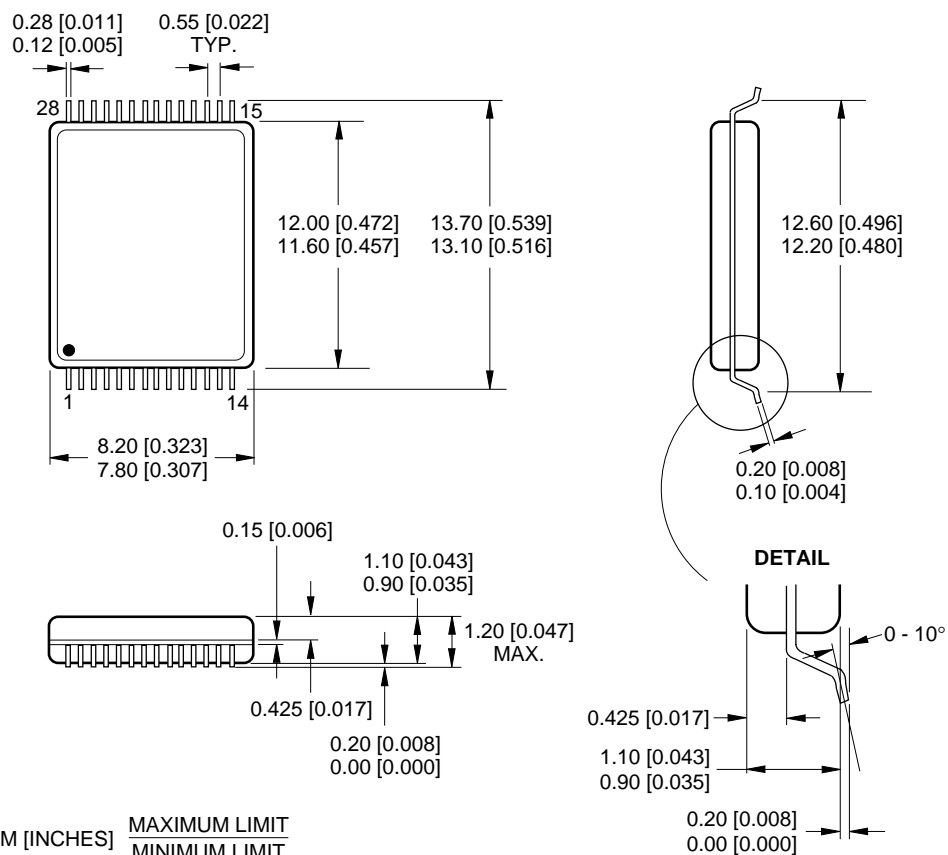
28SOP (SOP028-P-0450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

28SOP

28-pin, 450-mil SOP

28TSOP (TSOP028-P-0813)

28TSOP

28-pin, 8 × 13 mm² TSOP (Type I)**ORDERING INFORMATION**

LH53517
Device Type

X
Package

- D 28-pin, 600-mil DIP (DIP028-P-0600)
- N 28-pin, 450-mil SOP (SOP028-P-0450)
- T 28-pin, 8 x 13.4 mm² TSOP (Type I) (TSOP028-P-0813)
- TR 28-pin, 8 x 13 mm² TSOP (Type I) Reverse bend (TSOP028-P-0813)

CMOS 512K (64K x 8) Mask Programmable ROM

Example: LH53517D (CMOS 512K (64K x 8) Mask Programmable ROM, 28-pin, 600-mil DIP)

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