

# LH5P8128

CMOS 1M (128K × 8) Pseudo-Static RAM

## FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Single +5 V power supply
- Power consumption:  
Operating: 572/385/275 mW (MAX.)  
Standby (CMOS level): 1.1 mW (MAX.)
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Compatible with standard 1M SRAM pinout
- Packages:  
32-pin, 600-mil DIP  
32-pin, 525-mil SOP  
32-pin, 8 × 20 mm<sup>2</sup> TSOP (Type I)

## DESCRIPTION

The LH5P8128 is a 1M bit Pseudo-Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 128K × 8 SRAM sockets can be filled with the LH5P8128 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8128 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and a simple interface.

## PIN CONNECTIONS

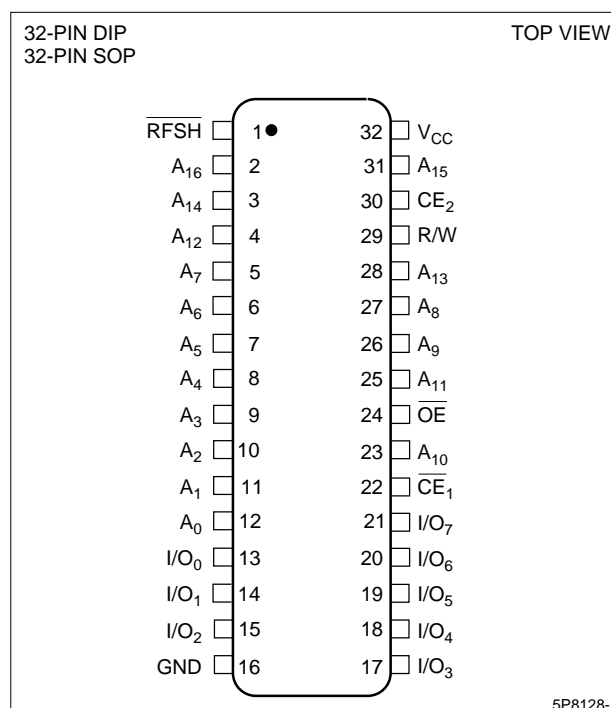


Figure 1. Pin Connections for DIP and SOP Packages

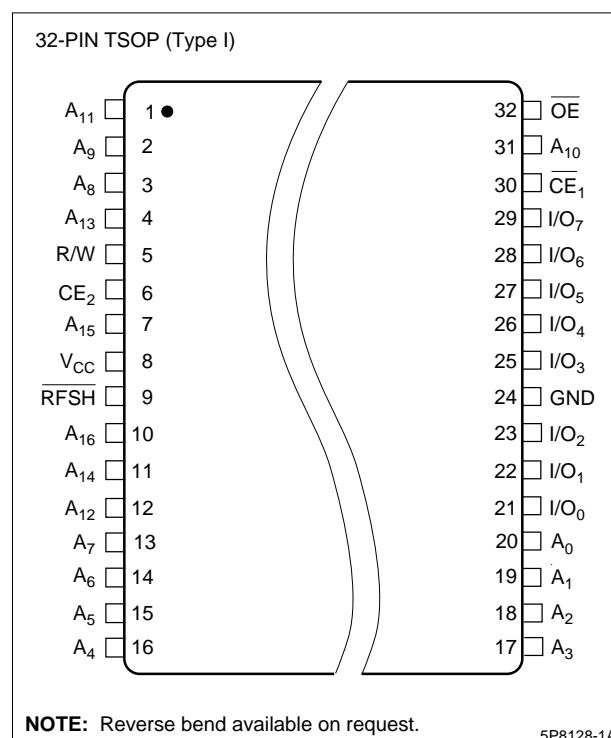


Figure 2. Pin Connections for TSOP Package

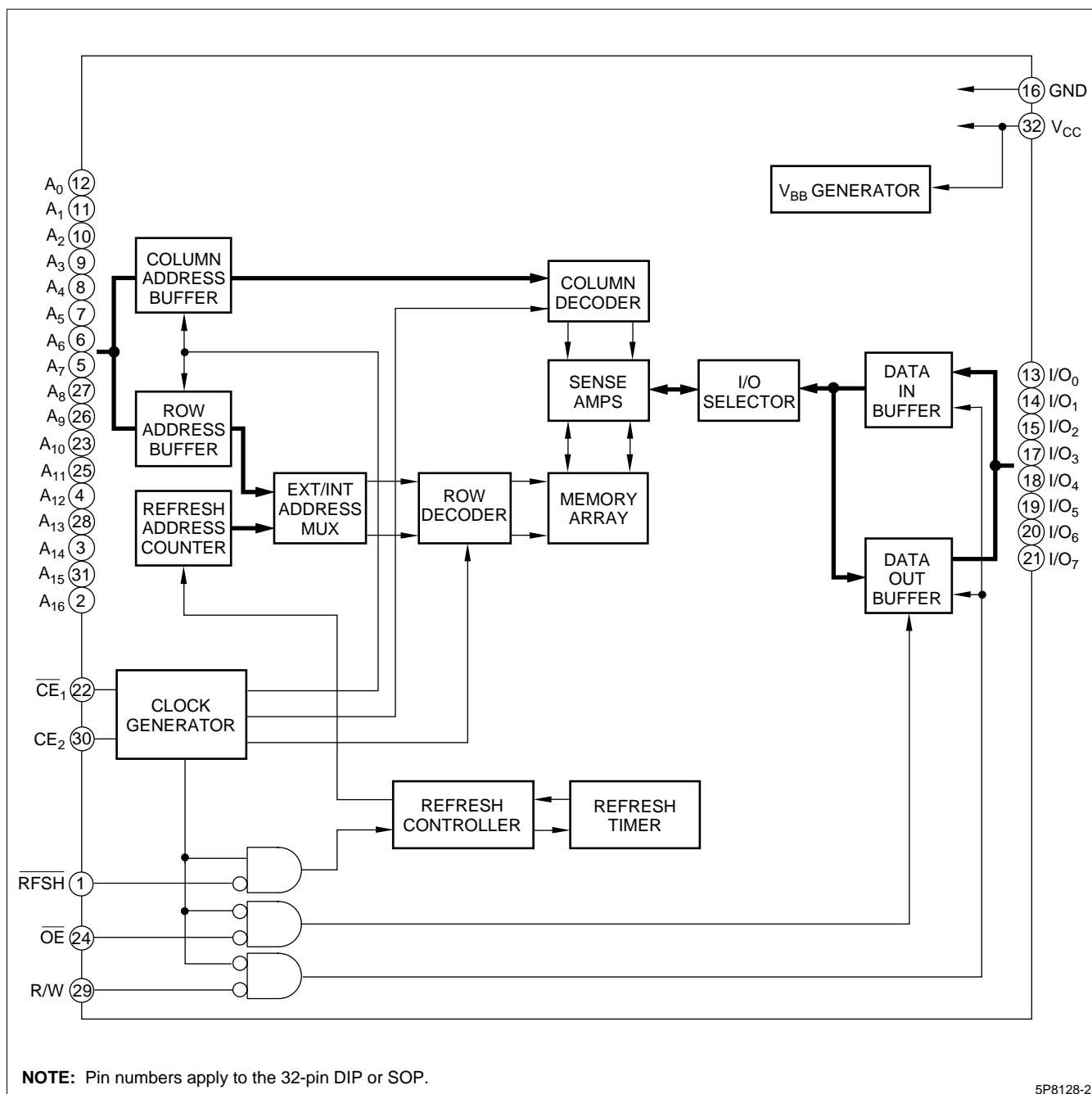


Figure 3. LH5P8128 Block Diagram

## PIN DESCRIPTION

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>16</sub>	Address input
R/W	Read/Write input
OE	Output Enable Input

SIGNAL	PIN NAME
CE <sub>1</sub> , CE <sub>2</sub>	Chip Enable input
RFSH	Refresh input
I/O <sub>0</sub> - I/O <sub>7</sub>	Data input/output

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	$V_T$	-1.0 to +7.0	V	1
Output short circuit current	$I_O$	50	mA	
Power dissipation	$P_D$	600	mW	
Operating temperature	$T_{opr}$	0 to +70	°C	
Storage temperature	$T_{stg}$	-55 to +150	°C	

**NOTE:**

1. The maximum applicable voltage on any pin with respect to GND.

**RECOMMENDED OPERATING CONDITIONS ( $T_A = 0$  to +70°C)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	$V_{IH}$	2.4		$V_{CC} + 0.3$	V
	$V_{IL}$	-1.0		0.8	V

**CAPACITANCE ( $T_A = 0$  to +70°C,  $f = 1$  MHz,  $V_{CC} = 5.0$  V  $\pm 10\%$ )**

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	$A_0 - A_{16}$	$C_{IN1}$		8	pF
	R/W, OE	$C_{IN2}$		5	pF
	$CE_1, CE_2$	$C_{IN3}$		5	pF
	RFSH	$C_{IN4}$		5	pF
Input/output capacitance	I/O <sub>0</sub> - I/O <sub>7</sub>	$C_{OUT1}$		10	pF

**DC CHARACTERISTICS ( $T_A = 0$  to +70°C,  $V_{CC} = 5.0$  V  $\pm 10\%$ )**

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8128-60	$I_{CC1}$	$t_{RC} = t_{RC} \text{ (MIN)}$		104	mA	1, 2
	LH5P8128-80				70		
	LH5P8128-10				50		
Standby current	TTL Input	$I_{CC2}$			1	mA	1, 3
	CMOS Input				0.2		1, 4
Self-refresh average current	TTL Input	$I_{CC3}$			1	mA	1, 5
	CMOS Input				0.2		1, 6
Input leakage current		$I_{LI}$	$0 \text{ V} \leq V_{IN} \leq 6.5 \text{ V}$ $0 \text{ V}$ except on test pins	-10	10	$\mu\text{A}$	
I/O leakage current		$I_{LO}$	$0 \text{ V} \leq V_{OUT} \leq V_{CC} + 0.3 \text{ V}$ Output in high-impedance state	-10	10	$\mu\text{A}$	
Output HIGH voltage		$V_{OH}$	$I_{OUT} = -1 \text{ mA}$	2.4		V	
Output LOW voltage		$V_{OL}$	$I_{OUT} = 4 \text{ mA}$		0.4	V	

**NOTES:**

1. Specified values are with outputs open.
2. Depends on the cycle time.
3.  $CE_1 = V_{IH}$ , RFSH =  $V_{IH}$
4.  $CE_1 = V_{CC} - 0.2 \text{ V}$ , RFSH =  $V_{CC} - 0.2 \text{ V}$
5.  $CE_1 = V_{IH}$ , RFSH =  $V_{IL}$
6.  $CE_1 = V_{CC} - 0.2 \text{ V}$ , RFSH =  $0.2 \text{ V}$

# AC ELECTRICAL CHARACTERISTICS<sup>1,2,3</sup>

( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ )

PARAMETER	SYMBOL	LH5P8128-60		LH5P8128-80		LH5P8128-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	$t_{RC}$	100		130		160		ns	
Read modify write cycle time	$t_{RMW}$	165		195		235		ns	
CE pulse width	$t_{CE}$	60	10,000	80	10,000	100	10,000	ns	
CE precharge time	$t_p$	40		40		50		ns	
Address setup time	$t_{AS}$	0		0		0		ns	4
Address hold time	$t_{AH}$	15		20		25		ns	4
Read command setup time	$t_{RCS}$	0		0		0		ns	
Read command hold time	$t_{RCH}$	0		0		0		ns	
CE access time	$t_{CEA}$		60		80		100	ns	5
OE access time	$t_{OEA}$		25		30		35	ns	5
CE to output in Low-Z	$t_{CLZ}$	20		20		20		ns	
OE to output in Low-Z	$t_{OLZ}$	0		0		0		ns	
Output enable from end of write	$t_{WLZ}$	0		0		0		ns	
Chip disable to output in High-Z	$t_{CHZ}$		20		25		30	ns	
Output disable to output in High-Z	$t_{OHZ}$		20		25		30	ns	
Write enable to output in High-Z	$t_{WHZ}$		20		25		30	ns	
OE setup time	$t_{OES}$	0		0		0		ns	
OE hold time	$t_{OEH}$	10		10		10		ns	
Write command pulse width	$t_{WP}$	30		30		30		ns	
Write command setup time	$t_{WCS}$	30		30		30		ns	
Write command hold time	$t_{WCH}$	40		50		60		ns	
Data setup time from write	$t_{DSW}$	25		30		35		ns	6
Data setup time from $\overline{CE}$	$t_{DSC}$	25		30		35		ns	6
Data hold time from write	$t_{DHW}$	0		0		0		ns	6
Data hold time from CE	$t_{DHC}$	0		0		0		ns	6
Transition time (rise and fall)	$t_T$	3	35	3	35	3	35	ns	
Refresh time interval	$t_{REF}$		8		8		8	ms	
Refresh command hold time	$t_{RHC}$	15		15		15		ns	
Auto refresh cycle time	$t_{FC}$	100		130		160		ns	
Refresh delay time from $\overline{CE}$	$t_{RFD}$	30		40		50		ns	
Refresh pulse width (Auto refresh)	$t_{FAP}$	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	$t_{FP}$	30		30		30		ns	
Refresh pulse width (Self refresh)	$t_{FAS}$	8,000		8,000		8,000		ns	
CE delay time from refresh precharge (Self refresh)	$t_{FRS}$	140		160		190		ns	

## NOTES:

- In order to initialize the circuit,  $\overline{CE}_1$  should be kept at  $V_{IH}$  or  $CE_2$  should be kept at  $V_{IL}$  for 100  $\mu\text{s}$  after power-up, followed by at least 8 dummy cycles.
- AC characteristics are measured at  $t_T = 5\text{ ns}$ .
- AC characteristics are measured at the following condition (see figure at right).
- Address is latched at the negative edge of  $\overline{CE}_1$  or at the positive edge of  $CE_2$ .
- Measured with a load equivalent to 2TTL + 100 pF.
- Data is latched at the positive edge of W/R or at the positive edge of  $CE_1$  or at the negative edge of  $CE_2$ .

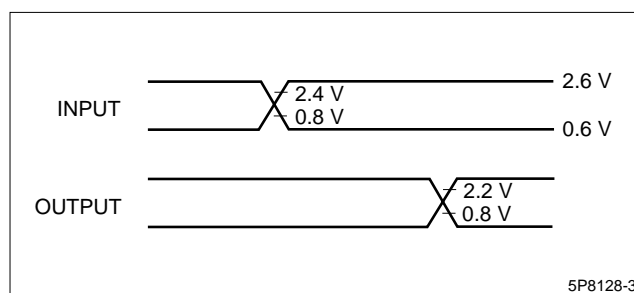
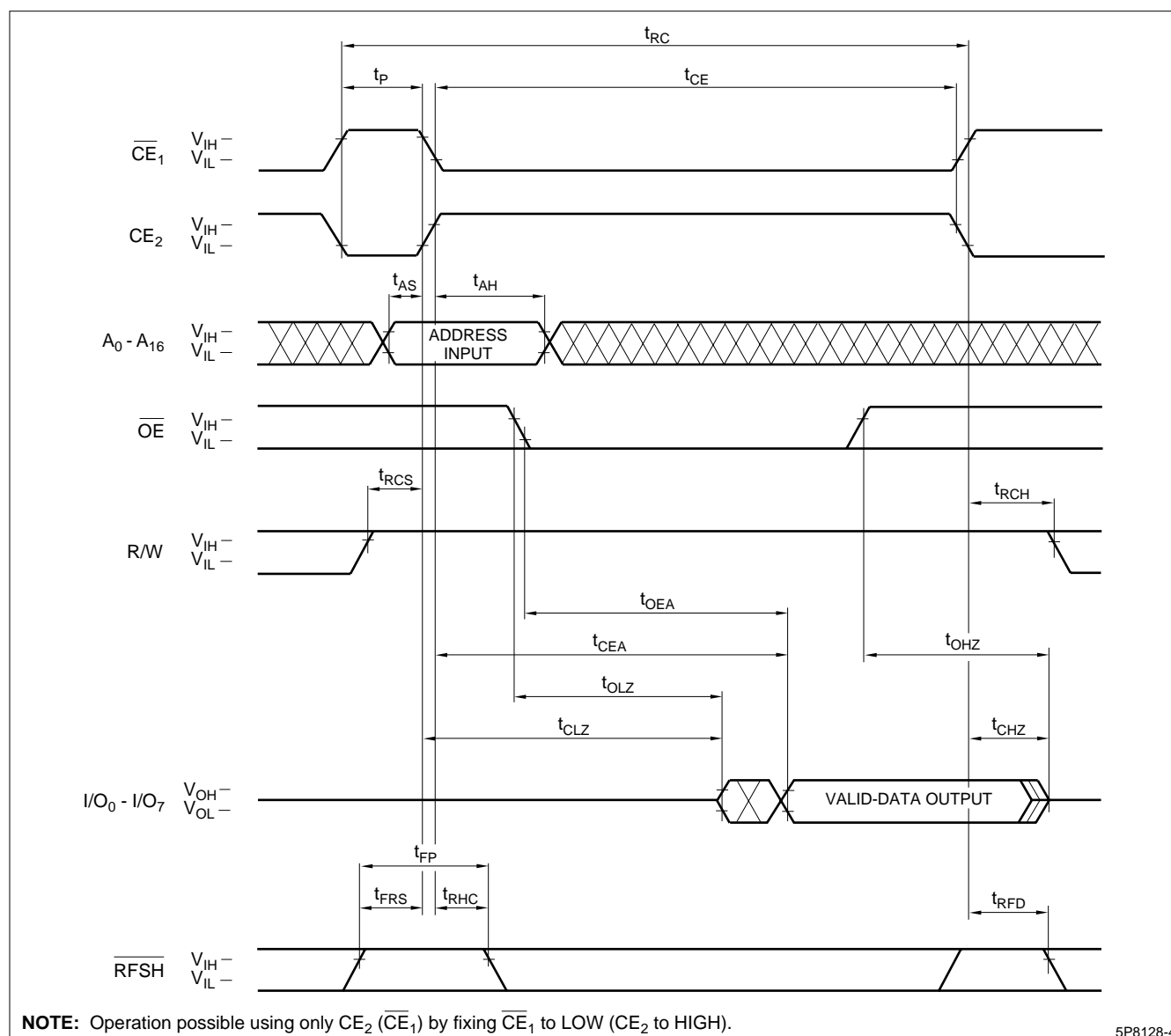
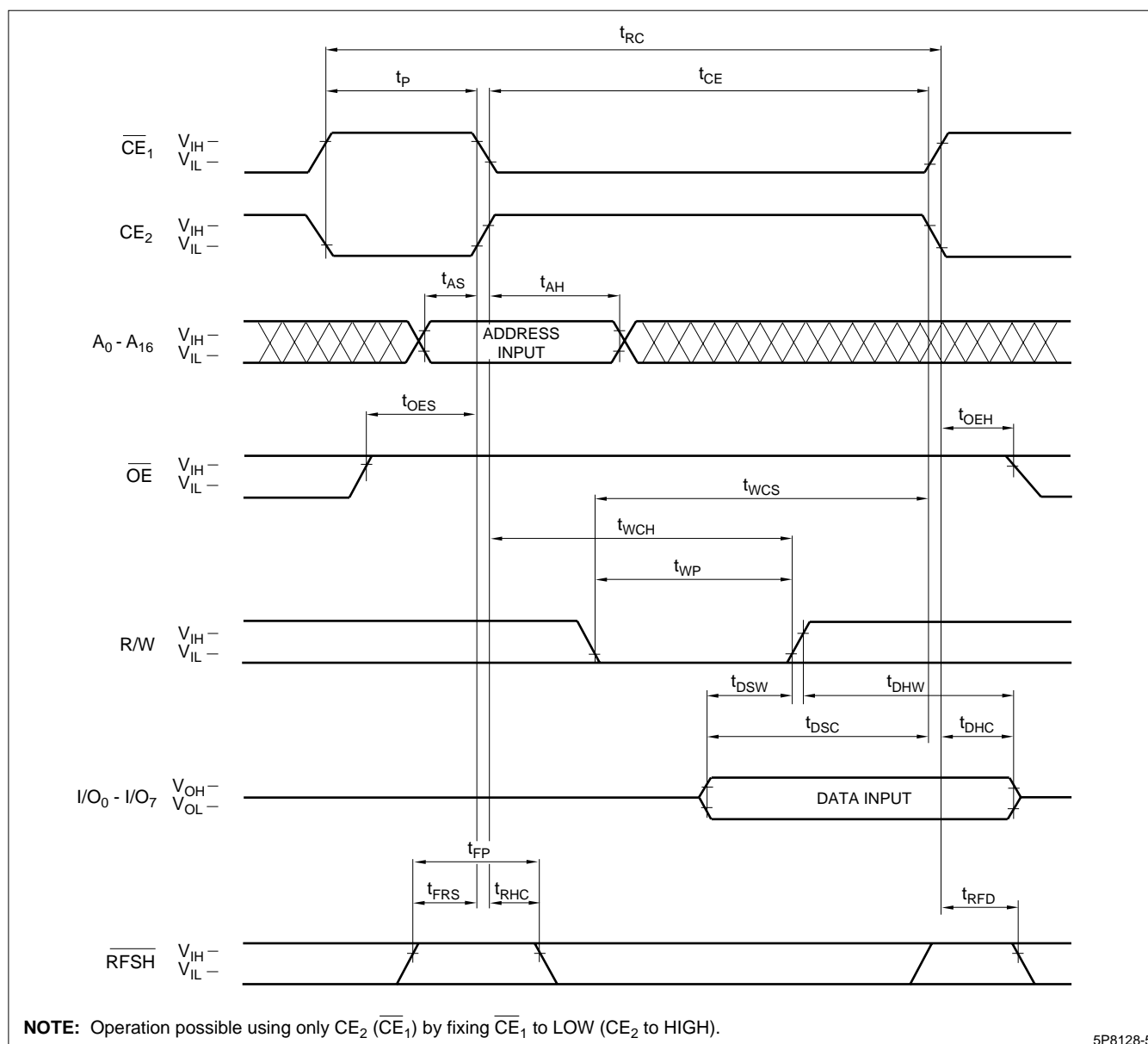
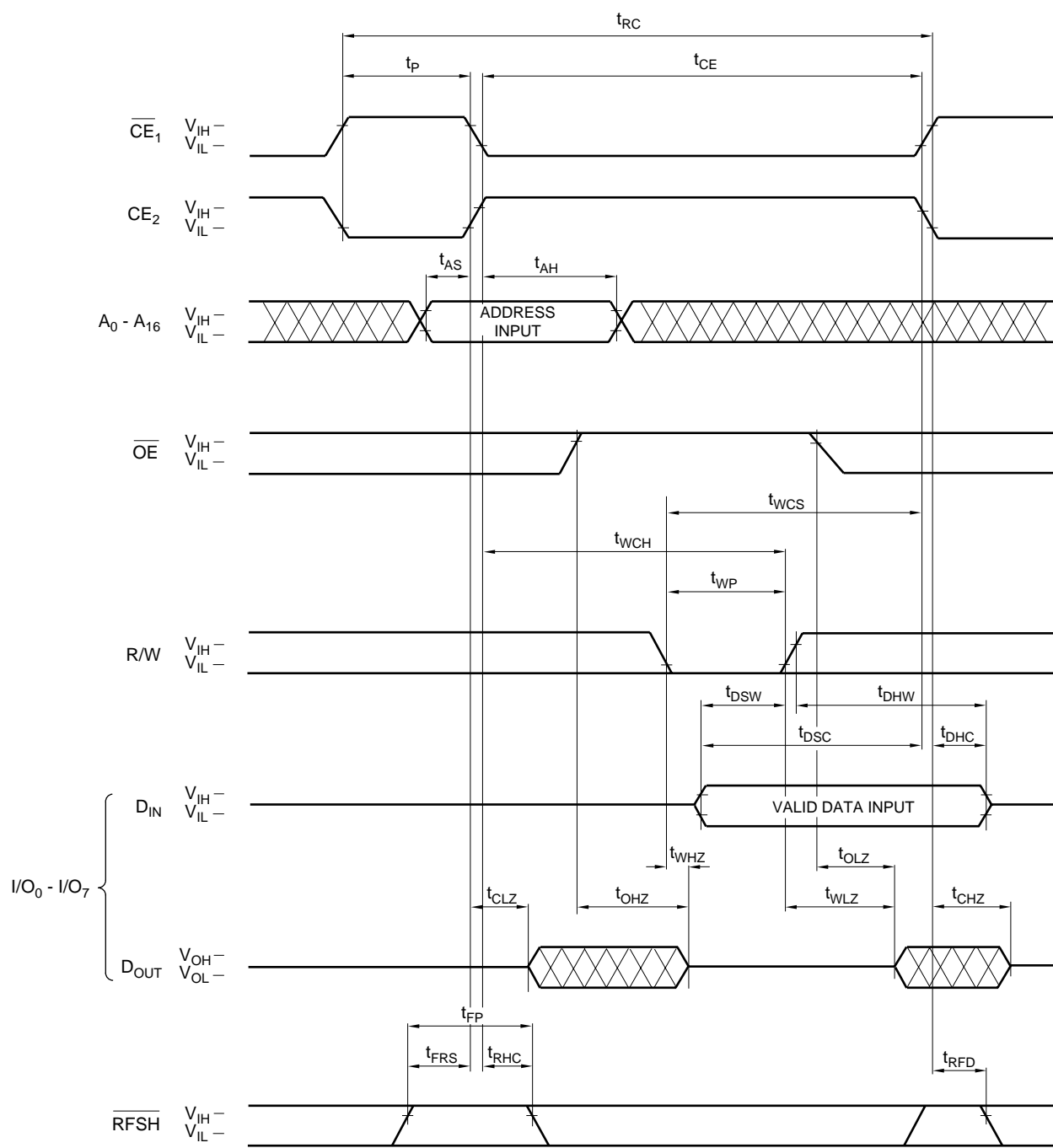


Figure 4. AC Characteristics



### Figure 5. Read Cycle

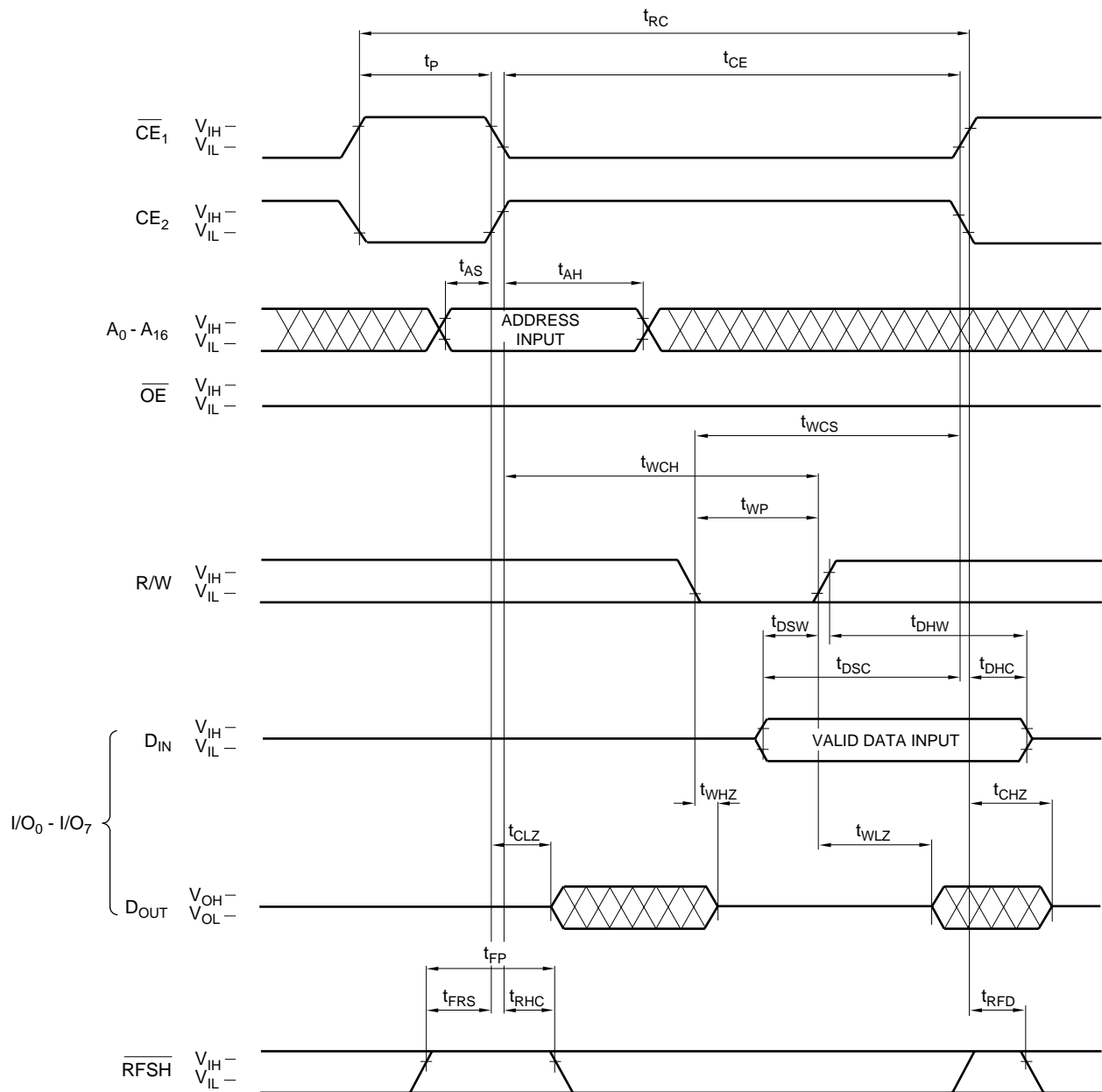
Figure 6. Write Cycle 1 ( $\overline{OE}$  = HIGH)



**NOTE:** Operation possible using only  $\overline{CE}_2$  ( $\overline{CE}_1$ ) by fixing  $\overline{CE}_1$  to LOW ( $\overline{CE}_2$  to HIGH).

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**Figure 7. Write Cycle 2 (OE Clock)**

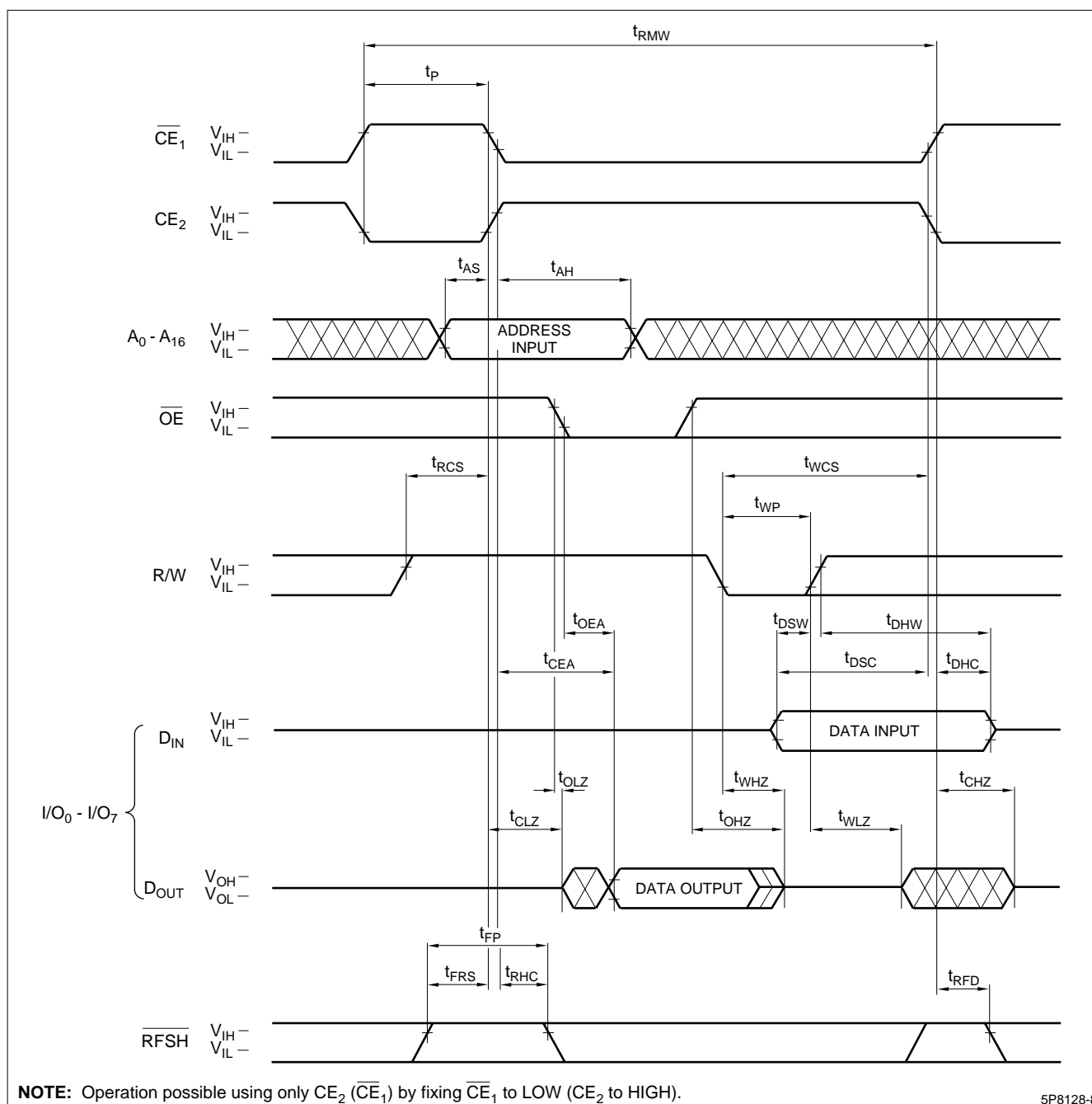


**NOTE:** Operation possible using only  $CE_2$  ( $\overline{CE}_1$ ) by fixing  $\overline{CE}_1$  to LOW ( $CE_2$  to HIGH).

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**Figure 8. Write Cycle 3 (OE = LOW)**





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Figure 9. Read-Modify-Write Cycle

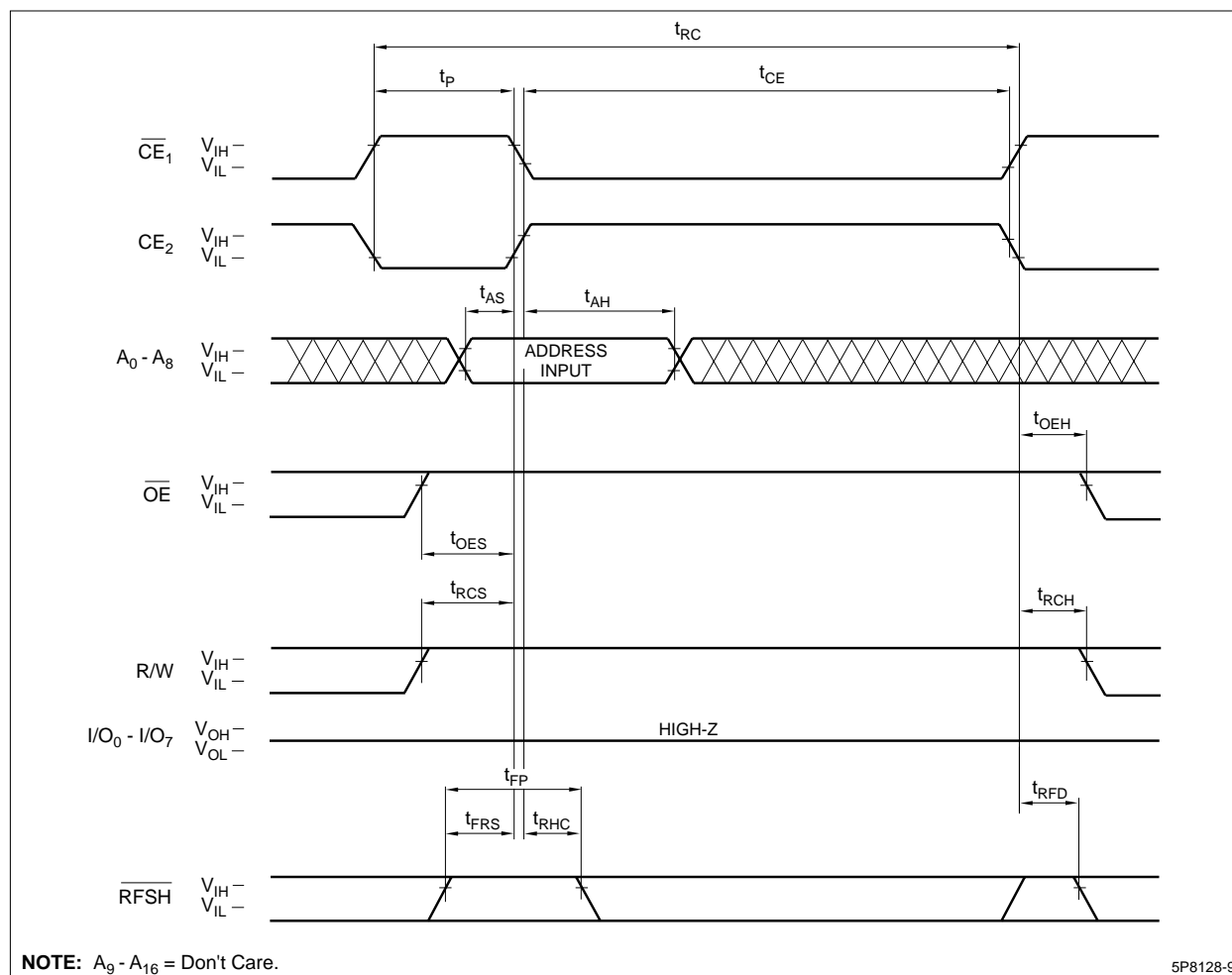


Figure 10. CE Only Refresh

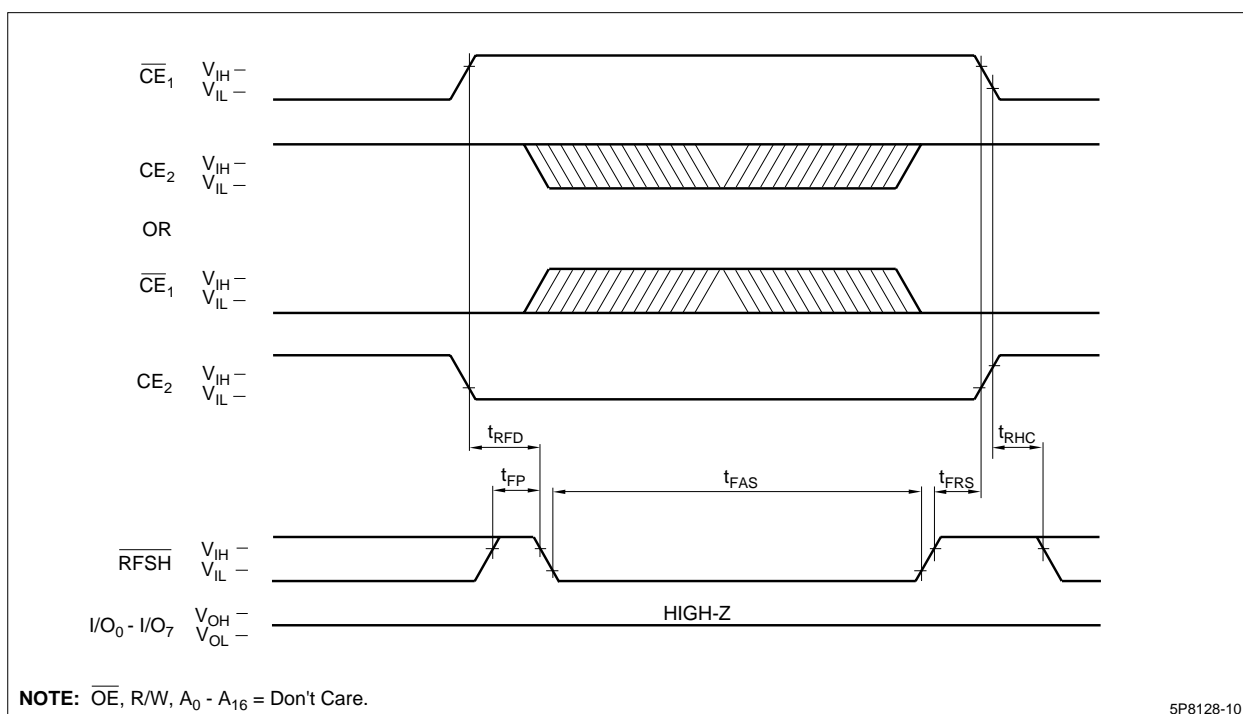


Figure 11. Self Refresh Cycle

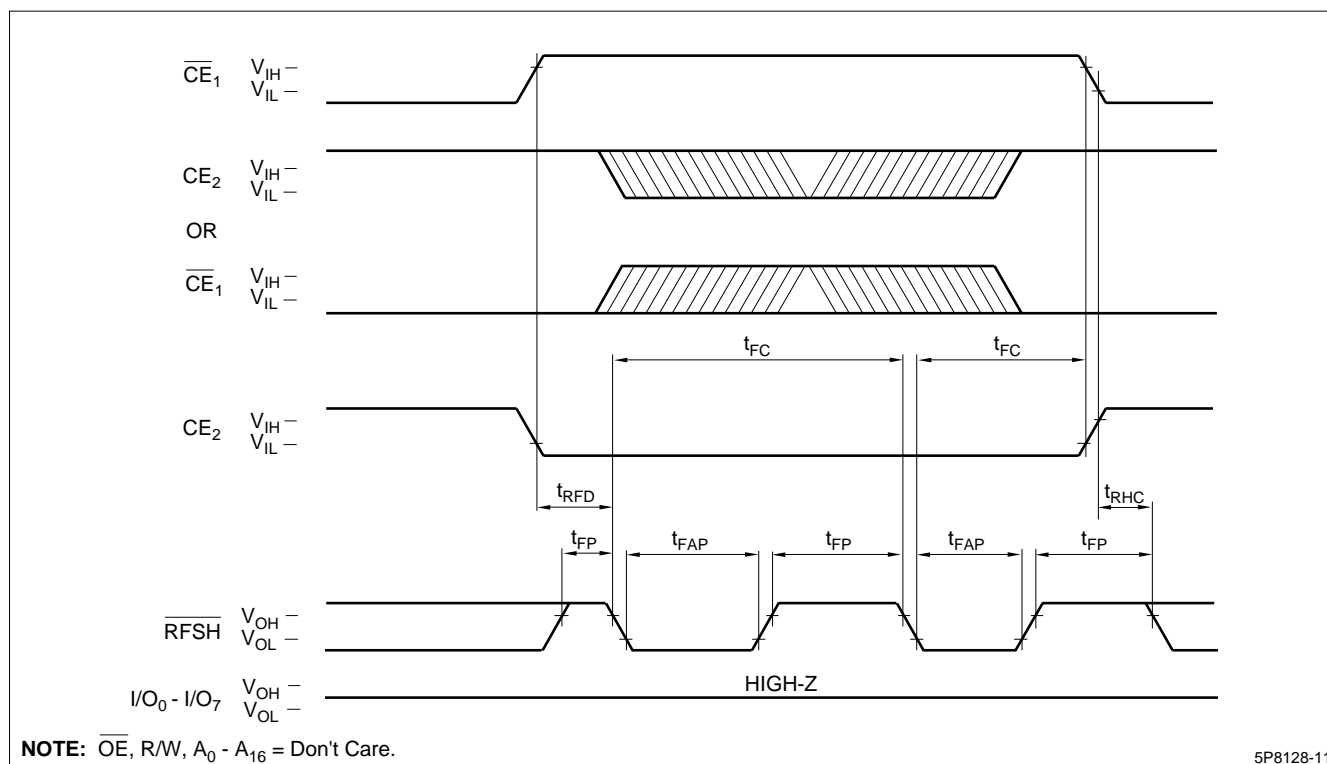
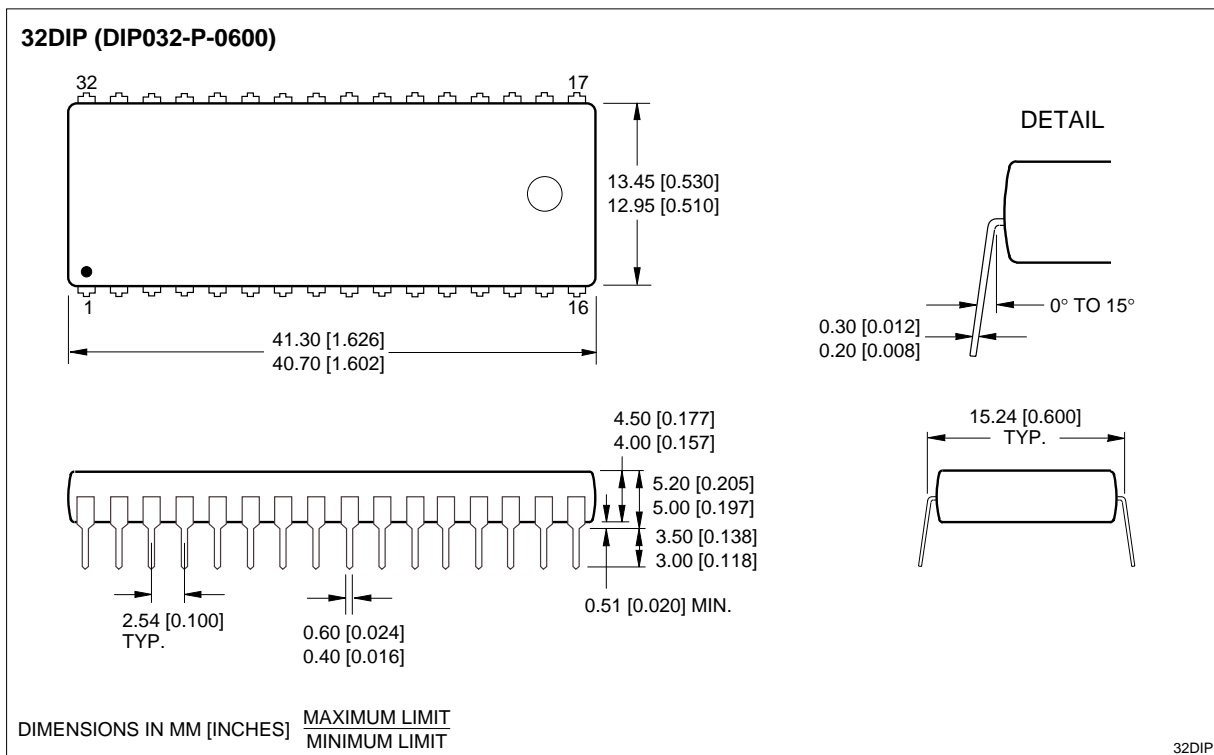
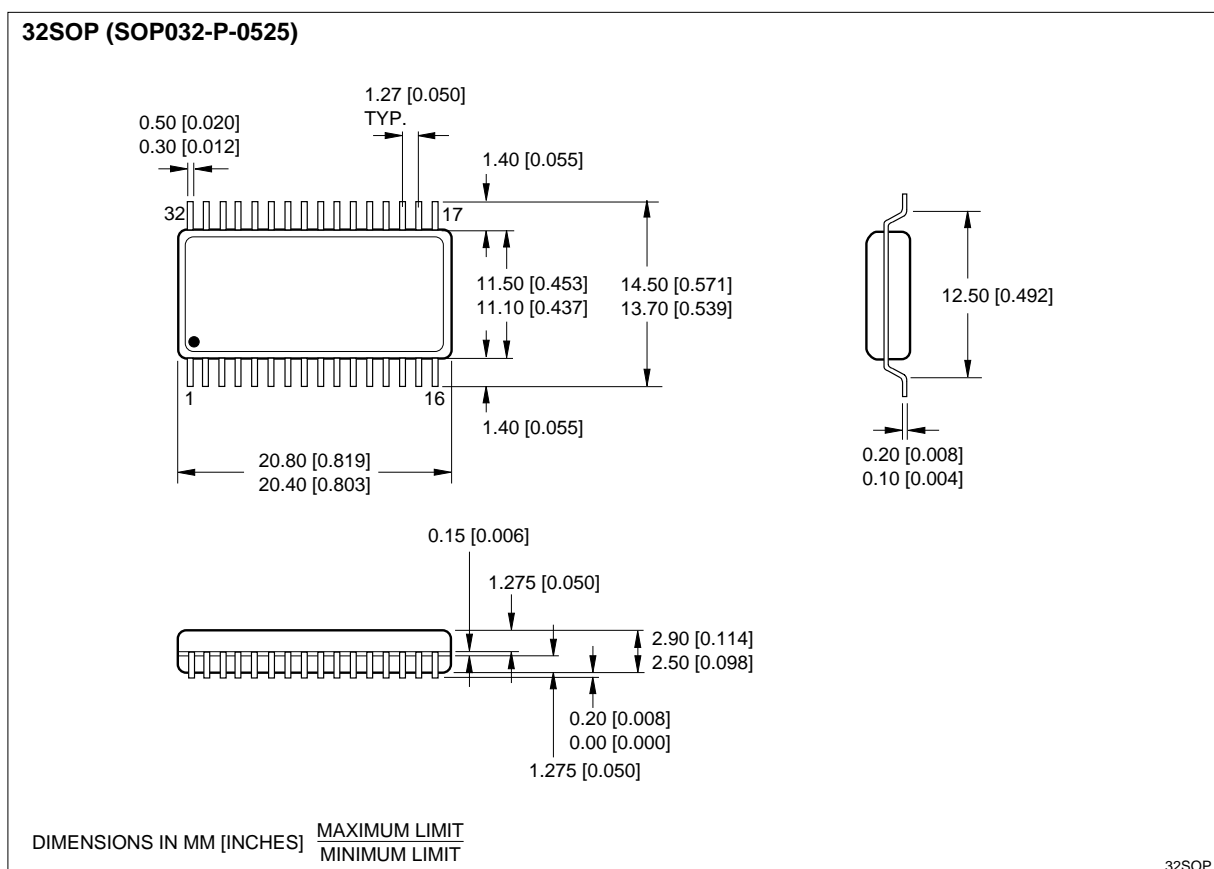


Figure 12. Auto Refresh Cycle

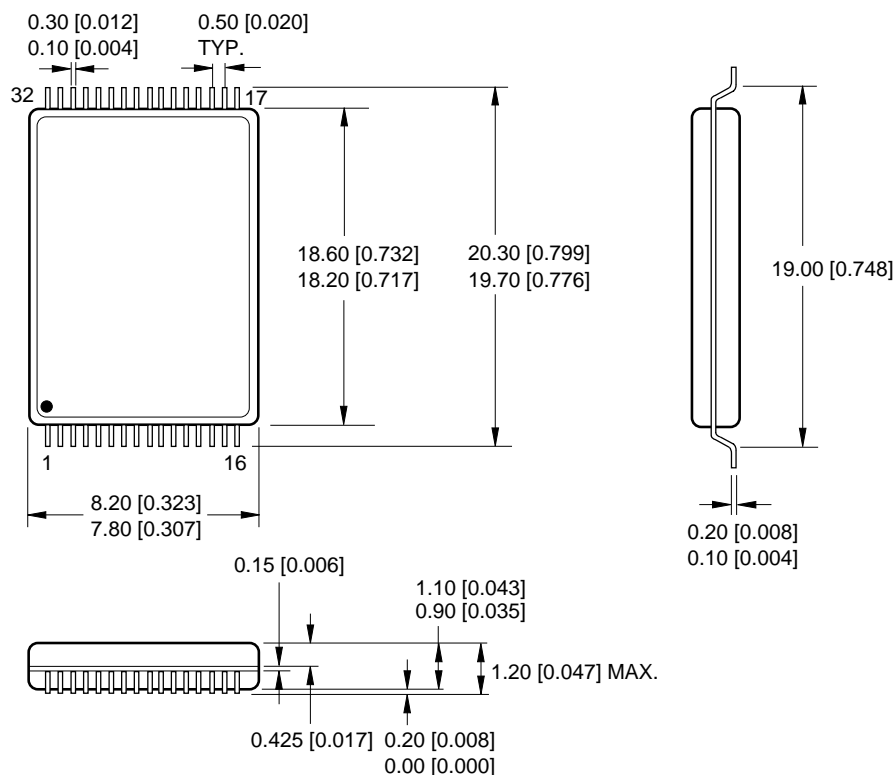
## PACKAGE DIAGRAMS



32-pin, 600-mil DIP



32-pin, 525-mil SOP

**32TSOP (Type I) (TSOP032-P-0820)**

DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

32TSOP

**32-pin, 8 × 20 mm<sup>2</sup> TSOP (Type I)****ORDERING INFORMATION**

LH5P8128	X	- ##	
Device Type	Package	Speed	
		60 60	
		80 80	Access Time (ns)
		10 100	
		Blank	32-pin, 600-mil DIP (DIP032-P-0600)
		N	32-pin, 525-mil SOP (SOP032-P-0525)
		T	32-pin, 8 x 20 mm <sup>2</sup> TSOP (Type I) (TSOP032-P-0820)
		TR	32-pin, 8 x 20 mm <sup>2</sup> TSOP (Type I) Reverse bend (TSOP032-P-0820)
			CMOS 1M (128K x 8) Pseudo-Static RAM

**Example:** LH5P8128N-60 (CMOS 1M (128K x 8) Pseudo-Static RAM, 60 ns, 32-pin, 525-mil SOP)

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