

# LRS1329

## Stacked Chip

16M Flash and 2M SRAM

(Model No.: LRS1329)

Spec No.: MFM2-J11601

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## Part 1 Overview

## 1. Description

The LRS1329 is a combination memory organized as 1M x16/2M x8 bit flash memory and 256K x8 bit static RAM in one package.

## Features

- Power supply . . . . . 2.7 V to 3.6 V
- Operating temperature . . . . . -25 °C to +85 °C
- Not designed or rated as radiation hardened
- 72 pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

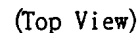
## Flash Memory

- Access Time . . . . . 100 ns (Max.)
- Operating current (The current for F-V<sub>cc</sub> pin)
  - Read . . . . . 25 mA (Max. t<sub>cycle</sub>=200ns)
  - Word/Byte write . . . . . 17 mA (Max.)
  - Block erase . . . . . 17 mA (Max.)
- Deep power down current (The current for F-V<sub>cc</sub> pin) . . . . . 10 μA (Max. F- $\overline{\text{CE}} \geq \text{F-V}_{\text{cc}} - 0.2\text{V}$ ,  
F-RP ≤ 0.2V, F-V<sub>pp</sub> ≤ 0.2V)
- Optimized Array Blocking Architecture
  - Two 4K-word/8K-byte Boot Blocks/ Six 4K-word/8K-byte Parameter Blocks/
  - Thirty-one 32K-word/64K-byte Main Blocks/ Top Boot Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte write Suspend to Read
  - Block Erase Suspend to Word/Byte write
  - Block Erase Suspend to Read

## SRAM

- Access Time . . . . . 85 ns (Max.)
- Operating current . . . . . 30 mA (Max.)
  - . . . . . 3 mA (Max. t<sub>RC</sub>, t<sub>WC</sub>=1 μs)
- Standby current . . . . . 15 μA (Max.)
- Data retention current . . . . . 15 μA (Max.)

## INDEX



From  $T_1$  to  $T_4$  pins need to be open.

Pin	Description	
A <sub>0</sub> to A <sub>16</sub>	Address Inputs (Common)	
F-A <sub>1</sub> , F-A <sub>17</sub> to F-A <sub>18</sub>	Address Inputs (Flash) F-A <sub>1</sub> : Not used in x16 mode.	
S-A <sub>17</sub>	Address Input (SRAM)	
F-CE	Chip Enable (Flash)	
S-CE <sub>1</sub> , S-CE <sub>2</sub>	Chip Enable (SRAM)	
F-WE	Write Enable (Flash)	
S-WE	Write Enable (SRAM)	
F-OE	Output Enable (Flash)	
S-OE	Output Enable (SRAM)	
F-RP	Reset/Deep Power Down (Flash) Block erase and Word/Byte Write: V <sub>IH</sub> or V <sub>IH</sub> Read: V <sub>IH</sub> or V <sub>IH</sub> Deep Power Down: V <sub>IL</sub>	
F-WP	Write Protect (Flash) Two Boot Blocks Locked: V <sub>IL</sub> (With F-RP=V <sub>IH</sub> Erase/Write can operate to all block)	
F-BYTE	Byte Enable (Flash); x8 mode: V <sub>IL</sub> , x16 mode: V <sub>IH</sub>	
F-RY/BY	Ready/Busy (Flash) During an Erase or Write operation: V <sub>OL</sub> Block Erase and Word/Byte Write Suspend: High-Z Deep Power Down: V <sub>OH</sub>	
DQ <sub>0</sub> to DQ <sub>7</sub>	Data Input/Outputs (Common)	
F-DQ <sub>8</sub> to F-DQ <sub>15</sub>	Data Inputs/Outputs (Flash); Not used in x8 mode.	
F-V <sub>CC</sub>	Power Supply (Flash)	
S-V <sub>CC</sub>	Power Supply (SRAM)	
F-V <sub>PP</sub>	Write, Erase Power Supply (Flash) Block Erase and Word/Byte Write: F-V <sub>PP</sub> =V <sub>PPLK</sub> All Blocks Locked: F-V <sub>PP</sub> <V <sub>PPLK</sub>	
F-GND	GND (Flash)	
S-GND	GND (SRAM)	
NC	No Connect	
T <sub>1</sub> to T <sub>4</sub>	Test pins (Should be open)	

3. Truth Table (\*1)

Flash	SRAM	Note	F- $\overline{CE}$	F- $\overline{RP}$	F- $\overline{OE}$	F- $\overline{WE}$	S- $\overline{CE}_1$	S- $\overline{CE}_2$	S- $\overline{OE}$	S- $\overline{WE}$	F-BYTE <sub>to DQ<sub>7</sub></sub>	DQ <sub>0</sub> to DQ <sub>7</sub>	F-DQ <sub>4</sub> to F-DQ <sub>5</sub>
Read	Standby	*4.5	L	H	L	H	*7	X	X	H	DOUT		
Output Disable					H					L	DOUT	High-Z	
						H				L	High-Z		
Write		*2, 3, 4			L	H				DIN			
										L	DIN	High-Z	
Standby	Read	*6	H	H	X	X	L	H	H	X	DOUT	High-Z	
	Output Disable	*6									High-Z		
	Write	*6									DIN		
Reset Power Down	Read	*6	X	L	X	X	L	H	H	X	DOUT	High-Z	
	Output Disable	*6									High-Z		
	Write	*6									DIN		
Standby	Standby	*6	H	H	X	X	*7	X	X	X	High-Z		
Reset Power Down		*6	X	L									

Notes) \*1. L= $V_{IL}$ , H= $V_{IH}$ , X=H or L. Refer to DC Characteristics.

\*2. Command writes involving block erase or word/byte write are reliably executed when  $F-V_{PP}=V_{PPH}$  and  $F-V_{CC}=2.7V$  to  $3.6V$ . Block erase or word/byte write with  $V_{IH} < F-RP < V_{IH}$  produce spurious results and should not be attempted.

\*3. Refer Section 5. Flash Memory Command Definition for valid DIN during a write operation.

\*4. Never hold F- $\overline{OE}$  low and F- $\overline{WE}$  low at the same timing.

\*5. F-A<sub>1</sub> set to  $V_{IL}$  or  $V_{IH}$  in byte mode (F-BYTE= $V_{IL}$ ).

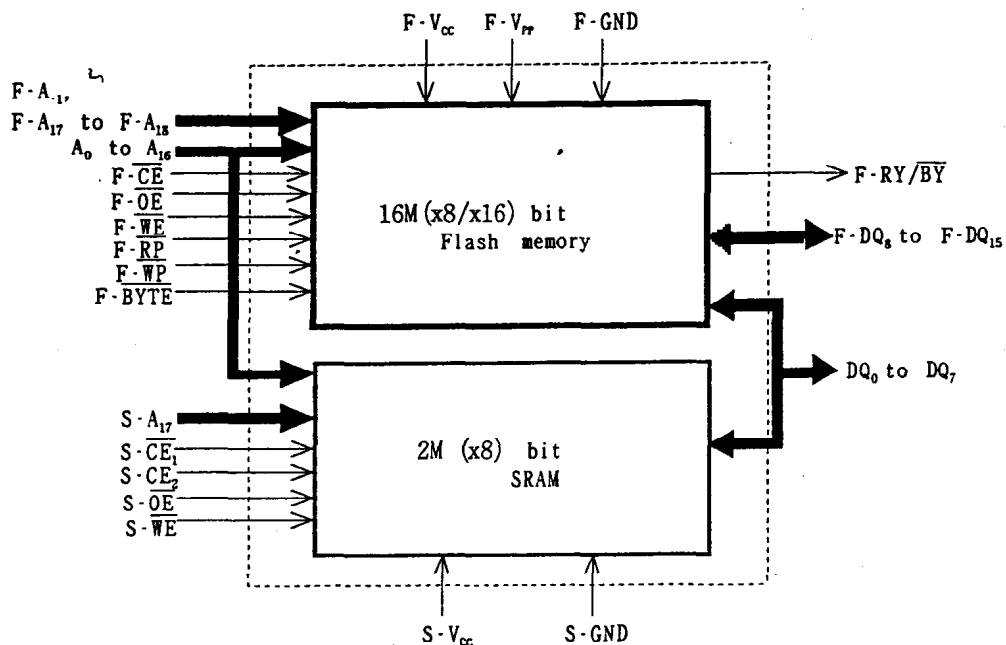
\*6. F-WP set to  $V_{IL}$  or  $V_{IH}$ .

\*7. See the following SRAM Standby mode.

SRAM Standby Mode

Mode	S- $\overline{CE}_1$	S- $\overline{CE}_2$
SRAM	H	X
Standby	X	L

## 4. Block Diagram



## 5 Command Definitions for Flash Memory (\*1)

Command	Bus Cycles Req'd.	Note	First Bus Cycle			Second Bus Cycle		
			Oper (*2)	Address (*3)	Data (*3)	Oper (*2)	Address (*3)	Data (*3)
Read Array/Reset	1		Write	XA	FFH			
Read Identifier Codes	$\geq 2$	*4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	*5	Write	BA	20H	Write	BA	DOH
Word/Byte Write	2	*5	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	*5	Write	XA	BOH			
Block Erase and Word/Byte Write Resume	1	*5	Write	XA	DOH			

## Note)

- \*1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
- \*2. BUS operations are defined in 3. Truth Table.
- \*3. XA=Any valid address within the device.  
IA=Identifier Code Address.  
BA=Address within the block being erased.  
WA=Address of memory location to be written.  
SRD=Data read from status register (See the next page "Status Register Definition").  
WD=Data to be written at location WA. Data is latched on the rising edge of  $\overline{F\text{-}WE}$  or  $\overline{F\text{-}CE}$  (whichever goes high first).  
ID=Data read from identifier codes.
- \*4. See the Following Identifier Codes.
- \*5. See the following Write Protection Alternatives.

## Identifier Codes

Codes	Address [A <sub>18</sub> -A <sub>0</sub> ]	Data [DQ <sub>7</sub> -DQ <sub>0</sub> ]
Manufacture Code	00000H	BOH
Device Code	00001H	48H

## Write Protection Alternatives

Operation	F-V <sub>PP</sub>	F- $\overline{RP}$	F- $\overline{WP}$	Effect
Block Erase or Word/Byte Write	V <sub>IL</sub>	X	X	All Blocks Locked.
	>V <sub>PPLK</sub>	V <sub>IL</sub>	X	All Blocks Locked.
		V <sub>IH</sub>	X	All Blocks Unlocked.
		V <sub>IH</sub>	V <sub>IL</sub>	2 Boot Blocks Locked.
		V <sub>IH</sub>	V <sub>IH</sub>	All Blocks Unlocks.

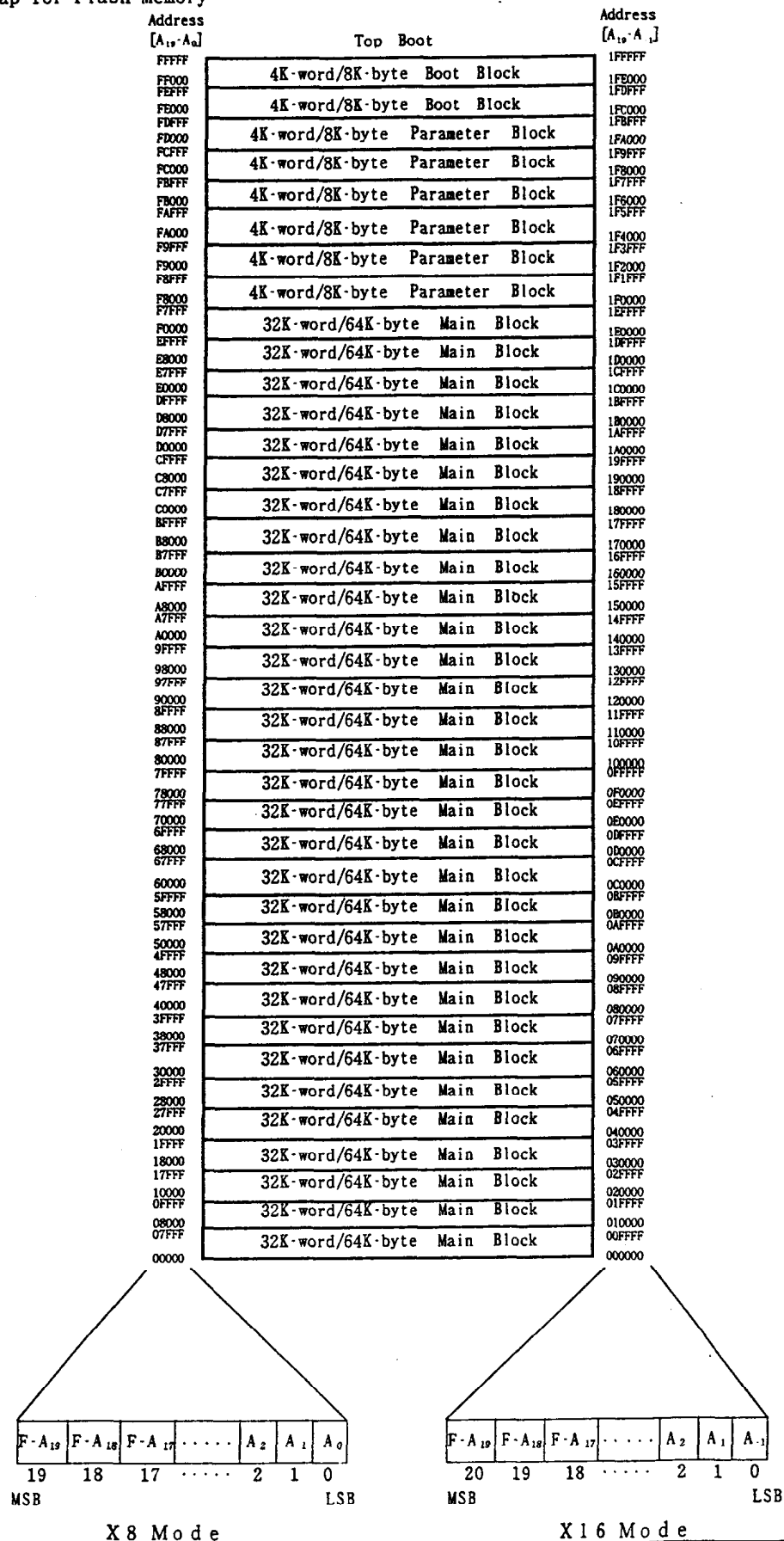
## 6. Status Register Definition

WSMS	ESS	ES	WBWS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

<p>S R. 7 = WRITE STATE MACHINE STATUS ( WSMS )  1 = Ready  0 = Busy</p> <p>S R. 6 = ERASE SUSPEND STATUS ( ESS )  1 = Block Erase Suspended  0 = Block Erase in Progress/Completed</p> <p>S R. 5 = ERASE STATUS ( ES )  1 = Error in Block Erasure  0 = Successful Block Erase</p> <p>S R. 4 = WORD/BYTE WRITE STATUS ( WBWS )  1 = Error in Word/Byte Write  0 = Successful Word/Byte Write</p> <p>S R. 3 = <math>V_{PP}</math> STATUS ( VPPS )  1 = <math>F-V_{PP}</math> Low Detect, Operation Abort  0 = <math>F-V_{PP}</math> OK</p> <p>S R. 2 = WORD/BYTE WRITE SUSPENDED STATUS ( WBWSS )  1 = Word/Byte Write Suspended  0 = Word/Byte Write in Progress/Completed</p> <p>S R. 1 = DEVICE PROTECT STATUS ( DPS )  1 = <math>F-\overline{WP}</math> or <math>F-\overline{RP}</math> Lock Detected, Operation Abort  0 = Unlock</p> <p>S R. 0 = RESERVED FOR FUTURE ENHANCEMENTS ( R )</p>	<p>NOTES:</p> <p>Check <math>RY/\overline{BY}</math> or SR.7 to determine block erase or word/byte write completion. SR.6-0 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of <math>F-V_{PP}</math> level. The WSM interrogates and indicates the <math>F-V_{PP}</math> level only after Block Erase or Word/ByteWrite command sequences. SR.3 is not guaranteed to reports accurate feedback only when <math>F-V_{PP} \neq V_{PPH1/2}</math>.</p> <p>The WSM interrogates the <math>F-\overline{WP}</math> and <math>F-\overline{RP}</math> only after Block Erase or Word/ByteWrite command sequences. It informs the system, depending on the attempted operation, if the <math>F-\overline{WP}</math> is not <math>V_{IH}</math>, <math>F-\overline{RP}</math> is not <math>V_{RH}</math>.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p>
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## 7. Memory Map for Flash Memory



## 8. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1, 2)	$V_{CC}$	-0.2 to +4.6	V
Input voltage (*1, 3)	$V_{IN}$	-0.2 (*4) to $V_{CC}+0.3$	V
Operating temperature	$T_{opr}$	-25 to +85	°C
Storage temperature	$T_{stg}$	-65 to +125	°C
F- $V_{PP}$ voltage (*1)	F- $V_{PP}$	-0.2 (*4) to +14.0(*5)	V
F- $\overline{RP}$ voltage (*1)	F- $\overline{RP}$	-0.5 (*4) to +14.0(*5)	V

Notes) \*1. The maximum applicable voltage on any pins with respect to GND.

\*2. Except F- $V_{PP}$ .

\*3. Except F- $\overline{RP}$ .

\*4. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

\*5. +14.0V overshoot is allowed when the pulse width is less than 20nsec.

## 9. Recommended DC Operating Conditions

( $T_a = -25^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V
Input voltage	$V_{IH}$	2.2		$V_{CC}+0.3(*1)$	V
	$V_{IL}$	-0.2 (*2)		0.8	V
	$V_{IN}(*3)$	11.4		12.6	V

Notes) \*1.  $V_{CC}$  is the lower one of S- $V_{CC}$  and F- $V_{CC}$ .

\*2. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

\*3. This voltage is applicable to F- $\overline{RP}$  Pin only.

## 10. Pin Capacitance

( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	$C_{IN}$	$V_{IN}=0V$			20	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$			22	pF

\*1

\*1

Note) \*1 Sampled but not 100% tested

## 11. DC Characteristics

DC Characteristics ( $T_a = -25^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

Parameter		Symbol	Conditions	Min.	Typ. (*)	Max.	Unit
Input leakage current ( $I_{LI}$ )		$I_{LI}$	$V_{IN} = V_{CC}$ or GND	-1.5		+1.5	$\mu\text{A}$
Output leakage current ( $I_{LO}$ )		$I_{LO}$	$V_{OUT} = V_{CC}$ or GND	-1.5		+1.5	$\mu\text{A}$
F- $V_{CC}$	V <sub>CC</sub> Standby Current	$I_{CCS}$ (*2, 7)	$F\text{-}\overline{CE} = F\text{-}\overline{RP} = F\text{-}V_{CC} \pm 0.2\text{V}$ $F\text{-}\overline{WP} = F\text{-}V_{CC} \pm 0.2\text{V}$ or $F\text{-}GND \pm 0.2\text{V}$		25	50	$\mu\text{A}$
			$F\text{-}\overline{CE} = F\text{-}\overline{RP} = V_{IH}$ $F\text{-}\overline{WP} = V_{IH}$ or $V_{IL}$		0.2	2	mA
	Deep Power-Down Current	$I_{CCD}$ (*7)	$F\text{-}\overline{RP} = F\text{-}GND \pm 0.2\text{V}$ , $I_{OUT} (F\text{-}RY/\overline{BY}) = 0\text{mA}$		5	10	$\mu\text{A}$
	V <sub>CC</sub> Read Current	$I_{CCR}$ (*3, 4)	CMOS Input $F\text{-}\overline{CE} = F\text{-}GND$ , $f = 5\text{MHz}$ , $I_{OUT} = 0\text{mA}$			25	mA
			TTL Input $F\text{-}\overline{CE} = F\text{-}GND$ , $f = 5\text{MHz}$ , $I_{OUT} = 0\text{mA}$			30	mA
	V <sub>CC</sub> Word/Byte Write Current	$I_{CCW}$	$F\text{-}V_{PP} = V_{PPH}$			17	mA
	V <sub>CC</sub> Block Erase Current	$I_{CCE}$	$F\text{-}V_{PP} = V_{PPH}$			17	mA
F- $V_{PP}$	V <sub>CC</sub> Word/Byte Write Block Erase Suspend Current	$I_{CCWS}$ $I_{CCES}$	$F\text{-}\overline{CE} = V_{IH}$			6	mA
	V <sub>PP</sub> Standby or Read Current	$I_{PPS}$ $I_{PPR}$	$F\text{-}V_{PP} = F\text{-}V_{CC}$		$\pm 2$	$\pm 15$	$\mu\text{A}$
			$F\text{-}V_{PP} > F\text{-}V_{CC}$		10	200	$\mu\text{A}$
	V <sub>PP</sub> Deep Power-Down Current	$I_{PPD}$	$F\text{-}\overline{RP} = F\text{-}GND \pm 0.2\text{V}$		0.1	5	$\mu\text{A}$
	V <sub>PP</sub> Word/Byte Write Current	$I_{PPW}$	$F\text{-}V_{PP} = V_{PPH}$		12	40	mA
	V <sub>PP</sub> Block Erase Current	$I_{PPE}$	$F\text{-}V_{PP} = V_{PPH}$		8	25	mA
	V <sub>PP</sub> Word/Byte Write or Block Erase Suspend Current	$I_{PPWS}$ $I_{PPES}$	$F\text{-}V_{PP} = V_{PPH}$		10	200	$\mu\text{A}$
S- $V_{CC}$	Standby Current	$I_{SB}$	$S\text{-}\overline{CE}_1, S\text{-}\overline{CE}_2 \geq S\text{-}V_{CC} - 0.2\text{V}$ or $S\text{-}\overline{CE}_2 \leq 0.2\text{V}$			15	$\mu\text{A}$
		$I_{SBI}$	$S\text{-}\overline{CE}_1 = V_{IH}$ or $S\text{-}\overline{CE}_2 = V_{IL}$			3.0	mA
	Operation Current	$I_{CC1}$	$S\text{-}\overline{CE}_1 = V_{IL}$ , $S\text{-}\overline{CE}_2 = V_{IH}$ $V_{IN} = V_{IL}$ or $V_{IH}$	$t_{CYCLE} = \text{Min.}$ $I_{I/O} = 0\text{mA}$		30	mA
		$I_{CC2}$	$S\text{-}\overline{CE}_1 = 0.2\text{V}$ , $S\text{-}\overline{CE}_2 = S\text{-}V_{CC} - 0.2\text{V}$ $V_{IN} = S\text{-}V_{CC} - 0.2\text{V}$ or $0.2\text{V}$	$t_{CYCLE} = 1\mu\text{s}$ $I_{I/O} = 0\text{mA}$		3	mA

## DC Characteristics (Continue)

(T<sub>a</sub> = -25°C to +85°C, V<sub>cc</sub> = 2.7 V to 3.6 V)

Parameter	Symbol	Test Conditions	Min.	Typ (*1)	Max.	Unit
Input Low Voltage	V <sub>IL</sub>		-0.2		0.8	V
Input High Voltage	V <sub>IH</sub>		2.2		V <sub>cc</sub> +0.3	V
Output Low Voltage	V <sub>OL</sub> (*2)	I <sub>OL</sub> = 2.0 mA			0.4	V
Output High Voltage	V <sub>OHI</sub> (*2)	I <sub>OHI</sub> = -1.0 mA	2.4			V
F-V <sub>pp</sub> Lockout during Normal Operations	V <sub>PPLK</sub> (*5)				1.5	V
F-V <sub>pp</sub> Word/Byte Write or Block Erase Operations	V <sub>PPH</sub>		2.7		3.6	V
F-V <sub>cc</sub> Lockout Voltage	V <sub>LKO</sub>		1.5			V
F-RP Unlock Voltage	V <sub>HH</sub> (*6)	Unavailable F-WP	11.4		12.6	V

## Notes)

- Reference values at V<sub>cc</sub>=3.0V and T<sub>a</sub>=+25°C.
- Includes F-RY/BY.
- Automatic Power Savings (APS) for Flash Memory reduces typical I<sub>CCR</sub> to 3mA at 2.7V V<sub>cc</sub> in static operation.
- CMOS inputs are either V<sub>cc</sub> ±0.2V or GND±0.2V. TTL inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
- Block erases and word/byte writes are inhibited when F-V<sub>pp</sub> ≤ V<sub>PPLK</sub> and not guaranteed in the range between V<sub>PPLK</sub> (max) and V<sub>PPH</sub> (min), and above V<sub>PPH</sub> (max).
- F-RP connection to a V<sub>HH</sub> supply is allowed for a maximum cumulative period of 80 hours.
- F-BYTE is V<sub>cc</sub>±0.2V in word mode and is GND±0.2V in byte mode.  
F-WP is V<sub>cc</sub>±0.2V or GND±0.2V.

## 12. Flash memory AC Characteristics

## AC Test Conditions

Input pulse level	0 V to 2.7 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.35 V
Output load	1TTL+C <sub>L</sub> (30pF)

## Read Cycle

(T<sub>a</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.6V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t <sub>AVAV</sub>	100		ns	
Address to Output Delay	t <sub>AVQV</sub>		100	ns	
F- $\overline{\text{CE}}$ to Output Delay	t <sub>ELQV</sub>		100	ns	*1
F- $\overline{\text{RP}}$ High to Output Delay	t <sub>PHQV</sub>		10	μs	
F- $\overline{\text{OE}}$ to Output Delay	t <sub>GLQV</sub>		45	ns	*1
F- $\overline{\text{CE}}$ to Output in Low Z	t <sub>ELQX</sub>	0		ns	
F- $\overline{\text{CE}}$ High to Output in High Z	t <sub>EHQZ</sub>		45	ns	
F- $\overline{\text{OE}}$ to Output in Low Z	t <sub>GLQX</sub>	0		ns	
F- $\overline{\text{OE}}$ High to Output in High Z	t <sub>GHQZ</sub>		20	ns	
Output Hold from Address, F- $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ Change, Whichever Occurs First	t <sub>OH</sub>	0		ns	
F-BYTE and A <sub>1</sub> to Output Delay	t <sub>FVQV</sub>		90	ns	
F-BYTE Low to Output in High Z	t <sub>FLQZ</sub>		30	ns	
F- $\overline{\text{CE}}$ to F-BYTE High Z or Low	t <sub>ELFV</sub>		5	ns	

Notes) \*1. F- $\overline{\text{OE}}$  may be delayed up to t<sub>ELQV</sub>-t<sub>GLQV</sub> after the falling edge of F- $\overline{\text{OE}}$  without impact on t<sub>ELQV</sub>.Write Cycle (F- $\overline{\text{WE}}$  Controlled) (\*2)(T<sub>a</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.6V)

Parameter	Sym.	Min.	Max.	Unit	
Write Cycle Time	t <sub>AVAV</sub>	100		ns	
F- $\overline{\text{RP}}$ High Recovery to F- $\overline{\text{WE}}$ going to Low	t <sub>PHWL</sub>	10		μs	
F- $\overline{\text{CE}}$ Setup to F- $\overline{\text{WE}}$ Going Low	t <sub>ELWL</sub>	0		ns	
F- $\overline{\text{WE}}$ Pulse Width	t <sub>WLWH</sub>	50		ns	
F- $\overline{\text{RP}}$ V <sub>HH</sub> Setup to F- $\overline{\text{WE}}$ Going High	t <sub>PHHWH</sub>	100		ns	
F- $\overline{\text{WP}}$ V <sub>HH</sub> Setup to F- $\overline{\text{WE}}$ Going High	t <sub>SHWH</sub>	100		ns	
F-V <sub>PP</sub> Setup to F- $\overline{\text{WE}}$ Going High	t <sub>VPWH</sub>	100		ns	
Address Setup to F- $\overline{\text{WE}}$ Going High	t <sub>AVWH</sub>	50		ns	*3
Data Setup to F- $\overline{\text{WE}}$ Going High	t <sub>DVWH</sub>	50		ns	*3
Data Hold from F- $\overline{\text{WE}}$ High	t <sub>WHDX</sub>	0		ns	
Address Hold from F- $\overline{\text{WE}}$ High	t <sub>WHAX</sub>	0		ns	
F- $\overline{\text{CE}}$ Hold from F- $\overline{\text{WE}}$ High	t <sub>WHCH</sub>	0		ns	
F- $\overline{\text{WE}}$ Pulse Width High	t <sub>WHWL</sub>	30		ns	
F- $\overline{\text{WE}}$ High to F-RY/ $\overline{\text{BY}}$ Going Low	t <sub>WHRL</sub>		100	ns	
Write Recovery before Read	t <sub>WHGL</sub>	0		ns	
F-V <sub>PP</sub> Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High Z	t <sub>QVVL</sub>	0		ns	
F- $\overline{\text{RP}}$ V <sub>HH</sub> Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High Z	t <sub>QVPH</sub>	0		ns	
F- $\overline{\text{WP}}$ V <sub>HH</sub> Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High	t <sub>QVSL</sub>	0		ns	
F-BYTE Setup to F- $\overline{\text{WE}}$ Going High	t <sub>FVWH</sub>	50		ns	
F-BYTE Hold from F- $\overline{\text{WE}}$ High	t <sub>WHFV</sub>	100		ns	

## Write Cycle (F-CE Controlled) (\*2)

(T<sub>i</sub> = -25°C to +85°C, V<sub>cc</sub> = 2.7V to 3.6V)

Parameter	Sym.	Min.	Max.	Unit
Write Cycle Time	t <sub>AVAV</sub>	100		ns
F-RP High Recovery to F-CE going to Low	t <sub>PHL</sub>	10		μs
F-WE Setup to F-CE Going Low	t <sub>WLEL</sub>	0		ns
F-CE Pulse Width	t <sub>ELFH</sub>	70		ns
F-RP V <sub>ih</sub> Setup to F-CE Going High	t <sub>PHHH</sub>	100		ns
F-WP V <sub>ih</sub> Setup to F-CE Going High	t <sub>SHHH</sub>	100		ns
F-Vpp Setup to F-CE Going High	t <sub>VPEH</sub>	100		ns
Address Setup to F-CE Going High	t <sub>AVEH</sub>	50		ns
Data Setup to F-CE Going High	t <sub>DVEH</sub>	50		ns
Data Hold from F-CE High	t <sub>EHDX</sub>	0		ns
Address Hold from F-CE High	t <sub>EHAX</sub>	0		ns
F-WE Hold from F-CE High	t <sub>ENWH</sub>	0		ns
F-CE Pulse Width High	t <sub>EHHL</sub>	25		ns
F-CE High to F-RY/BY Going Low	t <sub>EHRL</sub>		100	ns
Write Recovery before Read	t <sub>ENGL</sub>	0		ns
F-Vpp Hold from Valid SRD, F-RY/BY High Z	t <sub>QVVL</sub>	0		ns
F-RP V <sub>ih</sub> Hold from Valid SRD, F-RY/BY High Z	t <sub>QVPH</sub>	0		ns
F-WP V <sub>ih</sub> Hold from Valid SRD, F-RY/BY High	t <sub>QVSL</sub>	0		ns
F-BYTE Setup to F-CE Going High	t <sub>FVEH</sub>	50		ns
F-BYTE Hold from F-CE High	t <sub>ENFV</sub>	100		ns

\*3

\*3

Notes) \*2. Read timing characteristics during block erase and word/byte write operations are the same as during read-only operations. Refer to AC Characteristics for Read Cycle.

\*3. Refer to Section 5. Flash Memory Command Definition for valid AIN and DIN for block erase or word/byte write.

Block Erase and Word/Byte Write Performance(T<sub>a</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7 V to 3.6 V)

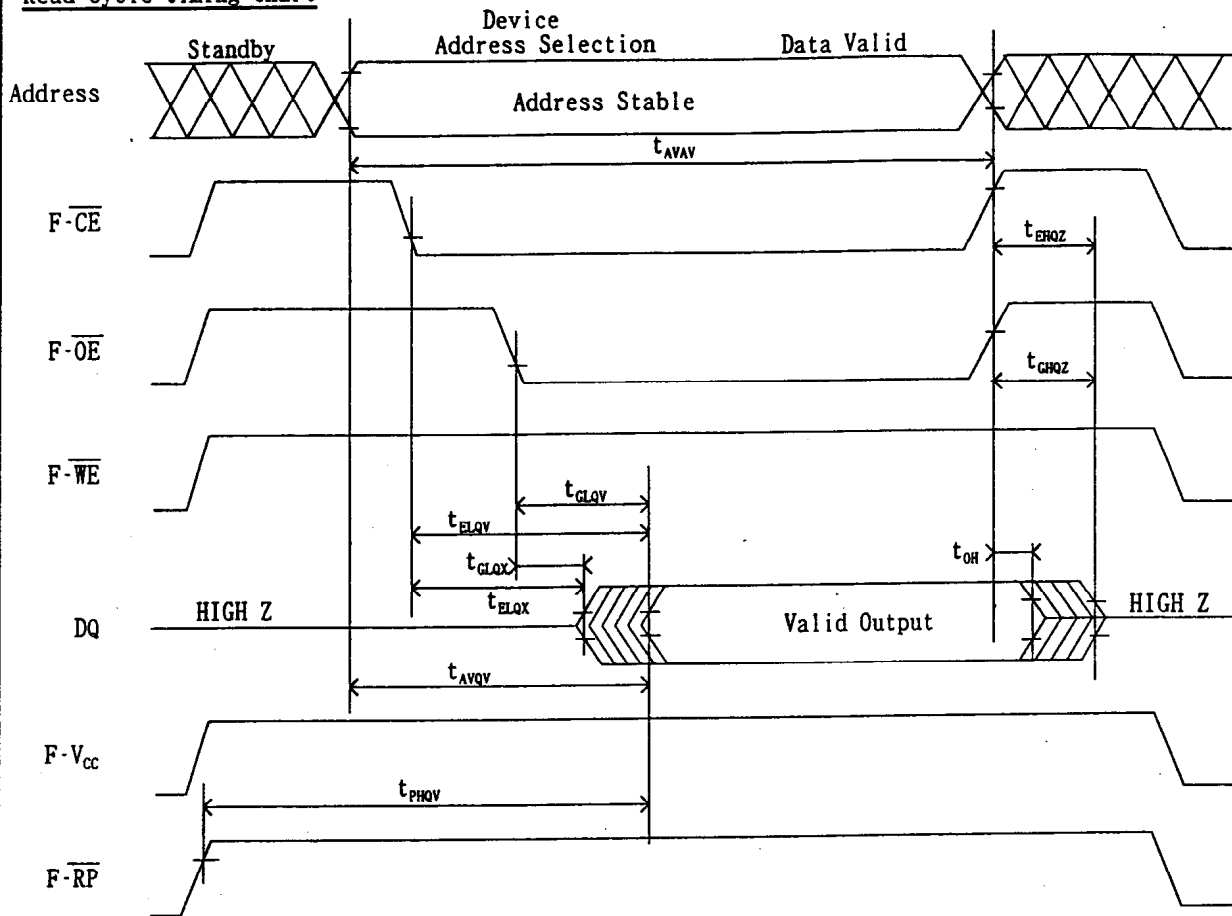
Sym.	Parameter		V <sub>DD</sub> = 2.7 V to 3.6 V			Unit	
			Min.	Typ. <sup>(*)</sup>	Max.		
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Word/Byte Write Time	32K-word Block /64K-byte Block		55		μs	*5
		4K-word Block /8K-byte Block		60		μs	*5
	Block Write Time (at word mode)	32K-word Block		1.8		s	*5
		4K-word Block		0.3			
	Block Write Time (at byte mode)	64K-byte Block		3.6		s	*5
		8K-byte Block		0.6			
t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Erase Time	32K-word Block		1.2		s	*5
		64K-byte Block					
		4K-word Block /8K-byte Block		0.5		s	*5
t <sub>WHR21</sub> t <sub>EHR21</sub>	Word/Byte Write Suspend Latency Time to Read			7.5	8.6	μs	
t <sub>WHR22</sub> t <sub>EHR22</sub>	Erase Suspend Latency Time to Read			19.3	23.6	μs	

Notes) \*4. Reference values at T<sub>a</sub> = +25°C and V<sub>CC</sub> = 3.0V, V<sub>PP</sub> = 3.0V.

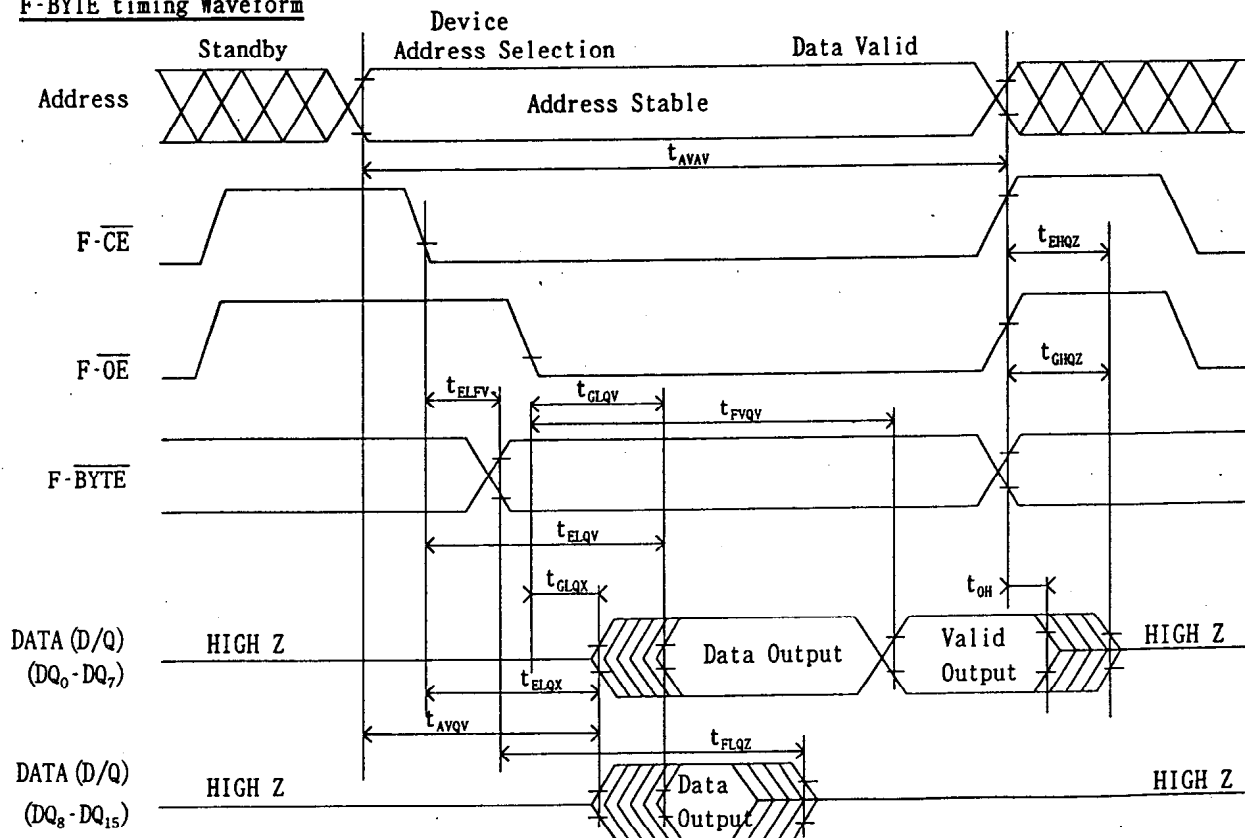
\*5. Excludes system-level overhead.

# Flash Memory AC Characteristic Timing Chart

## Read Cycle timing chart

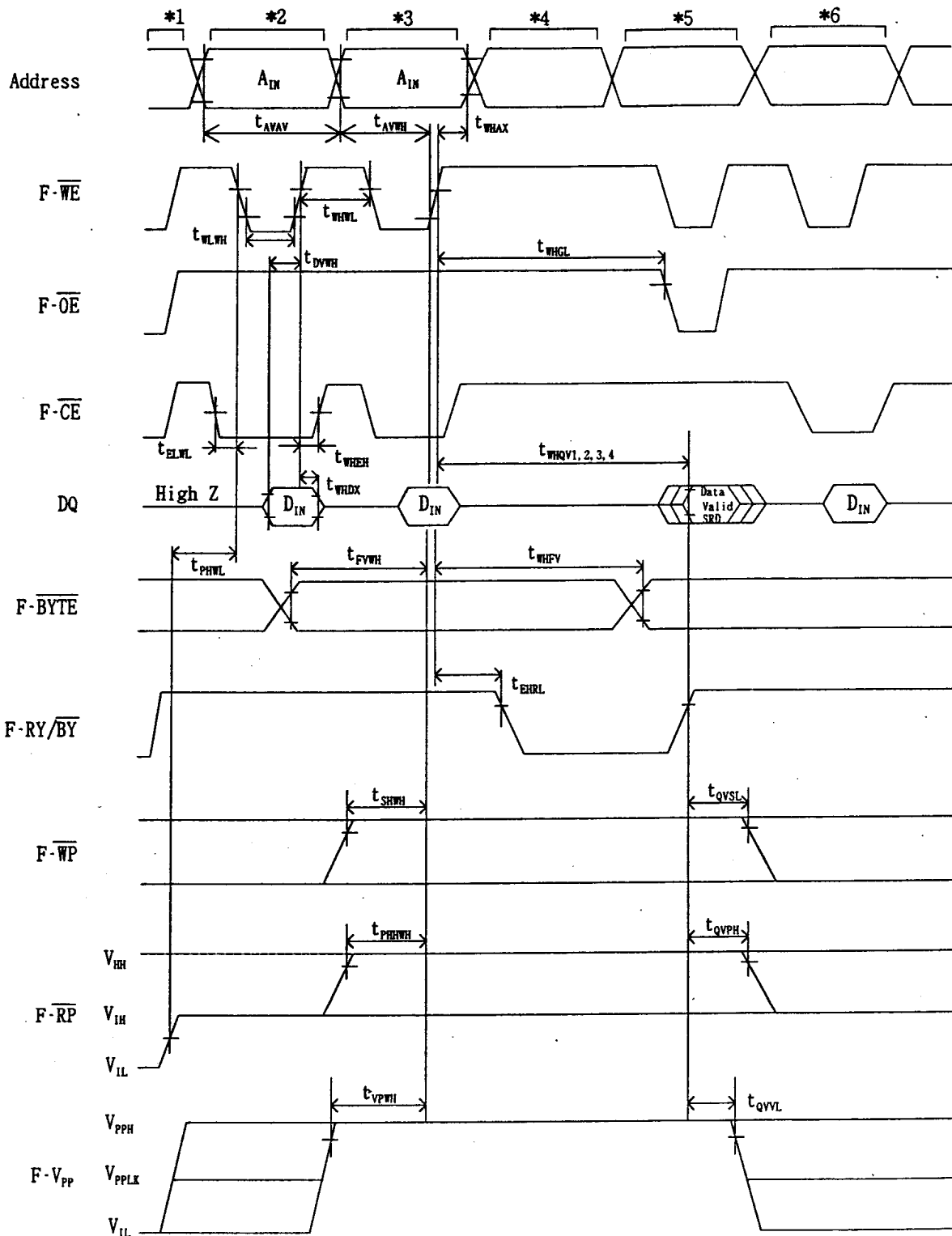


## F-BYTE timing Waveform





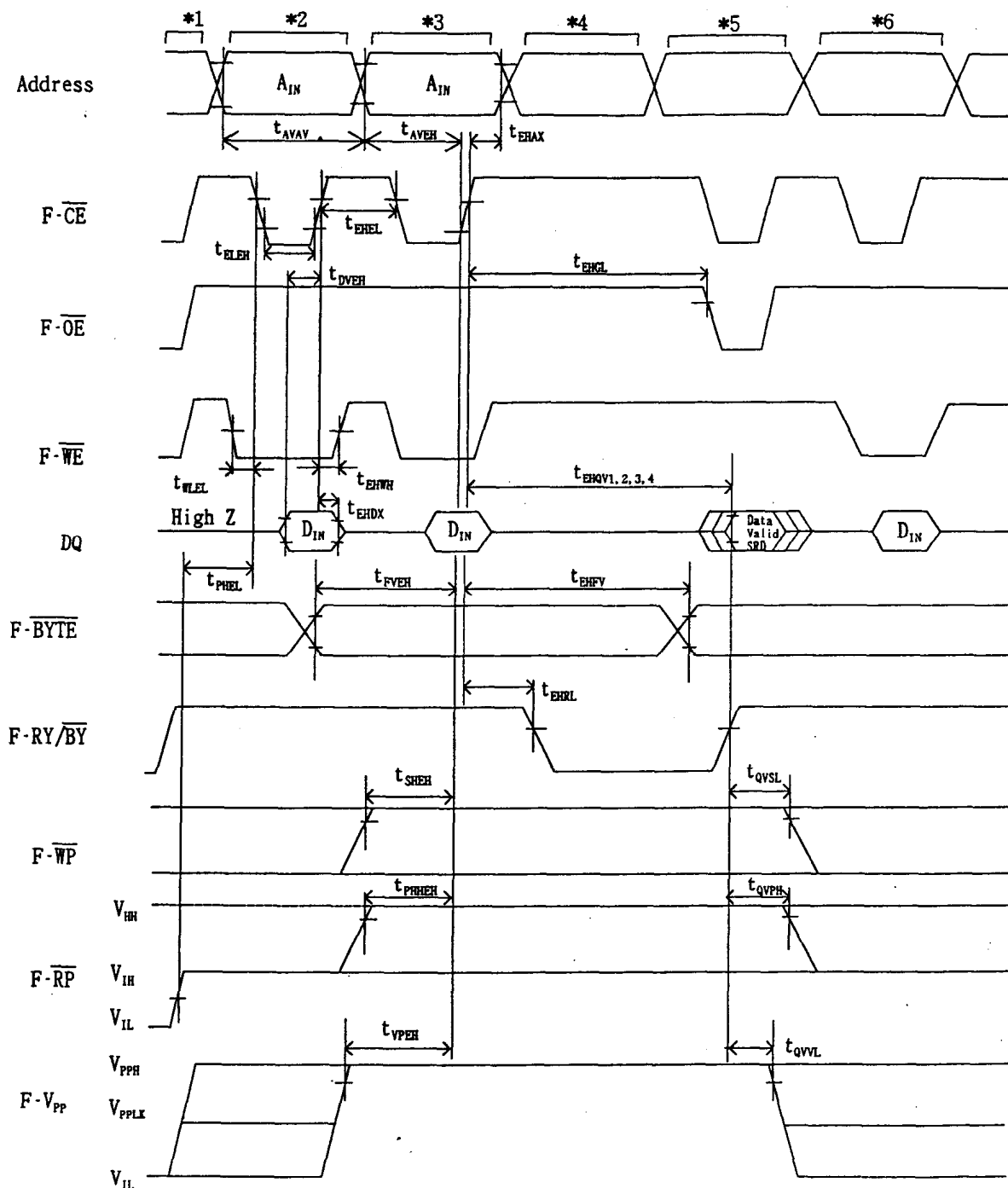
Write cycle timing chart (F-WE controlled)



## Notes:

- \*1. V<sub>CC</sub> Power-up and standby.
- \*2. Write block erase or word/byte write setup.
- \*3. Write block erase confirm or valid address and data.
- \*4. Automated erase or program delay.
- \*5. Read status register data.
- \*6. Write Read Array command.

Write cycle timing chart (F-CE controlled)



## Notes:

- \*1.  $V_{CC}$  Power-up and standby.
- \*2. Write block erase or word/byte write setup.
- \*3. Write block erase confirm or valid address and data.
- \*4. Automated erase or program delay.
- \*5. Read status register data.
- \*6. Write Read Array command.

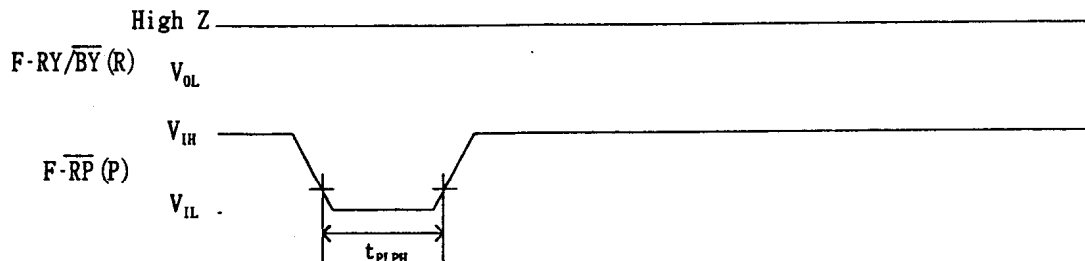
Reset Operations $(T_a = -25^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{V to } 3.6\text{V})$ 

Parameter	Sym.	Min.	Max.	Unit	
F- $\overline{\text{RP}}$ Pulse Low Time (If F- $\overline{\text{RP}}$ is tied to $V_{CC}$ , this specification is not applicable.)	$t_{\text{PLPH}}$	100		ns	
F- $\overline{\text{RP}}$ Low to Reset during Block Erase or Write	$t_{\text{PLRZ}}$		23.6	$\mu\text{s}$	*1, 2
F- $V_{CC}$ 2.7V to F- $\overline{\text{RP}}$ High	$t_{\text{VPH}}$	100		ns	*3

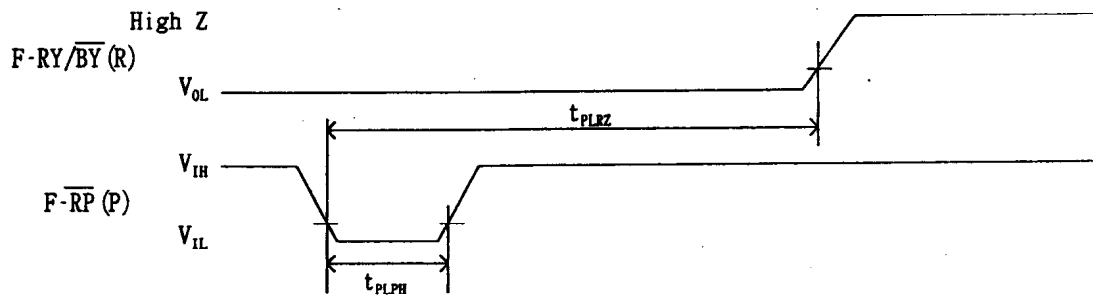
Notes)\*1. If F- $\overline{\text{RP}}$  is asserted while a block erase or word/byte write operation is not executing, the reset will complete with 100ns.

\*2. A reset time,  $t_{\text{PROV}}$ , is required from the later of F-RY/ $\overline{\text{BY}}$  going High Z or F- $\overline{\text{RP}}$  going high until outputs are valid.

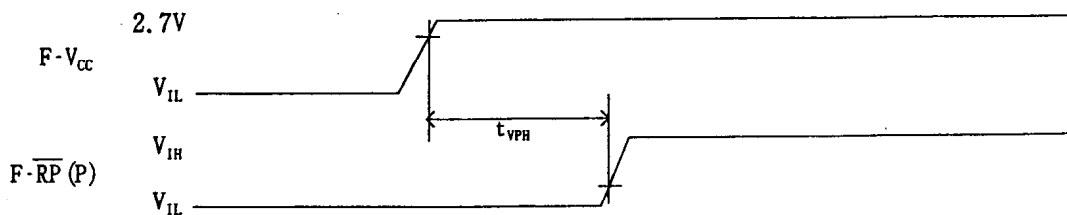
\*3. When the device power-up, holding F- $\overline{\text{RP}}$  low minimum 100ns is required after  $V_{CC}$  has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation

(A) Reset During Read Array Mode



(B) Reset During Block Erase or Word/Byte Write

(C) F- $\overline{\text{RP}}$  Rising Timing

## 13. SRAM AC Electrical Characteristics

## SRAM AC Test Conditions

Input pulse level	0.4 V to 2.2 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.5 V
Output load	1TTL+C <sub>L</sub> (30pF) (*1)

Note) \*1. Including scope and jig capacitance.

## Read Cycle

(T<sub>a</sub> = -25 °C to +85 °C , V<sub>CC</sub> = 2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t <sub>RC</sub>	85		ns	
Address access time	t <sub>AA</sub>		85	ns	
Chip enable access time (S-CE <sub>1</sub> )	t <sub>ACE1</sub>		85	ns	
(S-CE <sub>2</sub> )	t <sub>ACE2</sub>		85	ns	
Output enable to output valid	t <sub>OE</sub>		40	ns	
Output hold from address change	t <sub>OH</sub>	10		ns	
S-CE <sub>1</sub> , S-CE <sub>2</sub> Low (S-CE <sub>1</sub> )	t <sub>LZ1</sub>	10		ns	*2
to output active (S-CE <sub>2</sub> )	t <sub>LZ2</sub>	10		ns	*2
S-OE Low to output active	t <sub>OLZ</sub>	5		ns	*2
S-CE <sub>1</sub> , S-CE <sub>2</sub> High to (S-CE <sub>1</sub> )	t <sub>HZ1</sub>	0	25	ns	*2
output in High impedance (S-CE <sub>2</sub> )	t <sub>HZ2</sub>	0	25	ns	*2
S-OE High to output in High impedance	t <sub>OHZ</sub>	0	25	ns	*2

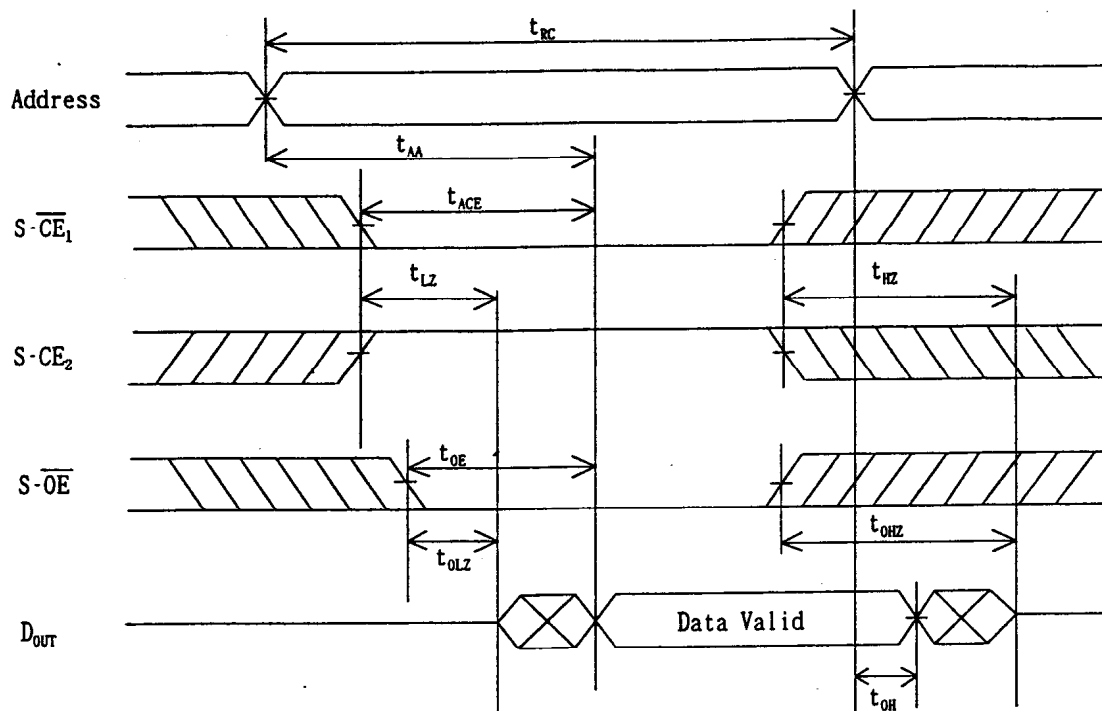
## Write Cycle

(T<sub>a</sub> = -25 °C to +85 °C , V<sub>CC</sub> = 2.7 V to 3.6 V)

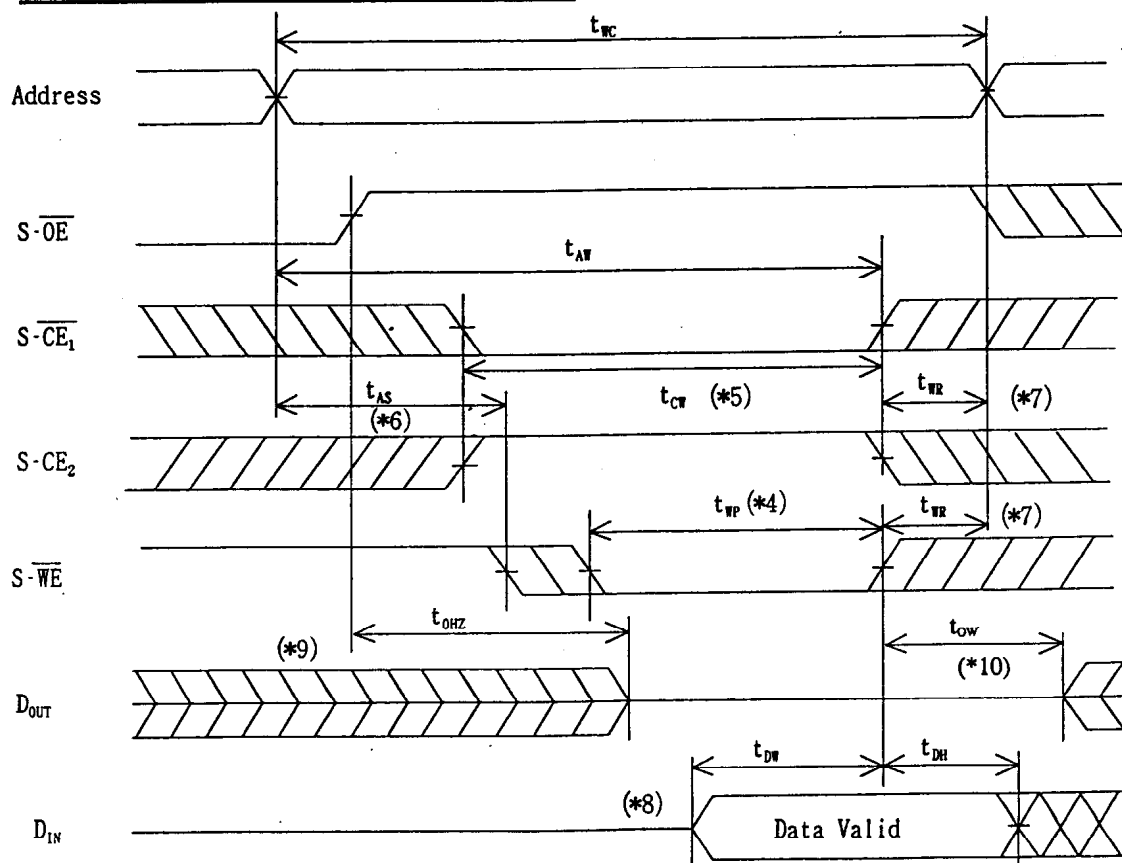
Parameter	Sym.	Min.	Max.	Unit	
Write cycle time	t <sub>WC</sub>	85		ns	
Chip enable to end of write	t <sub>CEW</sub>	70		ns	
Address valid to end of write	t <sub>AV</sub>	70		ns	
Address setup time	t <sub>AS</sub>	0		ns	
Write pulse width	t <sub>WP</sub>	55		ns	
Write recovery time	t <sub>WR</sub>	0		ns	
Input data setup time	t <sub>DW</sub>	35		ns	
Input data hold time	t <sub>DH</sub>	0		ns	
S-WE High to output active	t <sub>OW</sub>	5		ns	*2
S-WE Low to output in High impedance	t <sub>OZ</sub>	0	25	ns	*2

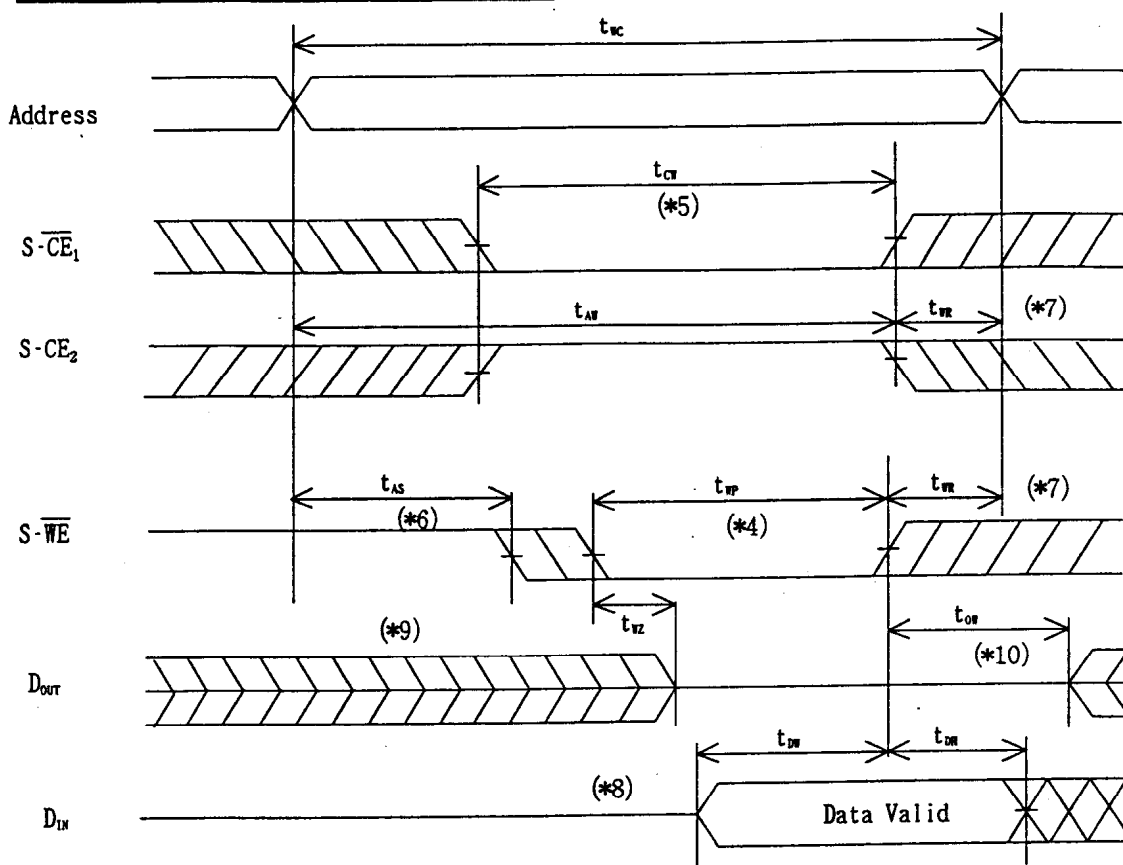
\*2. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

## SRAM AC Characteristics Timing Chart

Read cycle timing chart—(\*3)

\*3  $S-\overline{WE}$  is high for Read cycle.

Write cycle timing chart—( $S-\overline{OE}$  Controlled)

Write cycle timing chart—(S- $\overline{\text{OE}}$  Low fixed)

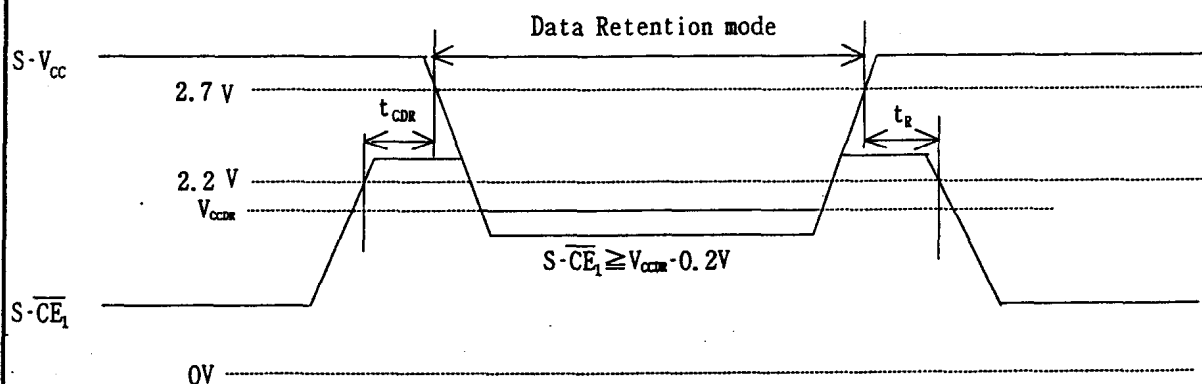
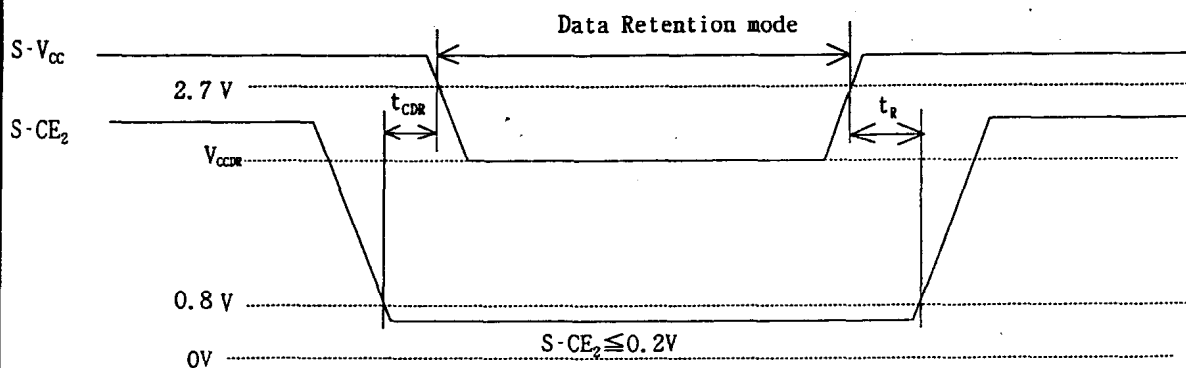
## Notes)

- \*4. A write occurs during the overlap of a low S- $\overline{\text{CE}}_1$ , a high S- $\overline{\text{CE}}_2$  and a low S- $\overline{\text{WE}}$ . A write begins at the latest transition among S- $\overline{\text{CE}}_1$  going low, S- $\overline{\text{CE}}_2$  going high and S- $\overline{\text{WE}}$  going low. A write ends at the earliest transition among S- $\overline{\text{CE}}_1$  going high, S- $\overline{\text{CE}}_2$  going low and S- $\overline{\text{WE}}$  going high.  $t_{wp}$  is measured from the beginning of write to the end of write.
- \*5.  $t_{cw}$  is measured from the later of S- $\overline{\text{CE}}_1$  going low or S- $\overline{\text{CE}}_2$  going high to the end of write.
- \*6.  $t_{as}$  is measured from the address valid to the beginning of write.
- \*7.  $t_{wr}$  is measured from the end of write to the address change.
- \*8. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- \*9. If S- $\overline{\text{CE}}_1$  goes low or S- $\overline{\text{CE}}_2$  goes high simultaneously with S- $\overline{\text{WE}}$  going low or after S- $\overline{\text{WE}}$  going low, the outputs remain in high impedance state.
- \*10. If S- $\overline{\text{CE}}_1$  goes high or S- $\overline{\text{CE}}_2$  goes low simultaneously with S- $\overline{\text{WE}}$  going high or S- $\overline{\text{WE}}$  going high, the outputs remain in high impedance state.

## 14. SRAM Data Retention Characteristics

(T<sub>a</sub> = -25 °C to +85 °C)

Parameter	Sym.	Conditions	Min.	Typ. (*1)	Max.	Unit
Data Retention Supply voltage	V <sub>CCDR</sub>	S-CE <sub>2</sub> ≤ 0.2V or S-CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2V (*2)	2.0		3.6	V
Data Retention Supply current	I <sub>CCDR</sub>	V <sub>CCDR</sub> = 3V S-CE <sub>2</sub> ≤ 0.2V or S-CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2V (*2)		0.2	15	μA
Chip enable setup time	t <sub>CDR</sub>		0			ns
Chip enable hold time	t <sub>R</sub>		5			ms

Notes) \*1. Reference value at T<sub>a</sub> = 25 °C, S-V<sub>CC</sub> = 3.0V.\*2. S-CE<sub>1</sub> ≥ V<sub>CC</sub> - 0.2V, S-CE<sub>2</sub> ≥ V<sub>CC</sub> - 0.2V (S-CE<sub>1</sub> controlled) or S-CE<sub>2</sub> ≤ 0.2V (S-CE<sub>2</sub> controlled)Data Retention timing chart (S-CE<sub>1</sub> Controlled) (\*3)Data Retention timing chart (S-CE<sub>2</sub> Controlled)

Note) \*3. To control the data retention mode at S-CE<sub>1</sub>, fix the input level of S-CE<sub>2</sub> between V<sub>CCDR</sub> and V<sub>CCDR</sub> - 0.2V or 0V or 0.2V and during the data retention mode.

## 15. Notes

This product is a stacked CSP package that a 16M(x8/x16) bit Flash Memory and a 2M(x8) bit SRAM are assembled into.

## Supply Power

Maximum difference (between  $F-V_{CC}$  and  $S-V_{CC}$ ) of the voltage is less than 0.3V.

## Power Supply and Chip Enable of Flash Memory and SRAM

$\overline{S-CE_1}$  should not be LOW and  $S-CE_2$  should not be HIGH when  $\overline{F-CE}$  is LOW simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both  $F-V_{CC}$  and  $S-V_{CC}$  are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

## Power UP Sequence

When turning on Flash memory power supply, keep  $\overline{F-RP}$  LOW. After  $F-V_{CC}$  reaches over 2.7V, keep  $\overline{F-RP}$  LOW for more than 100nsec.

## Device Decoupling

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals ( $\overline{F-CE}$ ,  $\overline{S-CE_1}$ ,  $S-CE_2$ ).



## 16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.

Such noises, when induced onto  $\overline{F\text{-}WE}$  signal or power supply may be interpreted as false commands, causing undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

### 1) Protecting data in specific block

By setting a  $\overline{F\text{-}WP}$  to low, only the boot block can be protected against overwriting.

Parameter and main blocks cannot be locked.

System program, etc., can be locked by storing them in the boot block.

When a high voltage is applied to  $\overline{F\text{-}RP}$ , overwrite operation is enabled for all blocks.

For further information on setting/resetting of block bit, and controlling of  $\overline{F\text{-}WP}$  and  $\overline{F\text{-}RP}$ , refer to the specification. (See 5. Command Definitions P.5)

### 2) Data protection through $V_{pp}$

When the level of  $V_{pp}$  is lower than  $VP_{PLK}$  (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.

For the lockout voltage, refer to the specification. (See Chapter 11. DC Characteristics P.10)

## Data protection during voltage transition

### 1) Data protection thorough $\overline{F\text{-}RP}$

When the  $\overline{F\text{-}RP}$  is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.

For the details of  $\overline{F\text{-}RP}$  control, refer to the specification. (See chapter 12. Flash Memory AC Electrical Characteristics)

## 17. Design Considerations

### 1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a  $0.1\mu\text{F}$  ceramic capacitor connected between its  $V_{\text{CC}}$  and GND and between its  $V_{\text{PP}}$  and GND. Low inductance capacitors should be placed as close as possible to package leads.

### 2. $V_{\text{PP}}$ Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the  $V_{\text{PP}}$  Power Supply trace. Use similar trace widths and layout considerations given to the  $V_{\text{CC}}$  power bus.

### 3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit.  
In case of reprogramming "0" to the data which has been programmed "1".

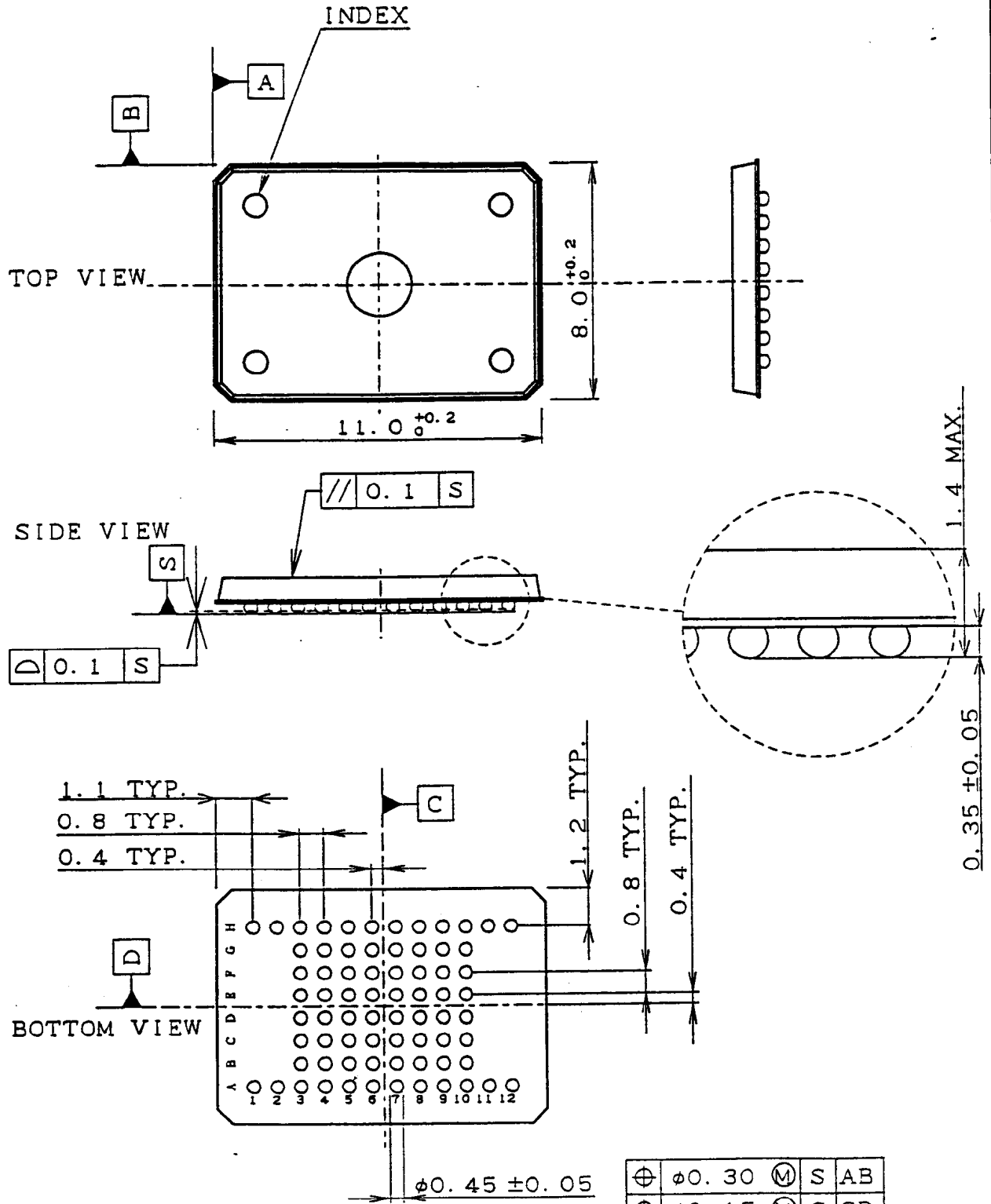
- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "1110111111111110" programming.

### 4. Power Supply

Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid  $V_{\text{PP}}$  (See 11. DC Characteristics) produce spurious results and should not be attempted. Device operations at invalid  $V_{\text{CC}}$  voltage (see 11. DC Characteristics) produce spurious results and should not be attempted.

SHARP



			尺度 SCALE	単位 UNIT	適用機種	16M FLASH MEMORY(X1638)
			5/1	1=1/1mm	APPLICABLE	+2M SRAM (X8)
			端子マトリクス MATRIX	12 X 8	MODEL	
			端子数 COUNTS	72	名称	LCSP072-P-0811
			端子ピッチ PITCH	0.8	NAME	(LFBGA072-P-0811)
改訂日 DATE	改訂記事 REVISE	担当 CHARGE	SHARP CORPORATION			
日付 DATE	1998. 2. 10		C 天津事業本部 TENRI IC GROUP			
設計 DESIGN	製図 DRAW	写図 TRACE	超LSI 開発研究所 VLSI DEVELOPMENT LABORATORIES			
承認 APPROVE			生産技術開発部 PRODUCTION ENGINEERING DEPT.			
SOTA	SOTA		図番			
					DRAWING No.	AA2078