

7496, LS96 Shift Registers

5-Bit Shift Register Product Specification

Logic Products

FEATURES

- 5-bit parallel-to-serial or serial-to-parallel converter
- Asynchronous ones transfer preset entry
- Buffered positive-triggered clock
- Buffered active LOW Clear (Master Reset)

DESCRIPTION

The '96 is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the '96 has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The '96 is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The Serial (S) input is edge-triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7496	25ns	48mA
74LS96	25ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7496N, N74LS96N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

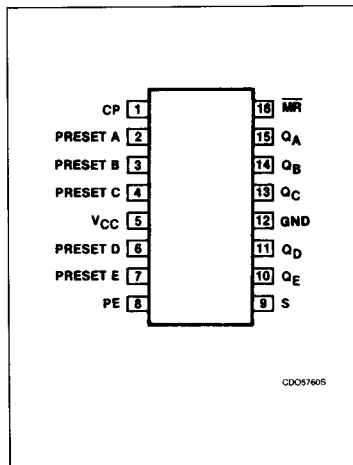
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
Preset enable	Inputs	5uI	5LSuI
All other	Inputs	1uI	1LSuI
Q	Outputs	10uI	10LSuI

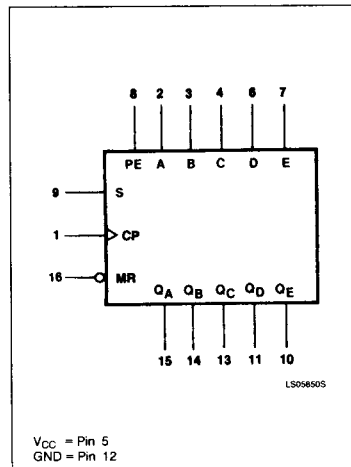
NOTE:

A 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION

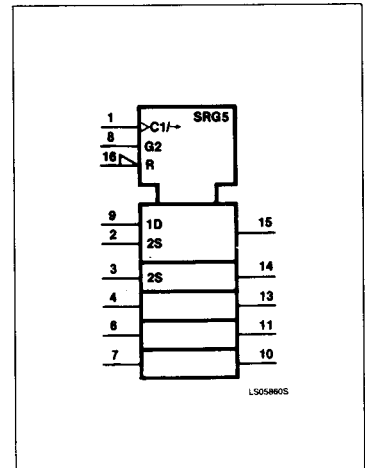


LOGIC SYMBOL



$V_{CC} = \text{Pin } 5$
 $GND = \text{Pin } 12$

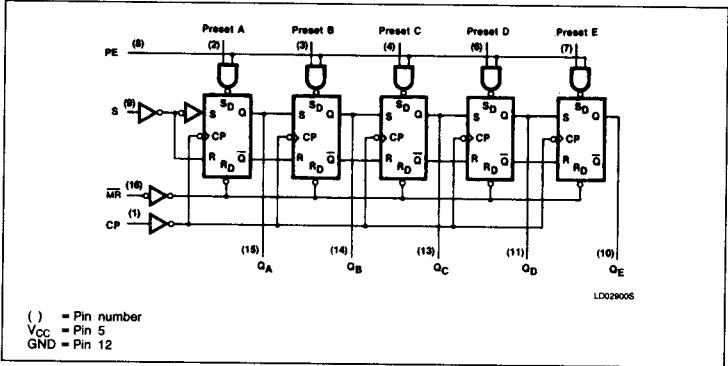
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



Each flip-flop has asynchronous set inputs, allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Preset Enable (PE) input. The PE input is not buffered, and care must be taken not to overload the driving element. When the PE is HIGH, a HIGH on the Preset (A - E) inputs will set the associated flip-flops HIGH. A LOW on the A - E inputs will cause "no change" in the appropriate flip-flops.

The asynchronous active LOW Clear (\overline{MR}) is buffered. When LOW, the \overline{MR} overrides the clock and clears the register if the PE is not active. The Preset inputs override the \overline{MR} , forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

FUNCTION TABLE

INPUTS							OUTPUTS						
Master Reset	Preset Enable	Preset					Clock	Serial	Q _A	Q _B	Q _C	Q _D	Q _E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	L	X	X	X	X	X	L	X	H	H	H	H	H
H	L	X	X	X	X	X	↑	H	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	L	X	X	X	X	X	↑	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}

H = HIGH voltage level, (steady state)
L = LOW voltage level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
QA0, QB0, etc = The level of QA, QB, etc, respectively before the indicated steady-state input conditions were established.
QA0, QB0, etc = The level of QA, QB, etc, respectively before the most recent ↑ transition of the clock.

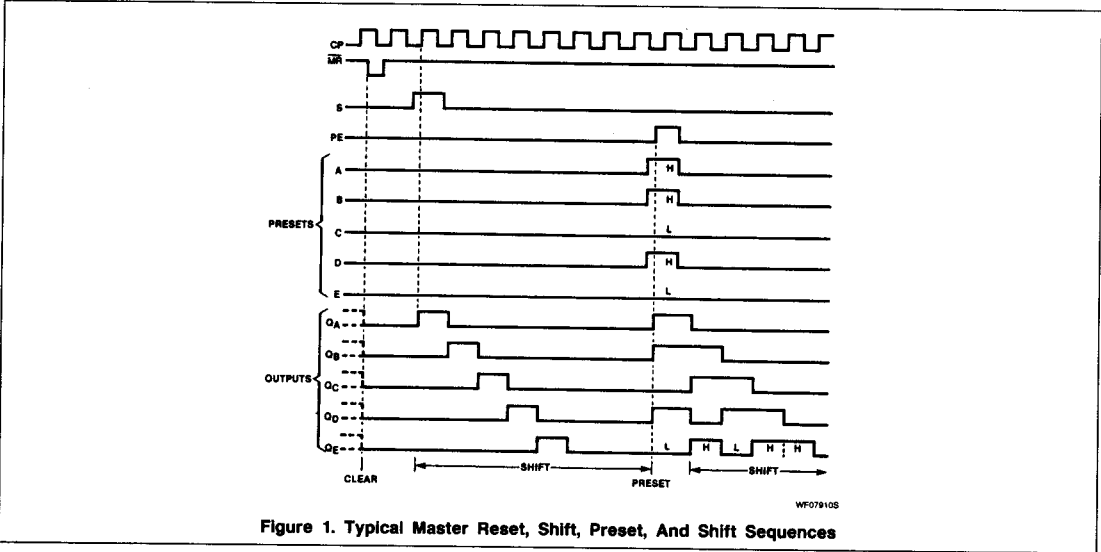


Figure 1. Typical Master Reset, Shift, Preset, And Shift Sequences

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-400			-400	μA
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		7496			74LS96			UNIT
				Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V
			I _{OL} = 4mA (74LS)					0.25	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
			V _I = 7.0V							
			PE inputs						0.5	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX	Other inputs						0.1	mA
			V _I = 2.4V			200				μA
			Other inputs			40				μA
			V _I = 2.7V						100	μA
			Other inputs						20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-8			-2	mA
			Other inputs			-1.6			-0.4	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-18		-57	-20		-100	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			48	79		12	20	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Clear grounded and all other inputs and outputs open.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

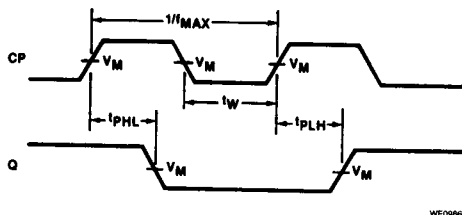
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	10		25		MHz
t_{PLH}	Propagation delay	Waveform 1		40		40	ns
t_{PHL}	Clock to output			40		40	
t_{PLH}	Propagation delay	Waveform 2		35		35	ns
	Preset or preset enable to output						
t_{PHL}	Propagation delay	Waveform 2		55		55	ns
	MR to output						

NOTE:

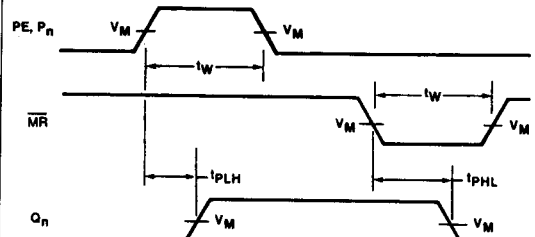
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

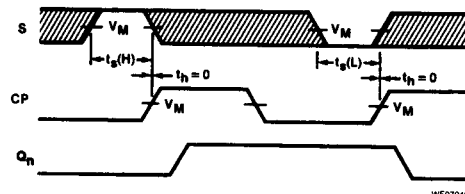
PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{\text{W(L)}}$ Clock pulse width, LOW	Waveform 1	35		20		ns
$t_{\text{W(L)}}$ MR pulse width, LOW	Waveform 2	30		30		ns
$t_{\text{W(H)}}$ Preset or preset enable pulse width, HIGH	Waveform 2	30		30		ns
t_s Set-up time, S to CP	Waveform 3	30		30		ns
t_h Hold time, S to CP	Waveform 3	0		0		ns

AC WAVEFORMS

Waveform 1. Clock To Output
Delays And Clock Pulse Width



Waveform 2. Parallel Load And Parallel Data To Output
Delays And Master Reset To Output Delay



For all waveforms, $V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

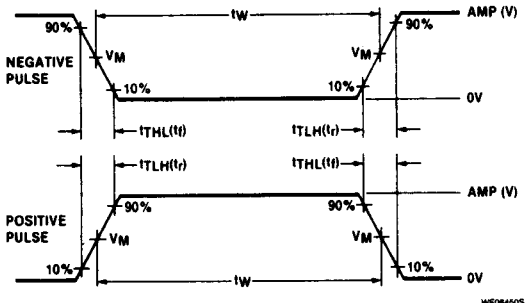
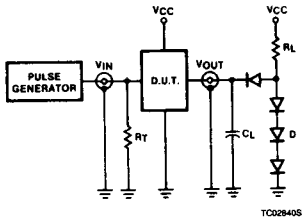
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 3. Data Set-up And Hold Time

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TEST CIRCUITS AND WAVEFORMS



VM = 1.3V for 74LS; VM = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS
RL = Load resistor to VCC; see AC CHARACTERISTICS for value.
CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
RT = Termination resistance should be equal to ZOUT of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
tTLH, tTHL Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	tTLH	tTHL
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns