

64-BIT THERMAL PRINthead DRIVER WITH HEAT HISTORY-BASED PRINthead MANAGEMENT AND 2-BIT PARALLEL INPUT

S-4680A

The S-4680A is a CMOS thermal printhead driver containing two 64-bit shift registers and six latches (3 x 2). Two-bit parallel data can be input to the driver. Since the driver print time can be controlled in accordance with heat history-based data using the gate pins, this driver is suitable for printheads that perform heat history-based management. Due to its large driver output current of 50 mA, the S-4680A is ideal for bar-code printers and high-speed thermal printers.

■ Features

- Low current consumption: 0.8 mA typ. ($f_{CLK}=5$ MHz, SI1 and SI2: Fixed)
- Driver output voltage: 30 V max.
- High speed operation: 8 MHz (cascade connection)
- Driver output current: 50 mA max.
- Two 64-bit shift registers and six latches (3 x 2) are built in.
- Driver-off function when supply voltage falls

■ Block Diagram

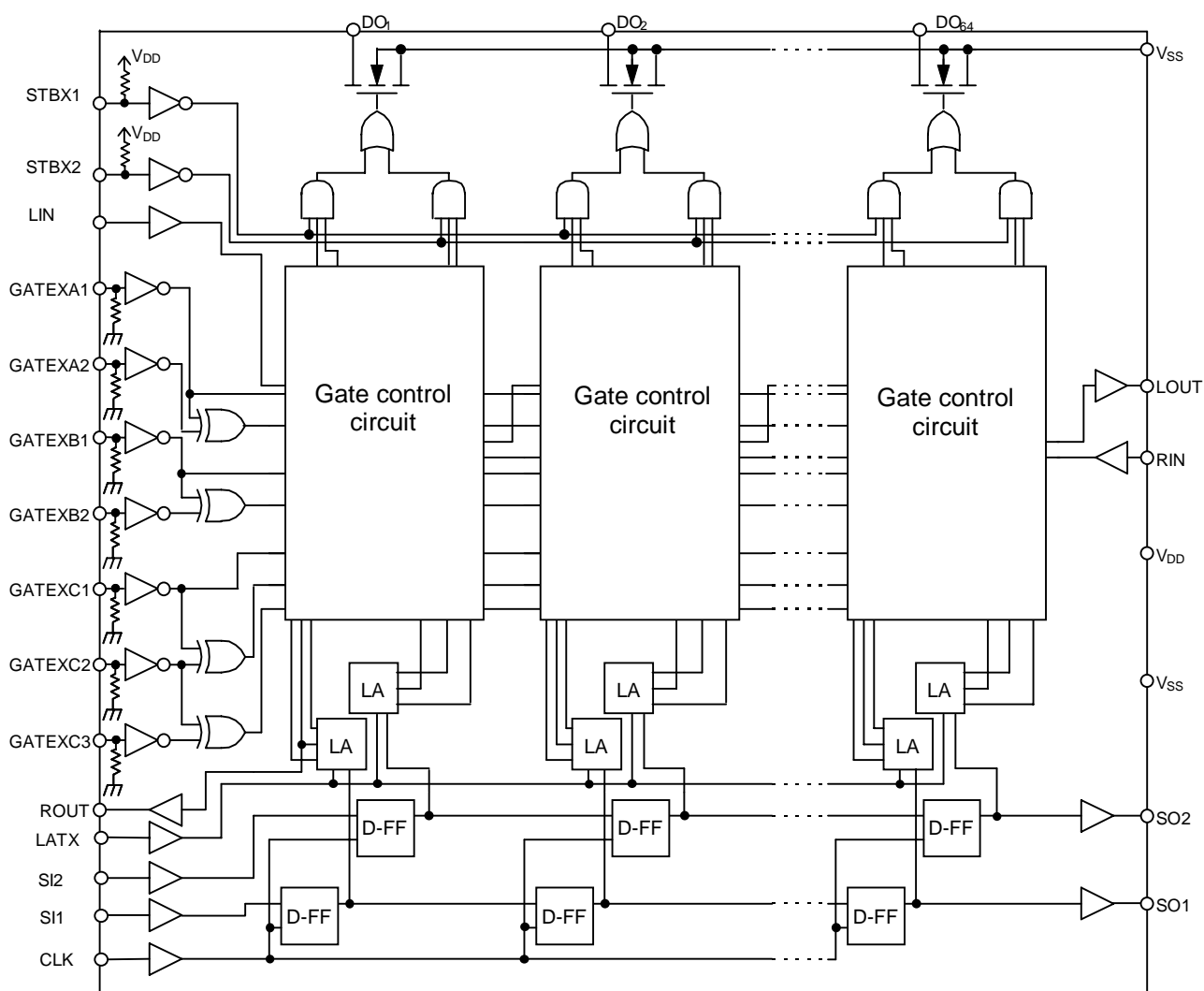


Figure 1 Block Diagram

■ Operation

(1) Basic operation

The shift registers read the data input to the SI1 and SI2 pins at the rising edge of the CLOCK input.

The latch operates depending on the level of the LATX pin. It reads the data of the shift register when the LATX pin is low and it holds the data of the shift register when it is high. A total of six data items (current, preceding and previous,) of SI1 and SI2 is held.

The driver output time can be controlled by combining current, preceding, previous, adjacent right and left preceding data items input from SI1 with gate pulses input from GATEXA1, GATEXA2, GATEXB1, and GATEXB2. The driver output time can be controlled by combining the current, preceding, previous, SI1 adjacent right and left preceding and SI1 previous data items input from SI2 with gate pulses input from GATEXC1, GATEXC2, and GATEXC3.

The latch data is output to the driver when the STBX pin is low. The STBX1 pin controls the driver output of the data input from SI1. The STBX2 pin controls the driver output of the data input from SI2. When the supply voltage changes from 0 to 5 V or 5 V to 0, the driver output transistor goes off.

(2) Generation of heat history-based printhead management print pulse

SI1 heat history -based printhead management operation:

The pulses input from STBX1 are controlled in accordance with the preceding data item, adjacent left preceding data item, adjacent right preceding data item, and previous data item, then they are changed to the respective print pulses. The print pulses determine the time to turn the output transistor on, and the on time can control print energy. When driver DOn is printed, driver DOn-1 which is one bit earlier is the adjacent left, and driver DOn+1 which is one bit later is the adjacent right, the data items preceding each of them are the adjacent left preceding data item and adjacent right preceding data item.

The heat history-based print pulse is generated as follows.

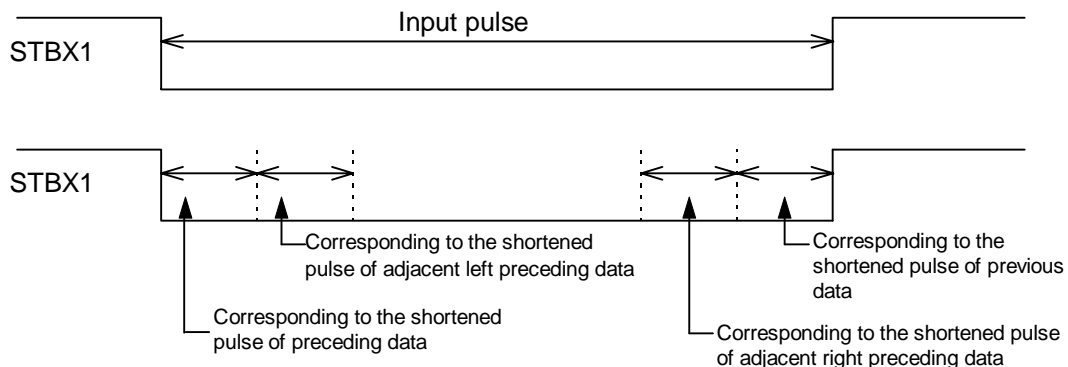


Figure 2 Heat History-Based Printhead Management Operation

If there is preceding data when a pulse is input from STBX1 as shown in Figure 2, the print pulse is reduced by the shortened pulse of the preceding data, allowing for printing with less energy. Similarly, if there is an adjacent right preceding data item, an adjacent left preceding data item or a previous data item, the input pulse is reduced, allowing for printing with less energy.

A print example is given below.

- I. Heat history-based printhead management print pulse when there is preceding data:

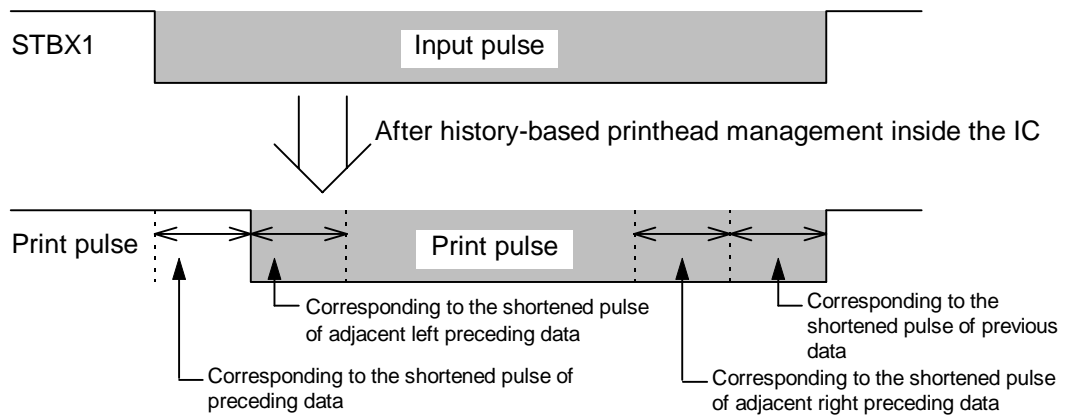


Figure 3 Print Pulse Heat History Management

	Print bit (SI1)	
	Adjacent left	Adjacent right
Previous data		○
Preceding data	○	●
Current data		●

* ● : Data is present
○ : No data

SI2 heat history-based printhead management operation:

The pulses input from STBX2 are controlled in accordance with the preceding data item, previous data item, preceding SI1 data item, and adjacent right/left preceding SI1 data items, and they are changed to the respective print pulses. The print pulses determine the time to turn the output transistor on, and the on time can control print energy. When driver DOn is printed, driver DOn-1 which is one bit earlier is the adjacent left, and driver DOn+1 which is one bit later is the adjacent right, the data items preceding each of them are the adjacent left preceding data item and adjacent right preceding data item.

A heat history-based printhead management print pulse is generated as follows.

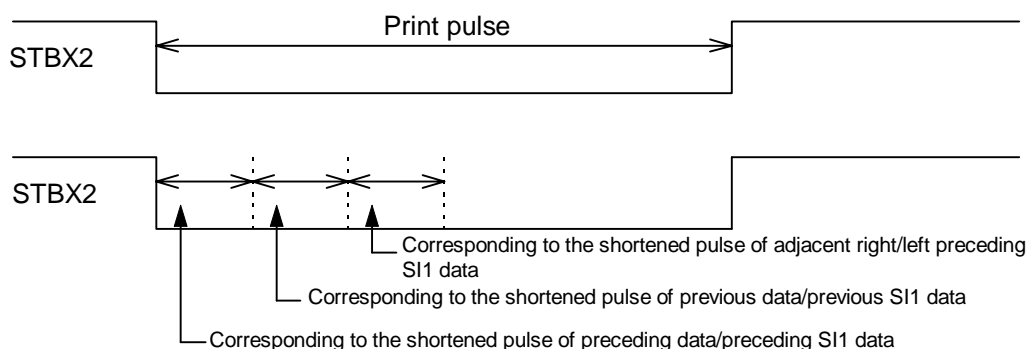


Figure 4 Generation of Heat History-Based Printhead Management Pulse

If there is preceding data when a pulse is input from STBX2 as shown in Figure 4, the print pulse is reduced by the shortened pulse of the preceding data, allowing for printing with less print energy. Similarly, if there is a previous data item, preceding SI1 data item, previous SI1 data, and adjacent right/left preceding SI1 data item, the input pulse is reduced, allowing for printing with less print energy.

A print example is given below.

- I. Heat history-based printhead management print pulse when there is a preceding data item:

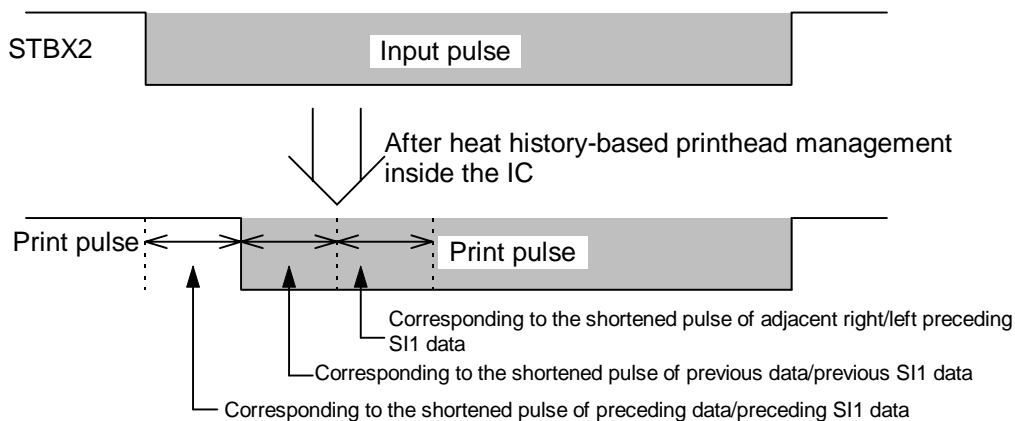


Figure 5 Heat History-Based Printhead Management Print Pulse

	Print bit (SI2)	Print bit (SI1)		
		Adjacent left		Adjacent right
Previous data	○		○	
Preceding data	●	○	○	○
Current data	●		○	

* ● : Data is present
 ○ : No data

- II. Heat history-based printhead management print pulse when there are a preceding data item, a preceding S11 data, and an adjacent left preceding S11 data item:

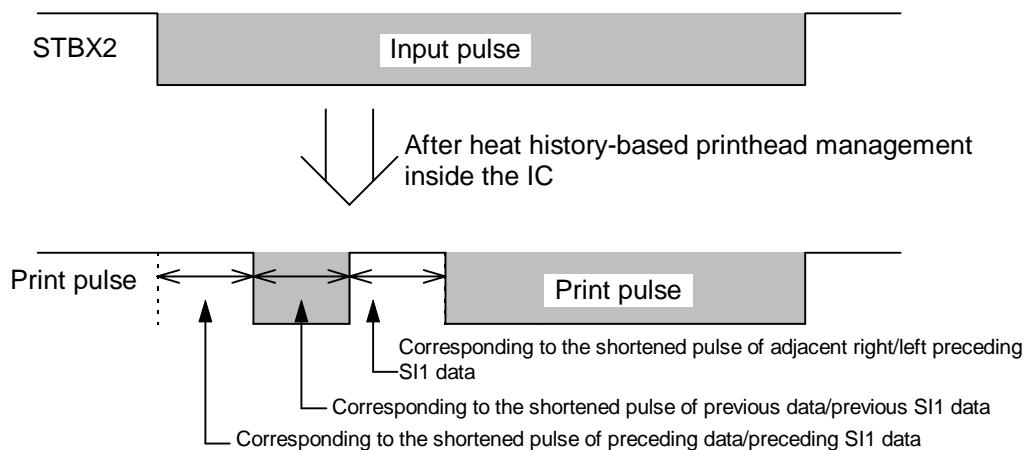


Figure 6 Heat History-Based Printhead Management Print Pulse

	Print bit (SI2)	Print bit (SI1)		
		Adjacent left		Adjacent right
Previous data	○		○	
Preceding data	●	●	●	○
Current data	●		○	

* ● : Data is present
 ○ : No data

SI1/SI2 Heat History-Based Printhead Management Print Pulse

The SI1 print pulses are controlled by input pulse at STBX1 and the following signals a, b, c, and d.

- a: Corresponding to the shortened pulse of preceding data:
Pulse width input from GATEXA1
- b: Corresponding to the shortened pulse of adjacent left preceding data:
Difference between the pulse width input from GATEXA2 and pulse width input from GATEXA1
- c: Corresponding to the shortened pulse of previous data:
Pulse width input from GATEXB1
- d: Corresponding to the shortened pulse of adjacent right preceding data:
Difference between the pulse width input from GATEXB2 and pulse width input from GATEXB1

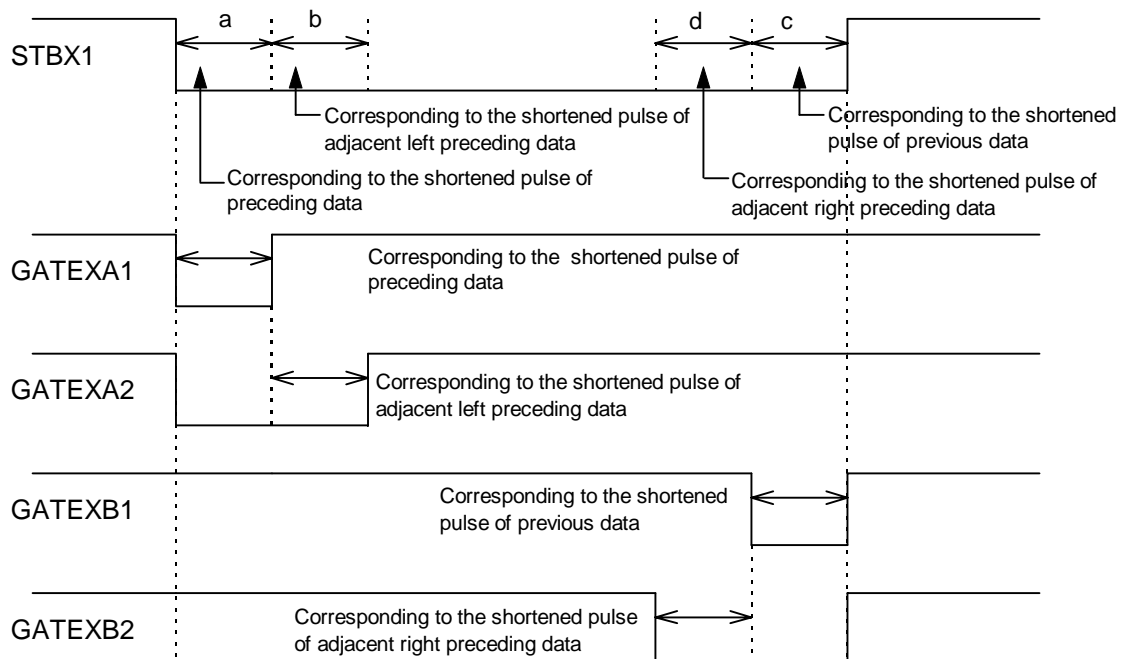


Figure 7 SI1 Heat History-Based Printhead Management Print Pulse

The SI2 print pulses are controlled by input pulse at STBX2 and the following signals e, f and g.

- e: Corresponding to the shortened pulse of preceding data/preceding SI1 data:
Pulse width input from GATEXC1
- f: Corresponding to the shortened pulse of previous data/previous SI1 data:
Difference between the pulse width input from GATEXC2 and pulse width input from GATEXC1
- g: Corresponding to the shortened pulse of adjacent left/right preceding SI1 data:
Difference between the pulse width input from GATEXC3 and pulse width input from GATEXC2

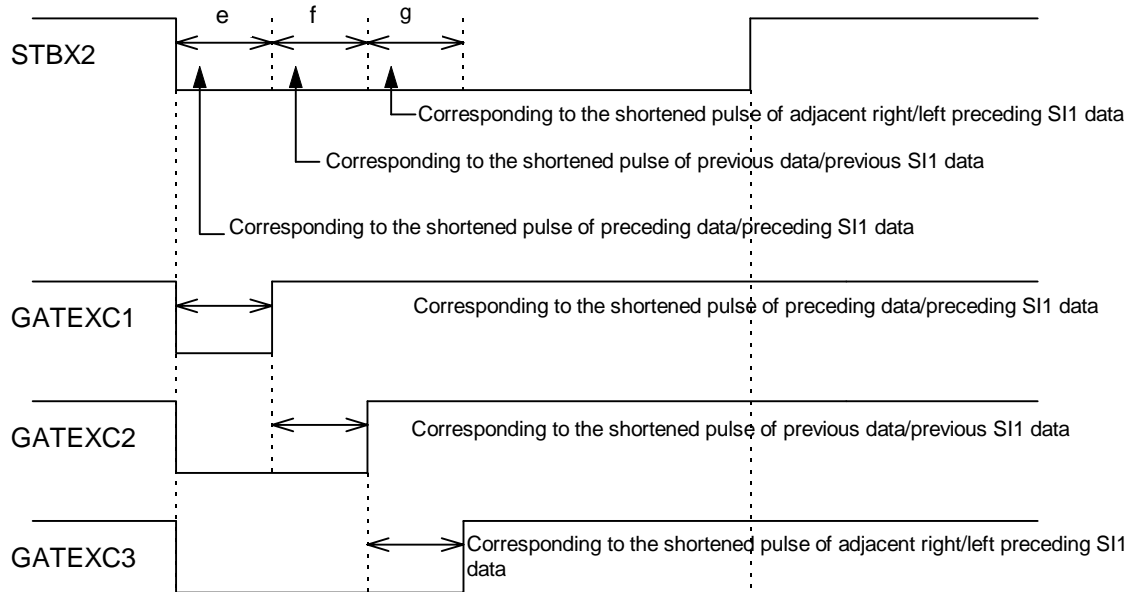


Figure 8 SI2 Heat History-Based Printhead Management Print Pulse

■ **Pin Description** (Refer to the dimensions for the pad assignment)

Table 1 Pin Description

Pin name	Description
DO ₁ to DO ₆₄ (DO _n)	Driver output pins (Nch open-drain)
V _{DD}	Positive power supply for logic (+5V)
V _{SS}	GND pin (0V)
CLK	Clock input pin for 64-bit shift registers (x2)
SI1	Serial data input pin 1 for 64-bit shift registers
SI2	Serial data input pin 2 for 64-bit shift registers
SO1	Serial data output pin 1 for 64-bit shift registers
SO2	Serial data output pin 2 for 64-bit shift registers
GATEXA1	SI1 shortened print pulse control pin when there is SI1 preceding data
GATEXA2	SI1 shortened print pulse control pin when there is SI1 adjacent left preceding data
GATEXB1	SI1 shortened print pulse control pin when there is SI1 previous data
GATEXB2	SI1 shortened print pulse control pin when there is SI1 adjacent right preceding data
GATEXC1	SI2 shortened print pulse control pin when there is SI2 or SI1 preceding data
GATEXC2	SI2 shortened print pulse control pin when there is SI2 or SI1 previous data
GATEXC3	SI2 shortened print pulse control pin when there is SI1 adjacent right/left preceding data
LATX	Data latch signal input pin LATX="L": Reads the current data of the shift register. LATX="H": Holds the current data, preceding data and previous data.
RIN	SI1 adjacent right preceding data (preceding data at bit 1 of the post-chip) input pin
LIN	SI1 adjacent left preceding data (preceding data at bit 64 of the pre-chip) input pin
ROUT	SI1 adjacent right preceding data (preceding data at bit 1 of the respective chip) output pin
LOUT	SI1 adjacent left preceding data (preceding data at bit 64 of the respective chip) output pin
STBX1	Driver strobe input pin. The latch data input from SI1 is output to the driver when this pin is low.
STBX2	Driver strobe input pin. The latch data input from SI1 is output to the driver when this pin is low.

■ Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{SS} to V_{DD}	-0.4 to +7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	50	mA
Input voltage	V_{IN}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Output voltage	V_{OUT}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Max. junction temperature	T_{jmax}	125	°C
Operating temperature range	T_{opr}	-10 to +80	°C
Storage temperature range	T_{stg}	-40 to +125	°C

■ DC Electrical Characteristics

Table 3 DC Electrical Characteristics

($V_{DD}=5.0\text{ V}\pm 10\%$, $T_a=-10^\circ\text{C}$ to 80°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High level input voltage	V_{IH}	*1	$0.7\times V_{DD}$	—	V_{DD}	V
Low level input voltage	V_{IL}		V_{SS}	—	$0.3\times V_{DD}$	V
High level input current	I_{IH}	$V_{DD}=5.0\text{ V}$ $V_{IH}=5.0\text{ V}$ $T_a=25^\circ\text{C}$ GATEXA1,GATEXA2, GATEXB1,GATEXB2, GATEXC1,GATEXC2,GATEXC3	—	—	55	μA
		Other input pins	—	—	0.5	μA
Low level input current	I_{IL}	$V_{DD}=5.0\text{ V}$ $V_{IL}=0\text{ V}$ $T_a=25^\circ\text{C}$ STBX1,STBX2	-55	—	—	μA
		Other input pins	-0.5	—	—	μA
High level output voltage	V_{OH}	SO pin, no load	4.45	—	—	V
Low level output voltage	V_{OL}	SO pin, no load	—	—	0.05	V
High level output current	I_{OH}	SO pin, $V_{OH}=V_{DD}-0.4\text{ V}$	—	—	-0.5	mA
Low level output current	I_{OL}	SO pin, $V_{OL}=0.4\text{ V}$	0.5	—	—	mA
High level driver output voltage	V_{DOH}	Heat generator resistance: 500 Ω min.	—	24	30	V
Low level driver output voltage	V_{DOL}	$I_{DOL}=30\text{ mA}$	—	0.7	1.5	V
Driver leakage current	I_{LEAK}	$V_{DOH}=30\text{ V}$, Per bit of driver output	—	—	1.0	μA
		$V_{DOH}=30\text{ V}$, Per 64 bits of driver output	—	—	10	μA
Current consumption	I_{DD}	$T_a=25^\circ\text{C}$ $f_{CLK}=5\text{ MHz}$, SI: Fixed, LATX: Fixed	—	0.8	2.4	mA
		$f_{CLK}=5\text{ MHz}$, SI=1/2 f_{CLK} , LATX: Fixed	—	3.0	9.0	mA
Supply voltage drop detection circuit	V_{DET}		0.8	—	4.0	V

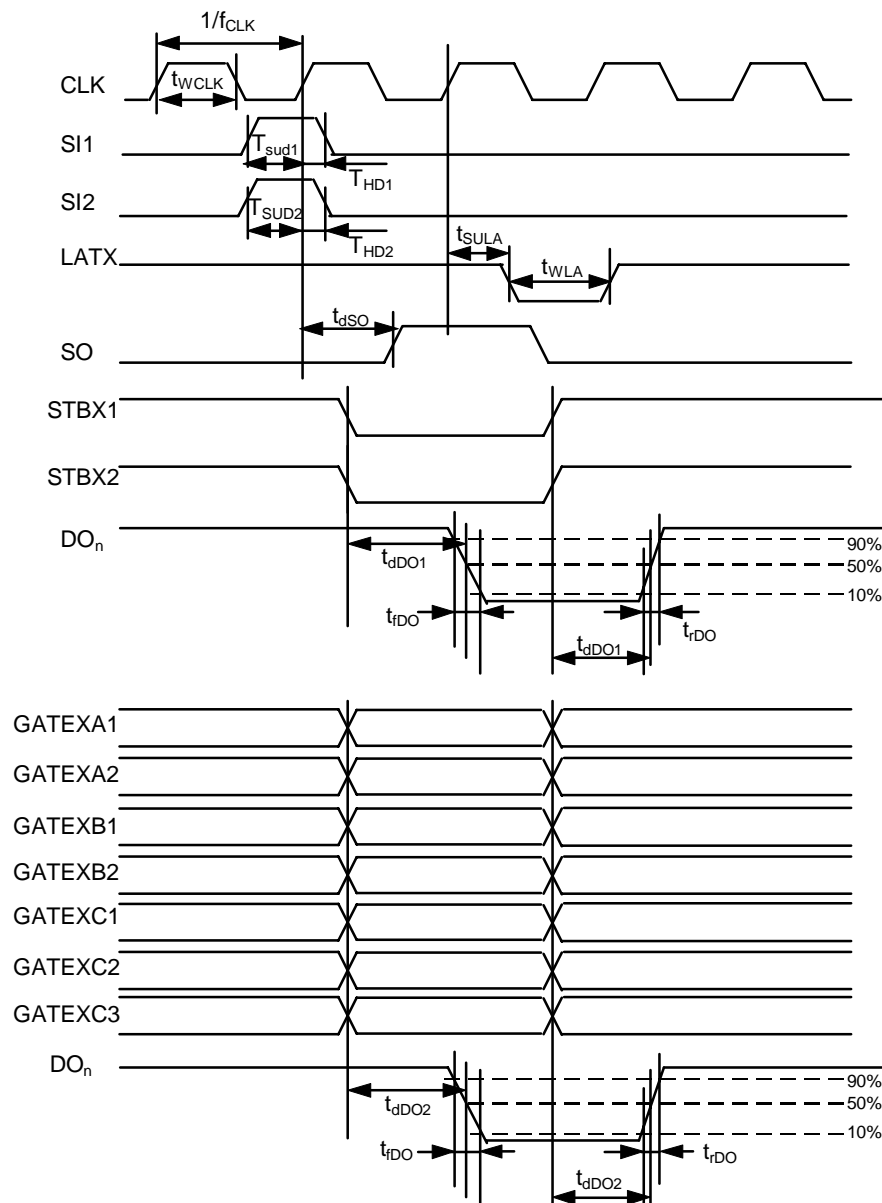
*1 CLK: $f_{CLK}=f_{max}$ duty 50%
 $T_{SUD}=T_{HD}=100\text{ nsec}$
 SI1,SI2: 1/2 f_{max}
 LATX: $T_{WLA}=100\text{ nsec}$
 Other: DC level

■ AC Electric Characteristics

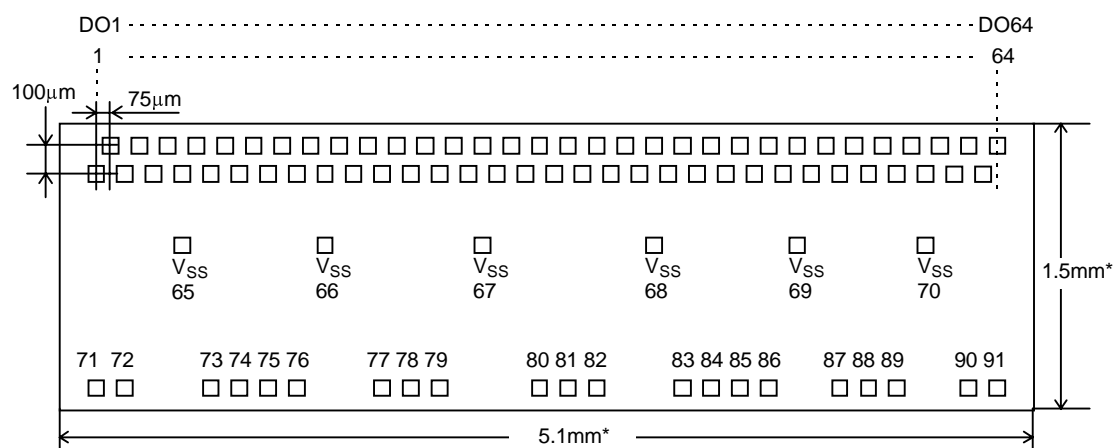
Table 4 AC Electrical Characteristics

($V_{DD}=5.0\text{ V}\pm 10\%$, $T_a=-10^\circ\text{C}$ to 80°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}	$V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	60	—	—	ns
Data setup time	t_{SUD}		35	—	—	ns
Data hold time	t_{HD}		35	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	$C_L=3\text{ pF}$	—	—	80	ns
STBX-DOn propagation delay time	t_{dDO1}	$R_L=1.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	—	10.5	μs
GATEX-DOn propagation delay time	t_{dDO2}	$R_L=1.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	—	10.5	μs
DOn rise time	t_{rDO}	$R_L=1.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	1.0	6.0	μs
DOn fall time	t_{fDO}	$R_L=1.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	1.0	10.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	8.0	MHz


Figure 9 Timing Chart

■ Pad Dimensions



Pad size: 80 μm \times 80 μm (passivation opening)
 Pad pitch: 75 μm (driver output pad)
 Die thickness: 350 \pm 30 μm

* Before dicing

Figure 10 Dimensions

■ Quality Standard

Table 6 Reliability Test Specification

No.	Test item	Test conditions	Test time	LTFR
1	High temperature/high humidity bias	Ta=85°C, RH=85%, Vabs.max ^{*1} \times 0.9	1000 H	10%
2	High humidity bias	Ta=125°C, Vabs.max ^{*1} \times 0.9	1000 H	10%
3	High temperature operation	Ta=125°C, Vopr.max ^{*2}	1000 H	10%
4	Electrostatic voltage	C=200 pF, V=200 V, V _{SS} (or GND), V _{DD} (or V _{CC}) positive or negative reference	Once	—
5	Latchup	V=±100 V, C=200 pF, V=Vopr.max ^{*2}	Once	—

^{*1} Vabs.max : Maximum absolute rating

^{*2} Vopr.max : Maximum operating voltage

Note: The test samples are encapsulated in a standard ceramic package (samples must be resin coated to perform a humidity resistance test).