
BATTERY PROTECTION IC (FOR A 3-SERIAL-CELL PACK)
S-8233C SERIES

The 8233C is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy voltage detection circuits and delay circuits. The 8233C output signals according to battery voltage.
It is suitable for a 3-serial-cell lithium-ion battery pack.

■ Features
(1) Internal high-accuracy voltage detection circuit

- Over charge detection voltage 3.80 ± 0.05 V to 4.40 ± 0.05 V
5 mV - step
- Over charge release voltage 3.45 ± 0.10 V to 4.40 ± 0.10 V
5 mV - step

(The over charge release voltage can be selected within the range where a difference from over charge detection voltage is 0 to 0.35 V at 50 mV - Step)

- Over discharge detection voltage 2.00 ± 0.08 V to 2.80 ± 0.08 V
50 mV - step
- Over discharge release voltage 2.00 ± 0.10 V to 4.00 ± 0.10 V
50 mV - step

(The over discharge release voltage can be selected within the range where a difference from over discharge detection voltage is 0 to 1.2V at 50 mV - Step)

- Over current detection voltage 1 0.15 V ± 10% to 0.50 V ± 10%
50 mV - step

(2) High input-voltage device (absolute maximum rating: 26 V)
(3) Indicates Li-ion battery state.
(4) Wide operating voltage range: 2 V to 24 V
(5) The delay time for every detection can be set via an external capacitor.
(6) Three over current detection levels (protection for short-circuiting)
(7) Internal charge/discharge prohibition circuit via the control terminal
(8) The function for charging batteries from 0 V is available.
(9) Low current consumption

- Operation 50 µA max (+25 °C)
- Power-down 0.1 µA max (+25 °C)

(10) 16-pin TSSOP package
■ Applications

Lithium-ion rechargeable battery packs

■ Selection Guide

Table1

Model / Item	Over charge detection voltage	Over charge release voltage	Over discharge detection voltage	Over discharge release voltage	Over current detection voltage ¹	0V battery charging function
S-8233CAFT	4.25±0.05V	4.05±0.10V	2.00±0.08V	2.30±0.10V	0.25V±10%	-

Change in the detection voltage is available in products other than the above listed ones.
Contact the SII Semiconductor Products Sales Department.

■ Block Diagram

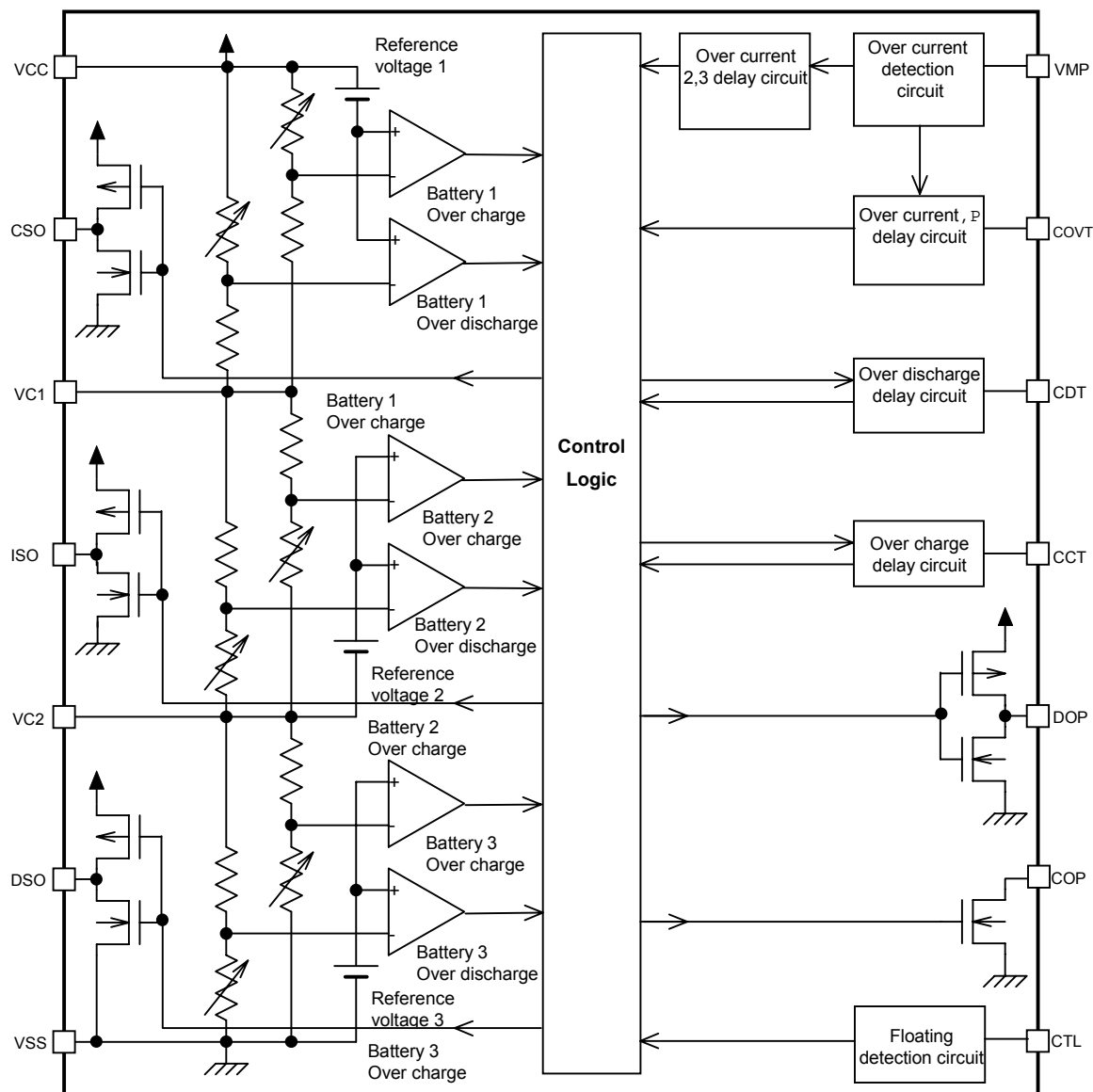


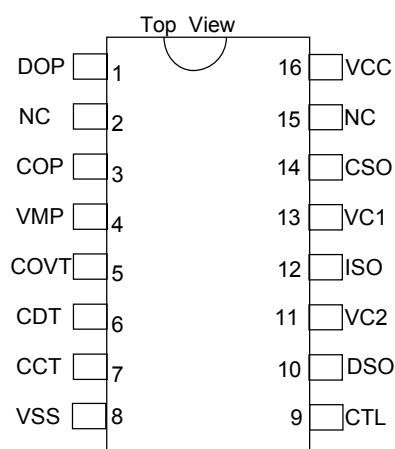
Figure 1

The delay time for over current detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

1. If one of the battery voltages becomes higher than the over charge detection voltage (VCU), the CSO terminal goes high.
2. If one of the battery voltages becomes lower than the over discharge detection voltage (VDD), the ISO terminal goes high.
3. If S-8233C series detect over current, the ISO terminal goes high.

In normal state each terminal output 'Low'.

■ Pin Assignment



TSSOP - 16

Figure 2

■ Pin Description

Table2

No.	Name	Description
1	DOP	Connects FET gate for discharge control (CMOS output)
3	COP	Connects FET gate for charge control (Nch open-drain output)
4	VMP	Detects voltage between VCC to VMP(Over current detection pin)
5	COVT	Connects capacitor for over current detection delay circuit
6	CDT	Connects capacitor for over discharge detection delay circuit
7	CCT	Connects capacitor for over charge detection delay circuit
8	VSS	Negative power input, and connects negative voltage for battery 3
9	CTL	Charge/discharge control signal input
10	DSO	Over discharge condition signal output
11	VC2	Connects battery 2 negative voltage and battery 3 positive voltage
12	ISO	Over current condition signal output
13	VC1	Connects battery 1 negative voltage and battery 2 positive voltage
14	CSO	Over voltage condition signal output
16	VCC	Positive power input and connects battery 1 positive voltage
2,15	N.C.	Non connect

■ Absolute Maximum Ratings

Table3

Ta = 25°C

Item	Sym.	Applied Pins	Rating	Unit
Input voltage between VCC and VSS	VDS		VSS-0.3 to VSS+26	V
Input terminal voltage	VIN	VC1,VC2,CTL,CCT,CDT,COVT	VSS-0.3 to VCC+0.3	V
VMP Input terminal voltage	VVMP	VMP	VSS-0.3 to VSS+26	V
CSO,ISO,DSO output terminal voltage	VOUT	CSO,ISO,DSO	VSS-0.3 to VCC+0.3	V
DOP output terminal voltage	VDOP	DOP	VSS-0.3 to VCC+0.3	V
COP output terminal voltage	VCOP	COP	VSS-0.3 to VMP+0.3	V
Power dissipation	PD	TSSOP-16PKG	300	mW
Operating temperature range	Topr		-20 to +70	°C
Storage temperature range	Tstg		-40 to +125	°C

■ Electrical Characteristics

Table 4

Ta = 25°C

Item	Symbol	condition	Test circuit	Notice	Min.	Typ.	Max.	Unit
Detection voltage								
Over charge detection voltage1	VCU1	1	1	4.10 to 4.35 Adjustment	VCU1-0.05	VCU1	VCU1+0.05	V
Over charge release voltage1	VCD1	1	1	3.85 to 4.35 Adjustment	VCD1-0.10	VCD1	VCD1+0.10	V
Over discharge detection voltage1	VDD1	1	1	2.00 to 2.70 Adjustment	VDD1-0.08	VDD1	VDD1+0.08	V
Over discharge release voltage1	VDU1	1	1	2.00 to 3.70 Adjustment	VDU1-0.10	VDU1	VDU1+0.10	V
Over charge detection voltage2	VCU2	2	1	4.10 to 4.35 Adjustment	VCU2-0.05	VCU2	VCU2+0.05	V
Over charge release voltage2	VCD2	2	1	3.85 to 4.35 Adjustment	VCD2-0.10	VCD2	VCD2+0.10	V
Over discharge detection voltage2	VDD2	2	1	2.00 to 2.70 Adjustment	VDD2-0.08	VDD2	VDD2+0.08	V
Over discharge release voltage2	VDU2	2	1	2.00 to 3.70 Adjustment	VDU2-0.10	VDU2	VDU2+0.10	V
Over charge detection voltage3	VCU3	3	1	4.10 to 4.35 Adjustment	VCU3-0.05	VCU3	VCU3+0.05	V
Over charge release voltage3	VDSO	3	1	3.85 to 4.35 Adjustment	VDSO-0.10	VDSO	VDSO+0.10	V
Over discharge detection voltage3	VDD3	3	1	2.00 to 2.70 Adjustment	VDD3-0.08	VDD3	VDD3+0.08	V
Over discharge release voltage3	VDU3	3	1	2.00 to 3.70 Adjustment	VDU3-0.10	VDU3	VDU3+0.10	V
Over current detection voltage1	VIOV1	4	2	(*)0.15 to 0.50V Adjustment	VIOV1×0.9	VIOV1	VIOV1×1.1	V
Over current detection voltage2	VIOV2	4	2	VCC Reference	0.54	0.6	0.66	V
Over current detection voltage3	VIOV3	4	2	VSS Reference	1.0	2.0	3.0	V
Voltage temperature factor 1	TCOE1			(*)Ta=-20 to 70°C	-1.0	0	1.0	mV/°C
Voltage temperature factor 2	TCOE2			(*)Ta=-20 to 70°C	-0.5	0	0.5	mV/°C
Delay time								
Over charge detection delay time1	tCU1	9	6	CCCT=0.47μF	0.5	1.0	1.5	S
Over charge detection delay time2	tCU2	10	6	CCCT=0.47μF	0.5	1.0	1.5	S
Over charge detection delay time3	tCU3	11	6	CCCT=0.47μF	0.5	1.0	1.5	S
Over discharge detection delay time1	tDD1	9	6	CCDT=0.1μF	20	40	60	mS
Over discharge detection delay time2	tDD2	10	6	CCDT=0.1μF	20	40	60	mS
Over discharge detection delay time3	tDD3	11	6	CCDT=0.1μF	20	40	60	mS
Over current detection delay time1	tIOV1	12	7	CCOVT=0.1μF	10	20	30	mS
Over current detection delay time2	tIOV2	12	7		2	4	8	mS
Over current detection delay time3	tIOV3	12	7	FET gate capacitor =200pF	100	300	550	μS
Operating voltage								
Operating voltage between VCC and VSS	VDSOP			(*)3	2.0	-	24	V

Current consumption								
Current consumption (during normal operation)	IOPE	5	3	V1=V2=V3=3.5V	-	20	50	μA
Current consumption for cell 1	ICELL1	5	3	V1=V2=V3=3.5V	-300	0	300	nA
Current consumption for cell 2	ICELL2	5	3	V1=V2=V3=3.5V	-300	0	300	nA
Current consumption for cell 3	ICELL3	5	3	V1=V2=V3=3.5V	-300	0	300	nA
Current consumption at power down	IPDN	5	3	V1=V2=V3=1.5V	-	-	0.1	μA
Internal resistance with 0V battery charging function type.								
Resistance between VCC and VMP	Rvcm	6	3	V1=V2=V3=3.5V	0.20	0.50	0.80	MΩ
Resistance between VSS and VMP	Rvsm	6	3	V1=V2=V3=3.5V	0.20	0.50	0.80	MΩ
Internal resistance without 0V battery charging function type.								
Resistance between VCC and VMP	Rvcm	6	3	V1=V2=V3=3.5V	0.40	0.90	1.40	MΩ
Resistance between VSS and VMP	Rvsm	6	3	V1=V2=V3=3.5V	0.40	0.90	1.40	MΩ
Input voltage								
CTL"H"Input voltage	VCTL(H)				VCC×0.8	-	-	V
CTL"L"Input voltage	VCTL(L)				-	-	VCC×0.2	V
Output voltage								
DOP"H"voltage	VDO(H)	7	4	Iout=10μA	VCC-0.5	-	-	V
DOP"L"voltage	VDO(L)	7	4	Iout=10μA	-	-	VSS+0.1	V
COP"L"voltage	VCO(L)	8	5	Iout=10μA	-	-	VSS+0.1	V
COP OFF LEAK current	ICOL	14	9	V1=V2=V3=4.5V	-	-	100	nA
CSO"H"voltage	VCSO(H)	13	8	Iout=0.1μA	VCC-0.5	-	-	V
CSO"L"voltage	VCSO(L)	13	8	Iout=10μA	-	-	VSS+0.1	V
ISO"H"voltage	VISO(H)	13	8	Iout=0.1μA	VCC-0.5	-	-	V
ISO"L"voltage	VISO(L)	13	8	Iout=10μA	-	-	VSS+0.1	V
DSO"H"voltage	VDSO(H)	13	8	Iout=0.1μA	VCC-0.5	-	-	V
DSO"L"voltage	VDSO(L)	13	8	Iout=10μA	-	-	VSS+0.1	V
0V battery charging function (*5)								
0V charging start voltage	V0CHAR	15	10		-	-	1.4	V

(*1) Voltage temperature factor 1 indicates over charge detection voltage, over charge release voltage, over discharge detection voltage, and over discharge release voltage.

(*2) Voltage temperature factor 2 indicates over current detection voltage.

(*3) The DOP and COP logic must be established for the operating voltage.

(*4) If over current detection voltage 1 is 0.50 V, both over current detection voltages 1 and 2 are 0.54 to 0.55 V, but VIOV2 > VIOV1.

(*5) This spec applies for only 0V battery charging function available type.

■ Measurement Circuits

(1) Measurement 1 Measurement circuit 1

Set V1, V2, and V3 to 3.5 V under normal condition. Increase V1 from 3.5 V gradually. The V1 voltage when COP = 'H' is over charge detection voltage 1 (VCU1). Decrease V1 gradually. The V1 voltage when COP = 'L' is over charge release voltage 1 (VCSO). Further decrease V1. The V1 voltage when DOP = 'H' is over discharge voltage 1 (VDD1). Increase V1 gradually. The V1 voltage when DOP = 'L' is over discharge release voltage 1 (VDU1).

(2) Measurement 2 Measurement circuit 1

Set V1, V2, and V3 to 3.5 V under normal condition. Increase V2 from 3.5 V gradually. The V2 voltage when COP = 'H' is over charge detection voltage 2 (VCU2). Decrease V2 gradually. The V2 voltage when COP = 'L' is over charge release voltage 2 (VCD2). Further decrease V2. The V2 voltage when DOP = 'H' is over discharge voltage 2 (VDD2). Increase V2 gradually. The V2 voltage when DOP = 'L' is over discharge release voltage 2 (VDU2).

(3) Measurement 3 Measurement circuit 1

Set V1, V2, and V3 to 3.5 V under normal condition. Increase V3 from 3.5 V gradually. The V3 voltage when COP = 'H' is over charge detection voltage 3 (VCU3). Decrease V3 gradually. The V3 voltage when COP = 'L' is over charge release voltage 3 (VCD3). Further decrease V3. The V3 voltage when DOP = 'H' is over discharge voltage 3 (VDD3). Increase V3 gradually. The V3 voltage when DOP = 'L' is over discharge release voltage 3 (VDU3).

Note: The voltage change rate is 150 V/sec or less under measuring conditions 1 to 3.

(4) Measurement 4 Measurement circuit 2

Set V1, V2, V3 to 3.5 V and V4 to 0 V under normal condition. Increase V4 from 0 V gradually. The V4 voltage when DOP = 'H' and COP = 'H' is over current detection voltage 1 (VIOV1).

Set V1, V2, and V3 to 3.5 V and V4 to 0 V under normal condition. Fix the COVT terminal at VSS, increase V4 from 0 V gradually. The V4 voltage when DOP = 'H' and COP = 'H' is over current detection voltage 2 (VIOV2).

Set V1, V2, and V3 to 3.5 V and V4 to 0 V under normal condition. Fix the COVT terminal at VSS, increase V4 gradually from 0 V at 400 μ s to 2 ms. The V4 voltage when DOP = 'H' and COP = 'H' is over current detection voltage 3 (VIOV3).

(5) Measurement 5 Measurement circuit 3

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V4 to 0 V under normal condition and measure current consumption. I1 is the normal condition current consumption (IOPE), I2, the cell 2 current consumption (ICELL2), and I3, the cell 3 current consumption (ICELL3).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V4 to 4.5 V under over discharge condition. Current consumption I1 is power-down current consumption (IPDN).

(6) Measurement 6 Measurement circuit 3

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V4 to 10.5 V under normal condition. $V4/I4$ is the internal resistance between VCC and VMP (RVCM).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V4 to 4.1 V under over discharge condition. $(4.5-V4)/I4$ is the internal resistance between VSS and VMP (RVSM).

(7) Measurement 7 Measurement circuit 4

Set S1 to ON, S2 to OFF, V1, V2, and V3 to 3.5 V, and V4 to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when $I_5 = 10 \mu\text{A}$ is DOP'L' voltage (VD0 (L)).

Set S1 to OFF, S2 to ON, V1, V2, V3 to 3.5 V, and V4 to $V_{IOV2} + 0.1 \text{ V}$ under over current condition. Increase V6 from 0 V gradually. The V6 voltage when $I_6 = 10 \mu\text{A}$ is the DOP'H' voltage (VDO (H)).

(8) Measurement 8 Measurement circuit 5

Set V1, V2, V3 to 3.5 V and V4 to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when $I_5 = 10 \mu\text{A}$ is the COP'L' voltage (VC0 (L)).

(9) Measurement 9 Measurement circuit 6

Set V1, V2, V3 to 3.5 V under normal condition. Increase V1 from 3.5 V to 4.5 V immediately (within 10 μs). The time after V1 becomes 4.5 V until COP goes 'H' is the over charge detection delay time 1 (tCU1).

Set V1, V2, V3 to 3.5 V under normal condition. Decrease V1 from 3.5 V to 1.9 V immediately (within 10 μs). The time after V1 becomes 1.9 V until DOP goes 'H' is the over discharge detection delay time 1 (tDD1).

(10) Measurement 10 Measurement circuit 6

Set V1, V2, V3 to 3.5 V under normal condition. Increase V2 from 3.5 V to 4.5 V immediately (within 10 μs). The time after V2 becomes 4.5 V until COP goes 'H' is the over charge detection delay time 2 (tCU2).

Set V1, V2, V3 to 3.5 V under normal condition. Decrease V2 from 3.5 V to 1.9 V immediately (within 10 μs). The time after V2 becomes 1.9 V until DOP goes 'H' is the over discharge detection delay time 2 (tDD2).

(11) Measurement 11 Measurement circuit 6

Set V1, V2, V3 to 3.5 V under normal condition. Increase V3 from 3.5 V to 4.5 V immediately (within 10 μs). The time after V3 becomes 4.5 V until COP goes 'H' is the over charge detection delay time 3 (tCU3).

Set V1, V2, V3 to 3.5 V under normal condition. Decrease V3 from 3.5 V to 1.9 V immediately (within 10 μs). The time after V3 becomes 1.9 V until DOP goes 'H' is the over discharge detection delay time 3 (tDD3).

(12) Measurement 12 Measurement circuit 7

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal condition. Increase V4 from 0 V to 0.55 V immediately (within 10 μs). The time after V4 becomes 0.55 V until DOP goes 'H' is the over current detection delay time 1 (tIOV1).

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal condition. Increase V4 from 0 V to 0.75 V immediately (within 10 μs). The time after V4 becomes 0.75 V until DOP goes 'H' is the over current detection delay time 2 (tIOV2).

Set S1 to ON to inhibit over discharge detection. Set V1, V2, V3 to 4.0 V and increase V4 from 0 V to 6.0 V immediately (within 1 μs) and decrease V1, V2, and V3 to 2.0 V at a time. The time after V4 becomes 6.0 V until DOP goes 'H' is the over current detection delay time 3 (tIOV3).

(13) Measurement 13 Measurement circuit 8

Set S4 to ON, S1, S2, S3, S5, and S6 to OFF, V1, V2, V3 to 3.5 V, and V4, V6, to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when $I_5 = 10 \mu\text{A}$ is the CSO'L' voltage (VCSO(L)).

Set S5 to ON, S1, S2, S3, S4, and S6 to OFF, V1, V2, and V3 to 3.5 V and V4, V6 to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when $I_5 = 10 \mu\text{A}$ is the ISO'L' voltage (VISO(L)).

Set S6 to ON, S1, S2, S3, S4, and S5 to OFF, V1, V2, and V3 to 3.5 V and V4, V6 to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when $I_5 = 10 \mu\text{A}$ is the DSO'L' voltage (VDSO(L)).

Set S1 to ON, S2, S3, S4, S5, and S6 to OFF, V1 to 4.5V, V2, and V3 to 3.5 V, V5, and V6 to 0 V under over voltage condition. Increase V4 from 0 V gradually. The V4 voltage when $I_4 = 10 \mu\text{A}$ is the CSO'H' voltage (VCSO(H)).

Set S2 to ON, S1, S3, S4, S5, and S6 to OFF, V1, V2 and V3 to 3.5 V, V5 to 0 V, V6 to $V_{\text{iov2}}+0.1\text{V}$ under over current condition. Increase V4 from 0 V gradually. The V4 voltage when $I_4 = 10 \mu\text{A}$ is the ISO'H' voltage (VISO(H)).

Set S3 to ON, S1, S2, S4, S5, and S6 to OFF, V1 to 1.9V, V2 and V3 to 3.5 V, V5 and V6 to 0 V under over discharge condition. Increase V4 from 0 V gradually. The V4 voltage when $I_4 = 10 \mu\text{A}$ is the DSO'H' voltage (VDSO(H)).

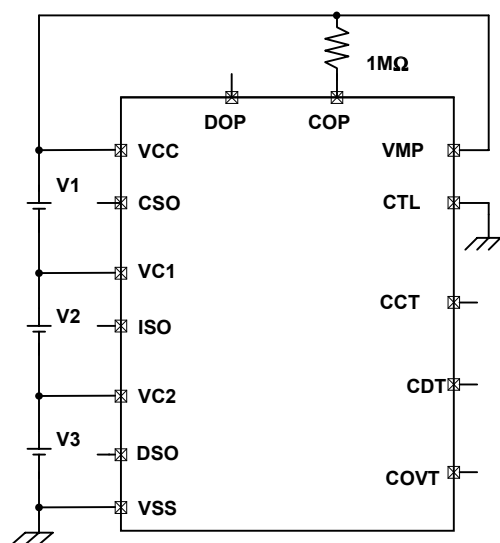
(14) Measurement 14 Measurement circuit 9

Set V1, V2, and V3 to 4.5 V under over charge condition. The current I_1 flowing to COP terminal is COP OFF LEAK current (ICOL).

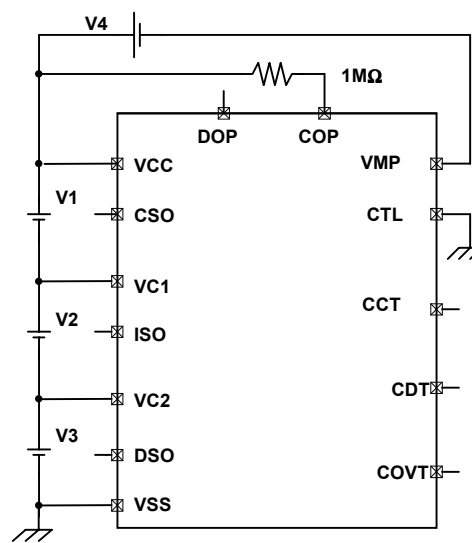
(15) Measurement 15 Measurement circuit 10

Set V1, V2, and V3 to 0 V, and V4 to 2 V, and decrease V4 gradually. The V4 voltage when COP = 'H' ($V_{\text{SS}} + 0.1 \text{ V}$ or higher) is the 0V charge start voltage (V0CHAR).

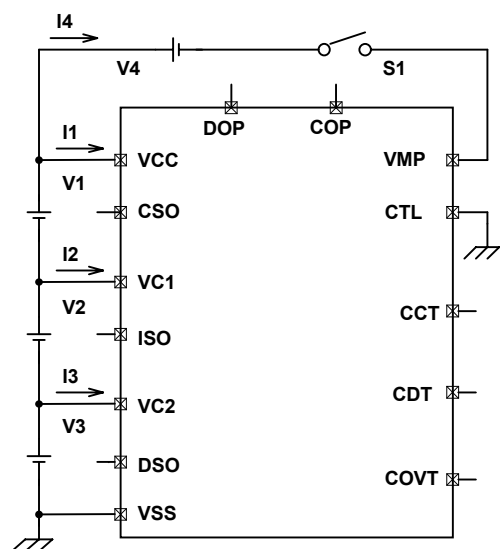
Note: The voltage change rate is 150 V/sec or less under the measuring condition.



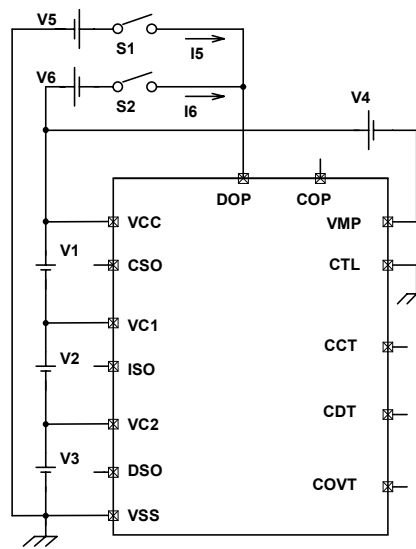
Measurement circuit 1



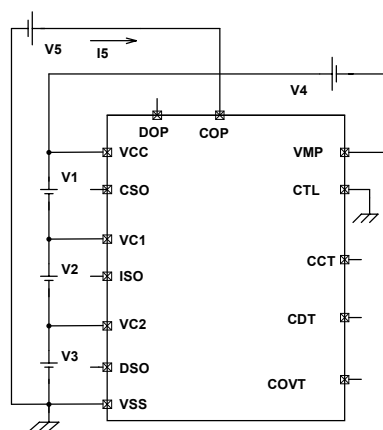
Measurement circuit 2



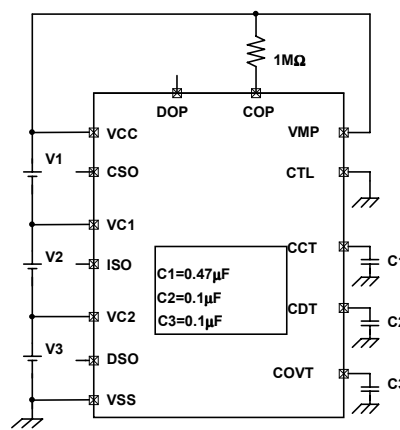
Measurement circuit 3



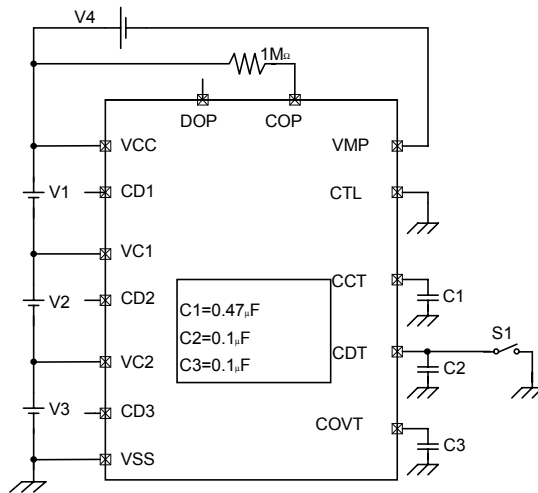
Measurement circuit 4



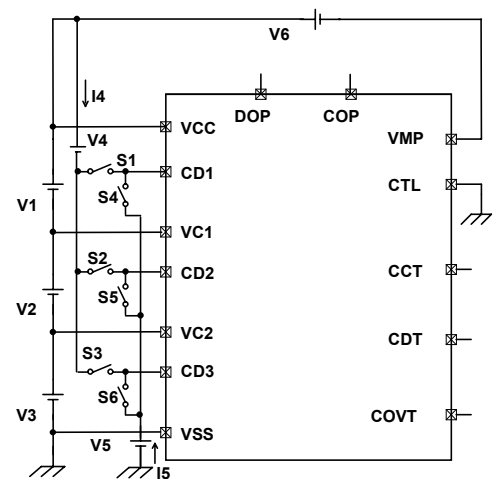
Measurement circuit 5



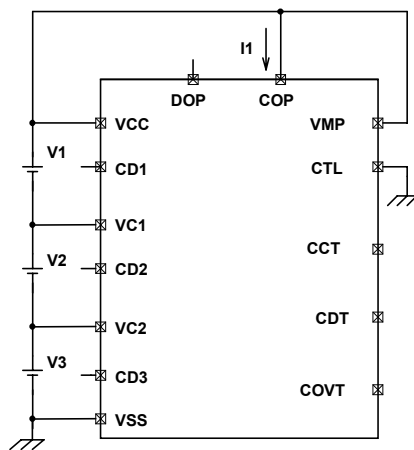
Measurement circuit 6



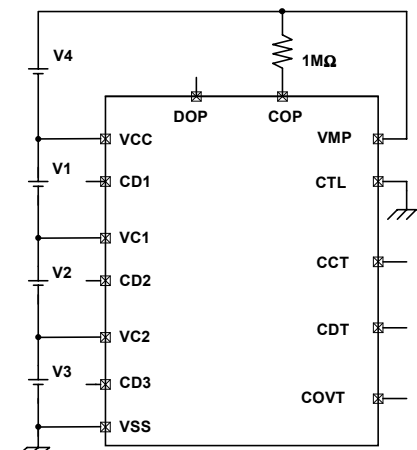
Measurement circuit 7



Measurement circuit 8



Measurement circuit 9



Measurement circuit 10

■ Description

Normal condition

This IC monitors the voltages of the three serially-connected batteries and the discharge current to control charging and discharging. If the voltages of all the three batteries are in the range from the over discharge detection voltage (VDD) to the over charge detection voltage (VCU), and the current flowing through the batteries becomes equal or lower than a specified value (the VMP terminal voltage is equal or lower than over current detection voltage 1), the charging and discharging FETs turn on. In this condition, charging and discharging can be carried out freely. This condition is called the normal condition. In this condition, output voltage of CSO, ISO and DSO go 'low'. VCC terminals are shorted by the Rvcm resistor.

Over current condition

This IC is provided with the three over current detection levels (VIOV1, VIOV2 and VIOV3) and the three over current detection delay time (tIOV1, tIOV2 and tIOV3) corresponding to each over current detection level.

If the discharging current becomes equal to or higher than a specified value (the VMP terminal voltage is equal to or higher than the over current detection voltage) during discharging under normal condition and it continues for the over current detection delay time (tIOV) or longer, the discharging FET turns off to stop discharging. This condition is called an over current condition. The VMP and VCC terminals are shorted by the Rvcm resistor at this time. The charging FET turns off.

When the discharging FET is off and a load is connected, the VMP terminal voltage equals the VSS potential. In this condition, output voltage of ISO goes 'High'.

The over current condition returns to the normal condition when the load is released and the impedance between the EB- and EB+ terminals (see Figure 7 for a connection example) is 100MΩ or higher.

When the load is released, the VMP terminal, which and the VCC terminal are shorted with the Rvcm resistor, goes back to the VCC potential. The IC detects that the VMP terminal potential returns to over current detection voltage 1 (VIOV1) or lower (or the over current detection voltage 2 (VIOV2) or lower if the COVT terminal is fixed at the 'L' level and over current detection 1 is inhibited) and returns to the normal condition. At that time, output voltage of ISO goes 'Low'.

Over charge condition

If one of the battery voltages becomes higher than the over charge detection voltage (VCU) during charging under normal condition and it continues for the over charge detection delay time (tCU) or longer, the charging FET turns off to stop charging. This condition is called the over charge condition. The 'H' level signal is output to the conditioning terminal corresponding to the battery which exceeds the over charge detection voltage until the battery becomes equal to lower than the over charge release voltage (VCD). The battery can be discharged by connecting an Nch FET externally. The discharging current can be limited by inserting R11, R12 and R13 resistors (see Figure 7 for a connection example). The VMP and VCC terminals are shorted by the Rvcm resistor under the over charge condition. In this condition, output voltage of CSO is 'High'.

The over charge condition is released in two cases:

- 1) The battery voltage which exceeded the over charge detection voltage (VCU) falls below the over charge release voltage (VCD), the charging FET turns on and the normal condition returns.
- 2) If the battery voltage which exceeded the over charge detection voltage (VCU) is equal or higher than the over charge release voltage (VCD), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal condition returns.

The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VMP terminal voltage decreases by about 0.6 V from the VCC terminal voltage momentarily. The IC detects this voltage (over current detection voltage 1 or higher), releases the over charge condition and returns to

the normal condition. At that time, output voltage of CSO goes 'Low'.

Over discharge condition

If any one of the battery voltages falls below the over discharge detection voltage (VDD) during discharging under normal condition and it continues for the over discharge detection delay time (tDD) or longer, the discharging FET turns off and discharging stops. This condition is called the over discharge condition. In this condition, output voltage of DSO goes 'High'. When the discharging FET turns off, the VMP terminal voltage becomes equal to the VSS voltage and the IC's current consumption falls below the power-down current consumption (IPDN). This condition is called the power-down condition. The VMP and VSS terminals are shorted by the Rvsm resistor under the over discharge and power-down conditions.

The power-down condition is canceled when the charger is connected and the voltage between VMP and VSS is 3.0 V or higher (over current detection voltage 3). When all the battery voltages becomes equal to or higher than the over discharge release voltage (VDU) in this condition, the over discharge condition changes to the normal condition. In this condition, output voltage of DSO goes 'Low'.

Delay circuits

The over charge detection delay time (tCU1 to tCU3), over discharge detection delay time (tDD1 to tDD3), and over current detection delay time 1 (tIOV1) are changed with external capacitors (C4 to C6). The delay times are calculated by the following equations:

	Min	Typ.	Max.
TCU[S]	=Delay factor (1.07, 2.13, 3.19)×C4 [uF]		
TDD[S]	=Delay factor (0.20, 0.40, 0.60)×C5 [uF]		
TIOV1[S]	=Delay factor (0.10, 0.20, 0.30)×C6 [uF]		

Note: The delay time for over current detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

CTL terminal

If the CTL terminal is floated under normal condition, it is pulled up to the VCC potential in the IC, and both the charging and discharging FETs turn off to inhibit charging and discharging. Both charging and discharging are also inhibited by applying the VCC terminal to the CTL terminal externally. At this time, the VMP and VCC terminals are shorted by the Rvcm resistor.

When the CTL terminal becomes equal to VSS potential, charging and discharging are enabled and go back to their appropriate conditions for the battery voltages.

0V battery charging function

This function is used to recharge the three serially-connected batteries after they self-discharge to 0V. When the 0V charging start voltage (V0CHAR) or higher is applied to between VMP and VSS by connecting the charger, the charging FET gate is fixed to VSS potential.

When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the over discharge release voltage (VDU), the normal condition returns.

Notes: In the products without 0V battery charging function, the resistance between VCC and VMP and between VSS and VMP are lower than the products with 0V battery charging function. It causes to that over charge detection voltage increases by the drop voltage of R5 (see Figure 7 for a

connection example) with sink current at VMP.

The COP output is undefined below 2.0V on VCC-VSS voltage in the products without 0V battery charging function.

Voltage temperature factor

Voltage temperature factor 1 indicates over charge detection voltage, over charge release voltage, over discharge detection voltage, and over discharge release voltage.

Voltage temperature factor 2 indicates over current detection voltage.

The Voltage temperature factors 1 and 2 are expressed by the oblique line parts in Figure 3.

Ex. Voltage temperature factor of over charge detection voltage

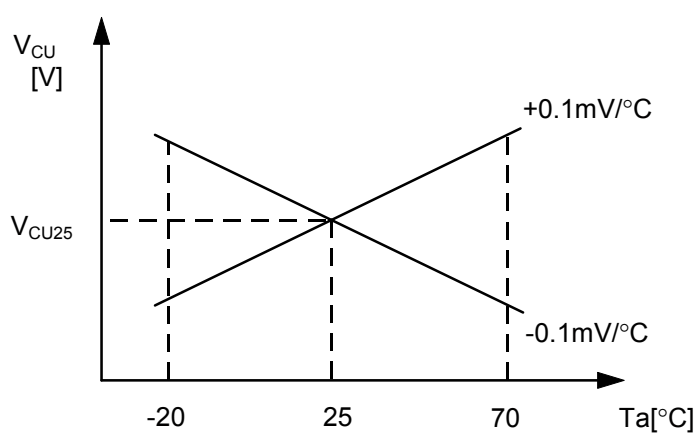


Figure 3

■ Operation Timing Charts

1. Over charge detection

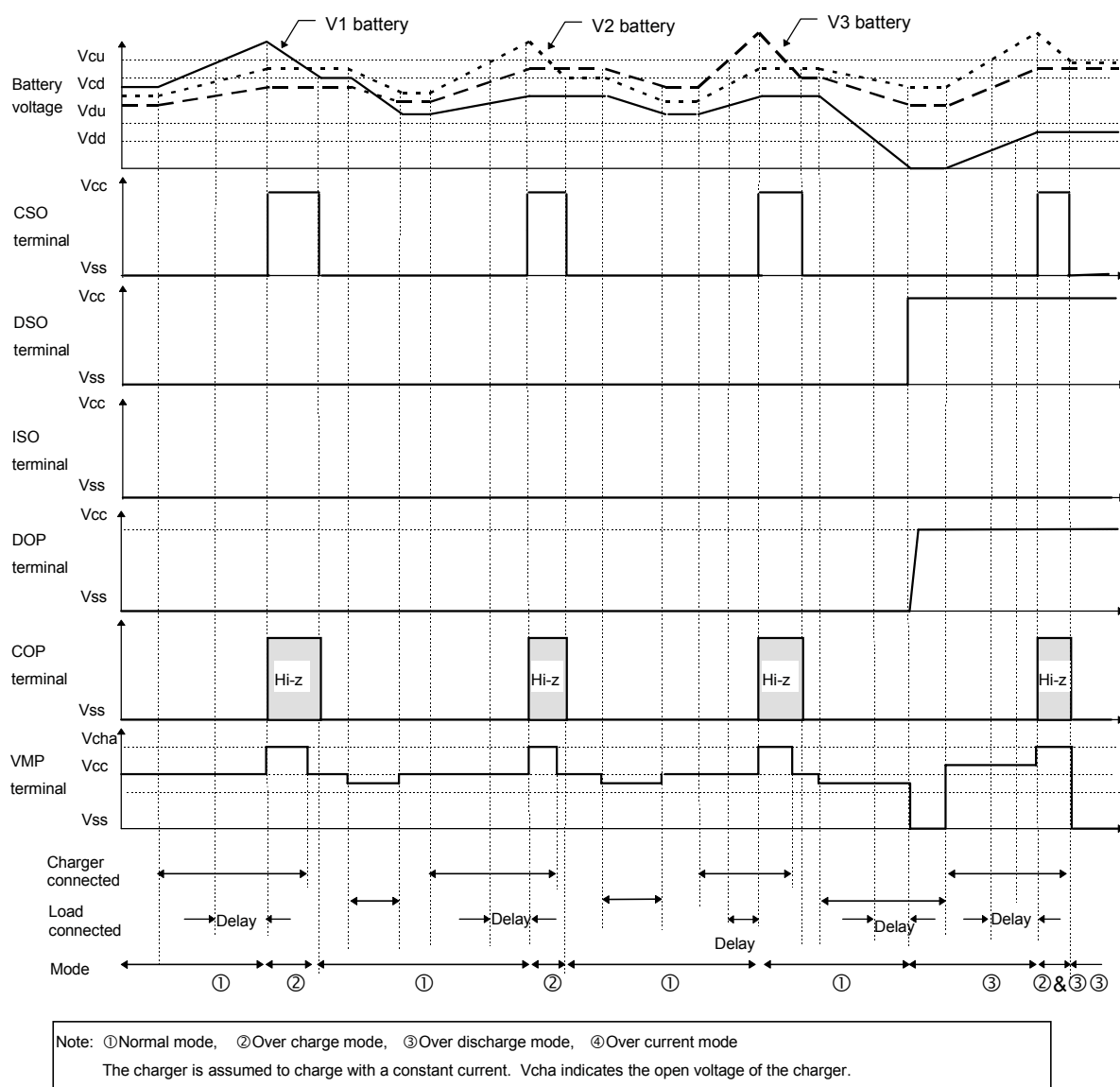


Figure 4

2. Over discharge detection

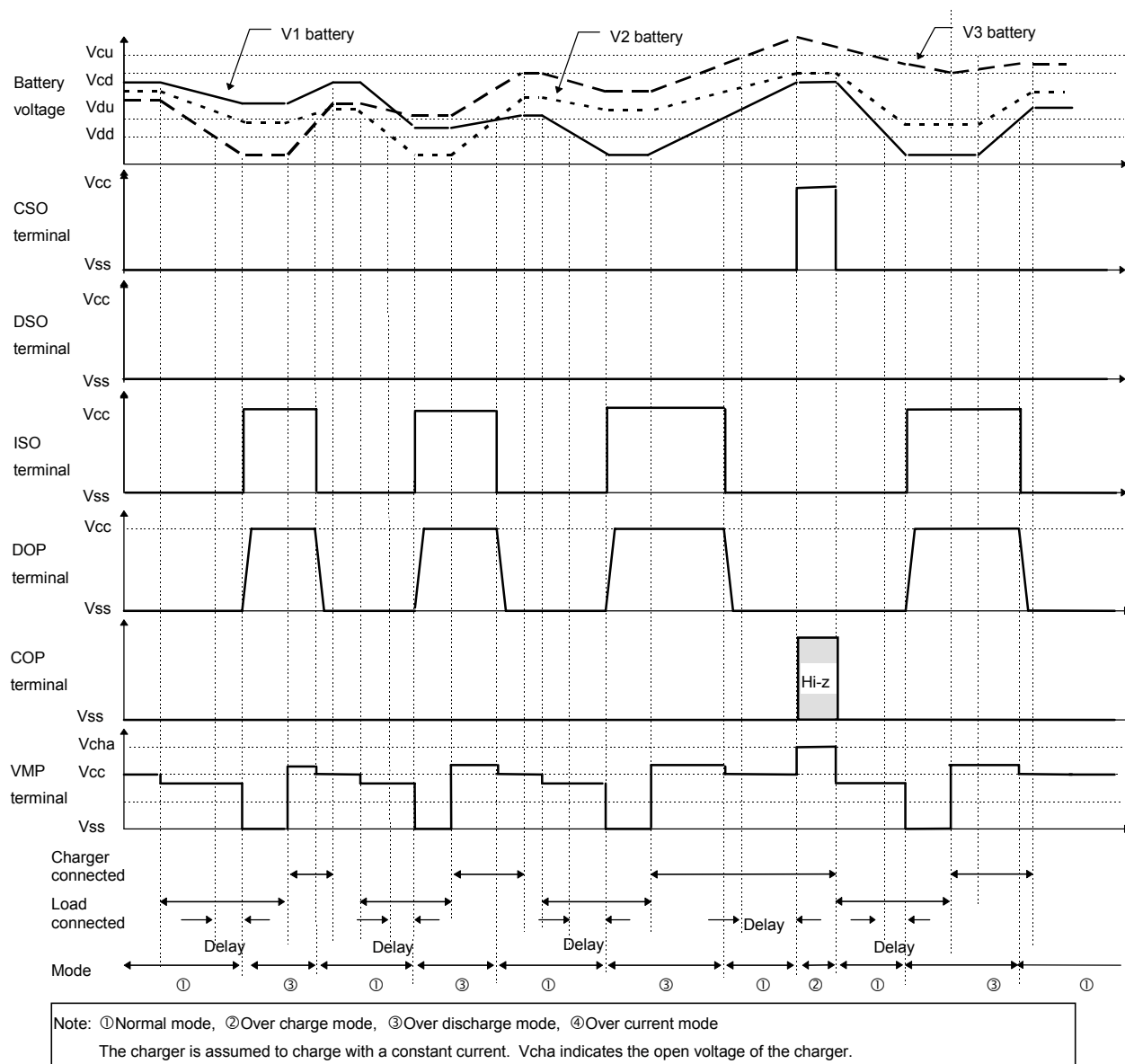


Figure 5

3. Over current detection

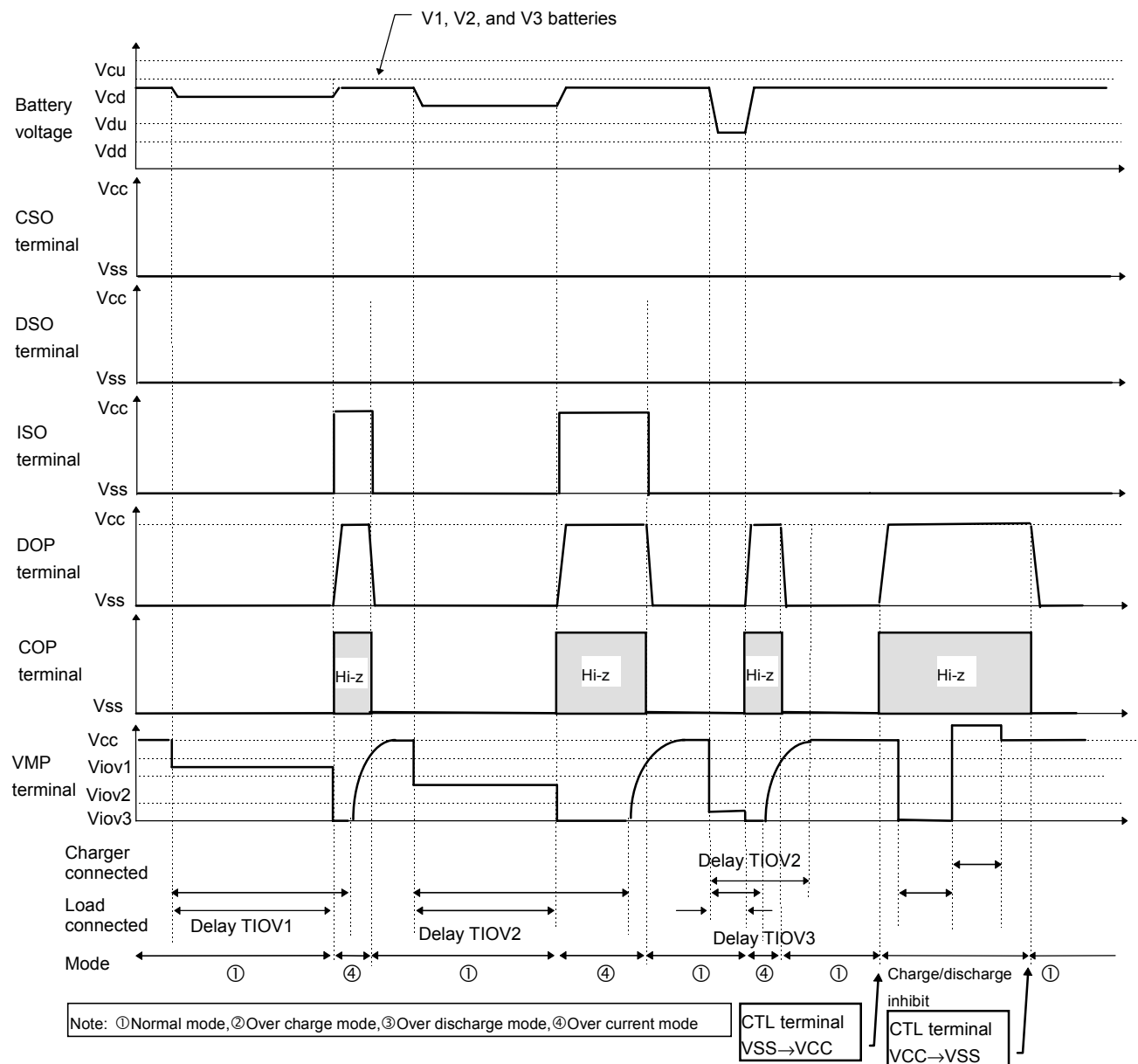


Figure 6

When the S-8233C series detects over current 1 or over current 2, ISO terminal goes 'High'. Delay time from load shorted to ISO terminal goes 'High' is TioV2(at that case delay time isn't TioV3).

■ Battery Protection IC Connection Example

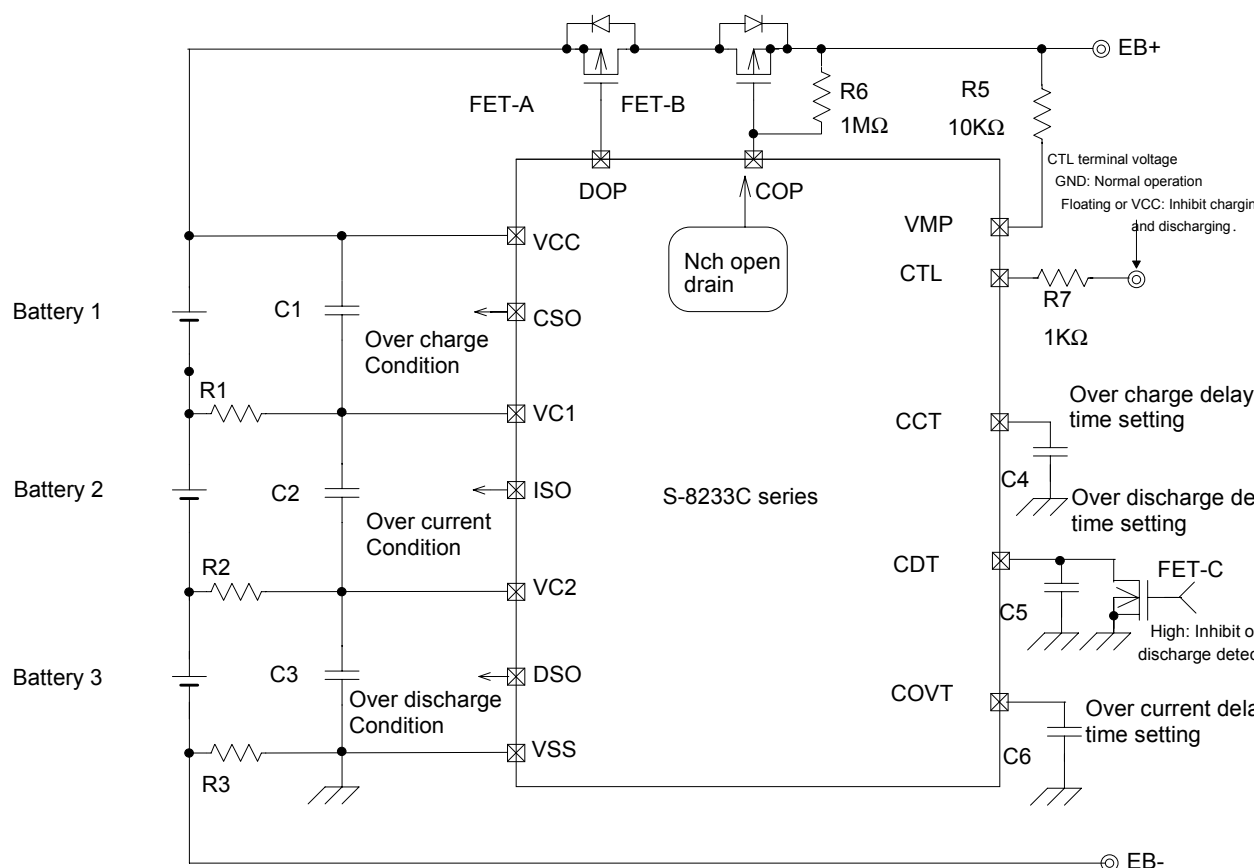


Figure 7

[Description of Figure 7]

- R11, R12, and R13 are used to adjust the battery conditioning current. The conditioning current during over charge detection is given by $V_{cu} / (R + R_{DS(on)})$. To disable the conditioning function, open CSO, ISO, and DSO.
- The over charge detection delay time (TCU1 to TCU3), over discharge detection delay time (TDD1 to TDD3), and over current detection delay time (TI0V1) are changed with external capacitors (C4 to C6). See the electrical characteristics.
- R6 is a pull-up resistor that turns FET-B off when the COP terminal is opened. Connect a 100k Ω to 1 M Ω resistor.
- R5 is used to protect the IC if the charger is connected in reverse. Connect a 10 k Ω to 50 k Ω resistor.
- If capacitor C6 is absent, rush current occurs when a capacitive load is connected and the IC enters the over current mode. C6 must be connected to prevent it.
- If capacitor C5 is not connected, the IC may enter the over discharge condition due to variations of battery voltage when the over current occurs. In this case, a charger must be connected to return to the normal condition. To prevent this, connect an at least 0.01 μ F capacitor to C5.
- If a leak current flows between the delay capacitor connection terminal (CCT, CDT, or COVT) and VSS, the delay time increases and an error occurs. The leak current must be 100 nA or less.
- Over discharge detection can be disabled by using FET-C. The FET-C off leak must be 0.1 μ A or less. If over discharge is inhibited by using this FET, the current consumption does not fall below 0.1 μ A even when the battery voltage drops and the IC enters the over discharge detection mode.
- R1, R2, and R3 must be 1k Ω or less.
- R7 is the protection of the CTL when the CTL terminal voltage higher than VCC voltage. Connect a 300 Ω to 5k Ω resistor. If the CTL terminal voltage never greater than the VCC voltage (ex. R7 connect to VSS), without R7 resistor is allowed.

Notes:

- If any electrostatic discharge of 2000 V or higher is not applied to the S-8233 series with a human body model, R1, R2, R3, C1, C2, and C3 are unnecessary.
- The above connection diagram and constants do not guarantee proper operations. Evaluate your actual application and set constants properly.

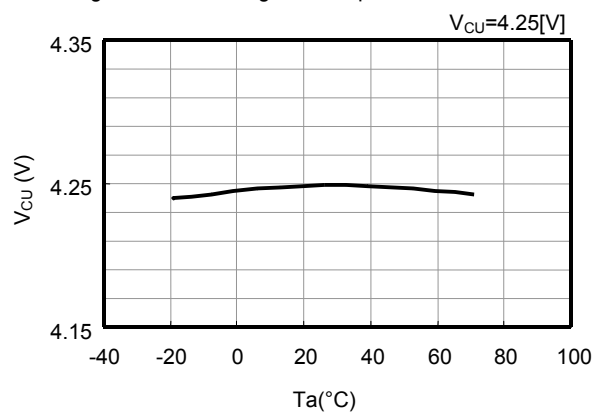
■ Precautions

- If a charger is connected in the over discharge condition and one of the battery voltages becomes equal to or higher than the over charge release voltage (VCU) before the battery voltage which is below the over discharge detection voltage (VDD) becomes equal to or higher than the over discharge release voltage (VDU), the over discharge and over charge conditions are entered and the charging and discharging FETs turn off. Both charging and discharging are disabled. If the battery voltage which was higher than the over charge detection voltage (VCU) falls to the over charge release voltage (VCD) due to internal discharging, the charging FET turns on. If the charger is detached in the over charge and over discharge condition, the over charge condition is released, but the over discharge condition remains. If the charger is connected again, the battery condition is monitored after that. The charging FET turns off after the over charge detection delay time, the over charge and over discharge conditions are entered.
- If any one of the battery voltages is equal to or lower than the over discharge release voltage (VDU) when they are connected for the first time, the normal condition may not be entered. If the VMP terminal voltage is made equal to or higher than the VCC voltage (if a charger is connected), the normal condition is entered.
- If the CTL terminal floats in power-down mode, it is not pulled up in the IC, charging and discharging may not be inhibited. However, the over discharge condition becomes effective. If the charger is connected, the CTL terminal is pulled up, and charging and discharging are inhibited immediately.

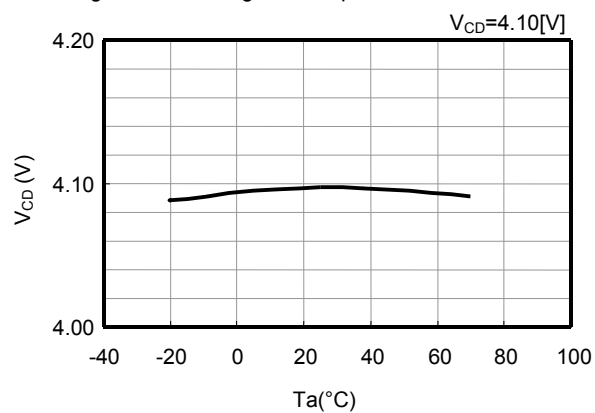
■ Characteristics (typical characteristics)

Detection voltage temperature characteristics

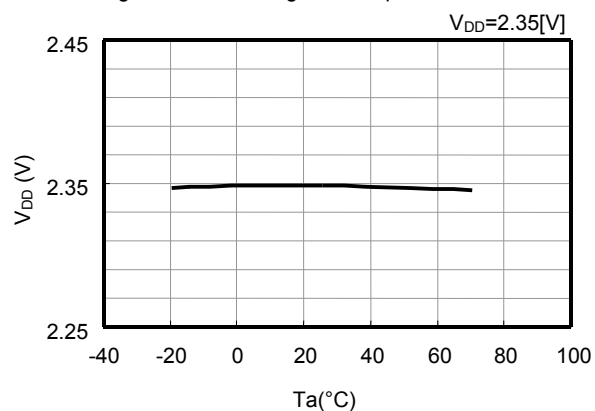
Overcharge detection voltage vs. temperature



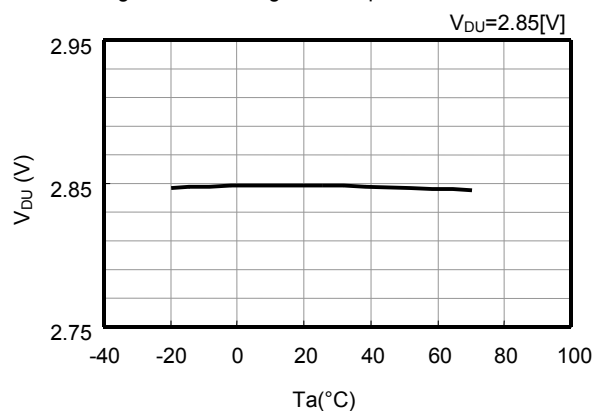
Overcharge release voltage vs. temperature



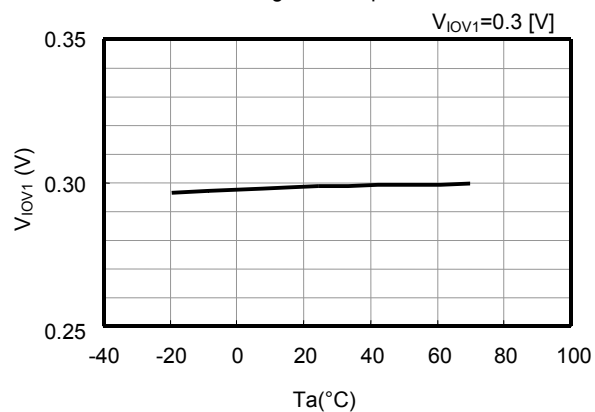
Overdischarge detection voltage vs. temperature



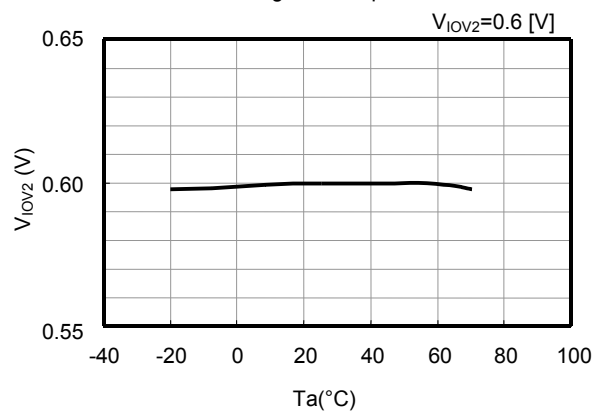
Overdischarge release voltage vs. temperature



Overcurrent1 detection voltage vs. temperature

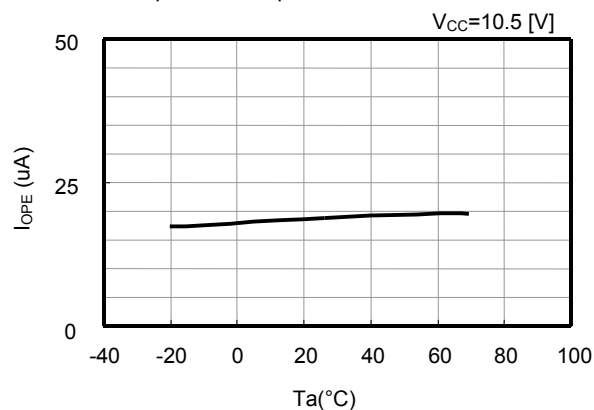


Overcurrent2 detection voltage vs. temperature

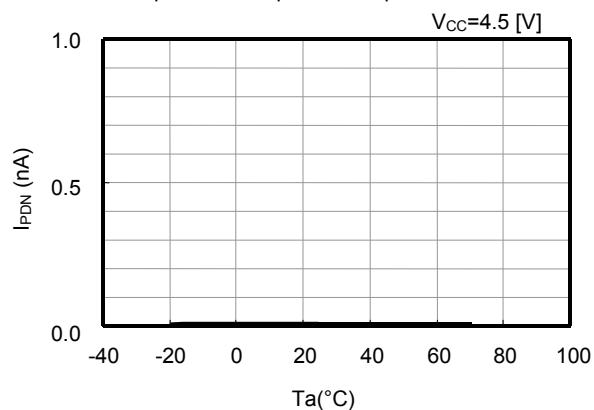


2. Current consumption temperature characteristics

Current consumption vs. temperature in normal mode

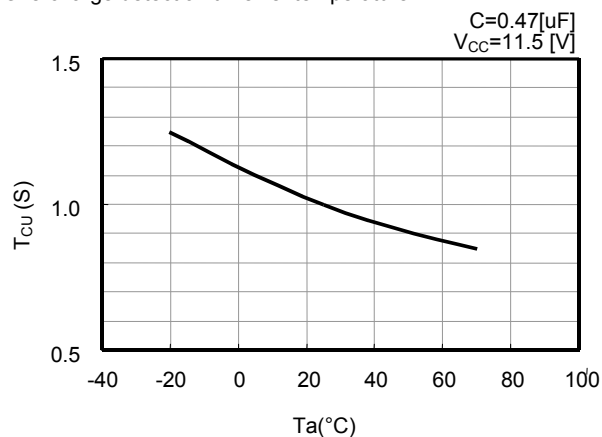


Current consumption vs. temperature in power-down mode

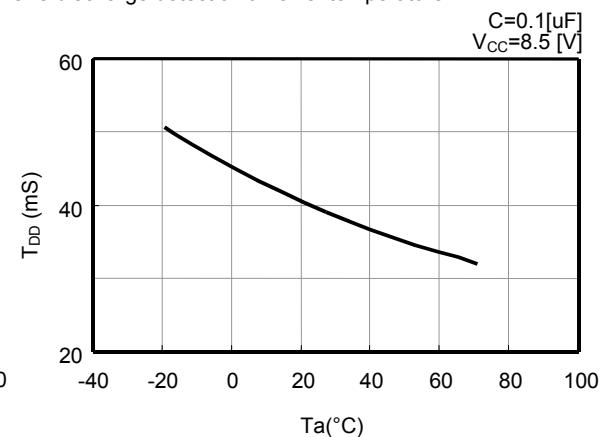


3. Delay time temperature characteristics

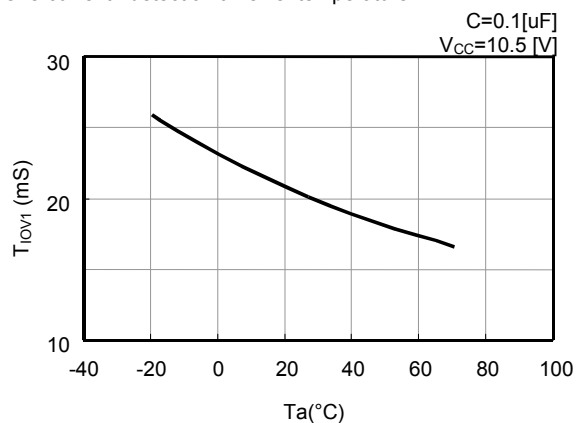
Overcharge detection time vs. temperature



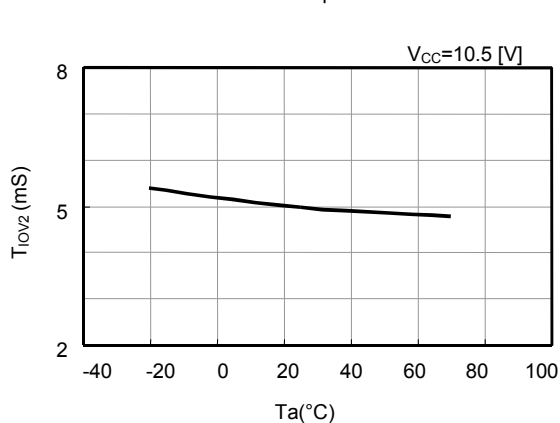
Overdischarge detection time vs. temperature



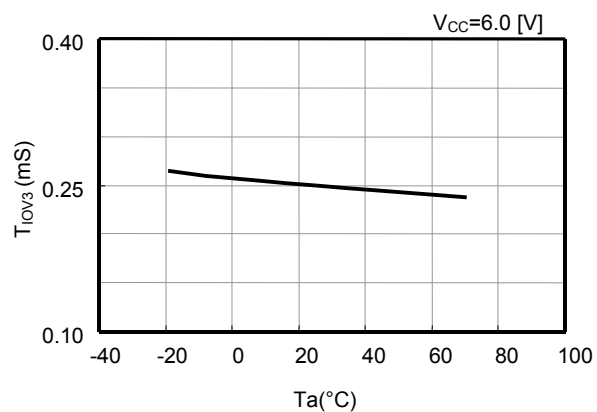
Overcurrent1 detection time vs. temperature



Overcurrent2 detection time vs. temperature

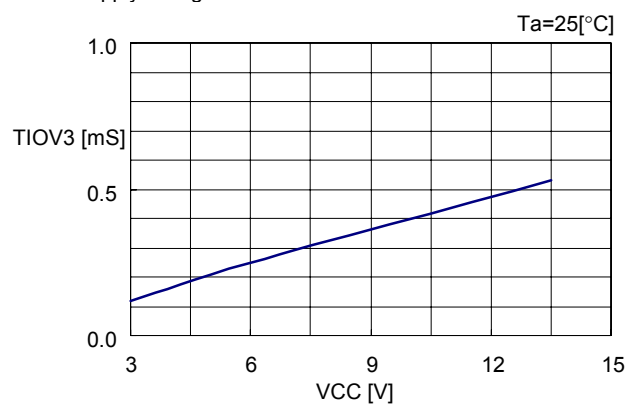


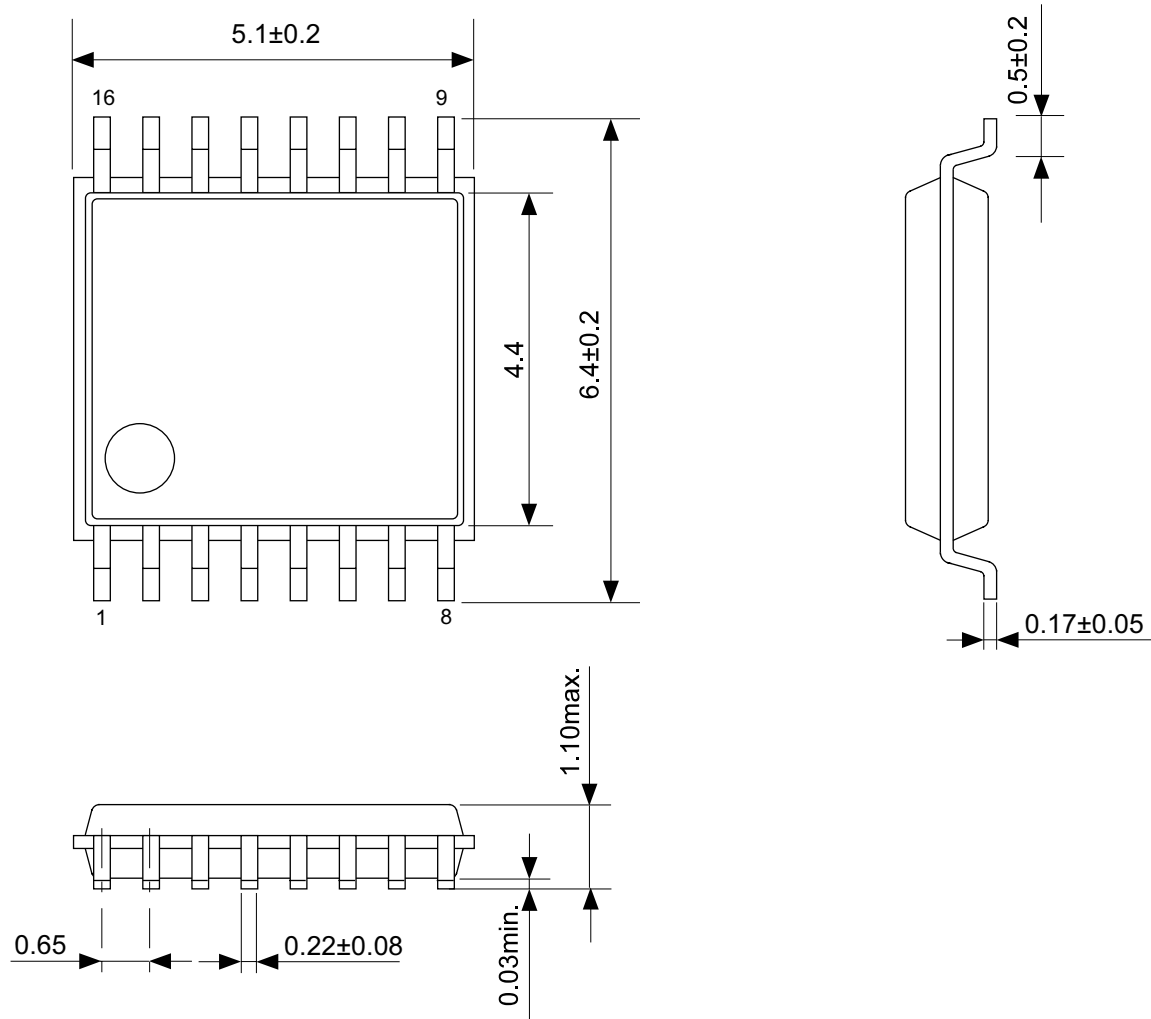
Overcurrent3 (load short) detection time vs. temperature



4. Delay time vs. power supply voltage

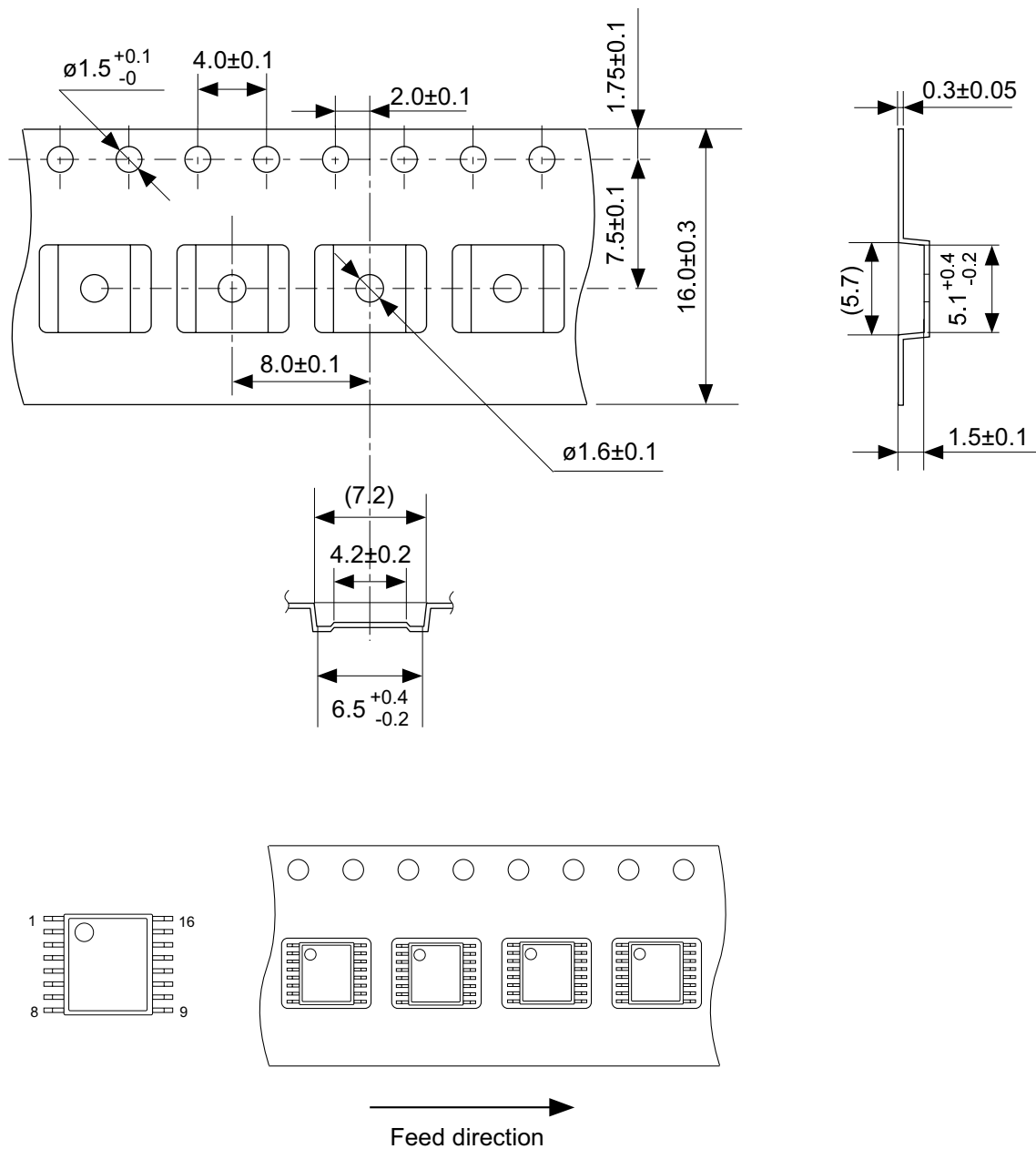
Over current 3 (load short) detection time vs. power supply voltage





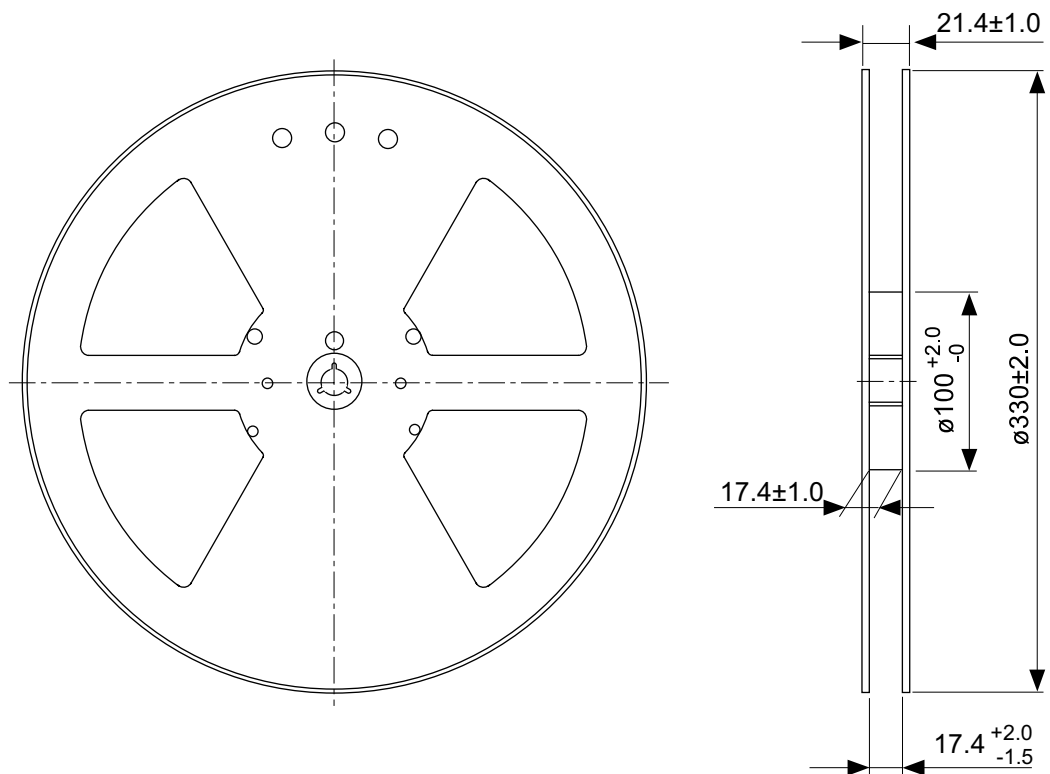
No. FT016-A-P-SD-1.1

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

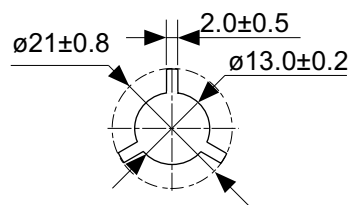


No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-SD-1.1

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.