

# BATTERY PROTECTION IC FOR 2-SERIAL OR 3-SERIAL-CELL PACK

## S-8253A/B Series

The S-8253A/B Series are protection ICs for 2-serial or 3-serial cell lithium-ion rechargeable batteries and include high-accuracy voltage detectors and delay circuits.

These ICs are suitable for protecting lithium-ion battery packs from overcharge, overdischarge and overcurrent.

### ■ Features

- (1) High-accuracy voltage detection for each cell
  - Overcharge detection voltage  $n$  ( $n = 1$  to  $3$ )      3.9 V to 4.4 V (50 mV steps)      Accuracy  $\pm 25$  mV
  - Overcharge release voltage  $n$  ( $n = 1$  to  $3$ )      3.8 V to 4.4 V<sup>\*1</sup>      Accuracy  $\pm 50$  mV
  - \*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage  $n$  ( $n = 1$  to  $3$ ) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV steps.)
  - Overdischarge detection voltage  $n$  ( $n = 1$  to  $3$ )      2.0 V to 3.0 V (100 mV steps)      Accuracy  $\pm 80$  mV
  - Overdischarge release voltage  $n$  ( $n = 1$  to  $3$ )      2.0 V to 3.4 V<sup>\*2</sup>      Accuracy  $\pm 100$  mV
  - \*2. Overdischarge release voltage = Overdischarge release voltage – Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage  $n$  ( $n = 1$  to  $3$ ) can be selected as 0 V or from a range of 0.2 V to 0.7 V in 100 mV steps.)
- (2) Three-level overcurrent detection (including load short circuiting detection)
  - Overcurrent detection voltage 1      0.05 V to 0.30 V (50 mV steps)      Accuracy  $\pm 25$  mV
  - Overcurrent detection voltage 2      0.5 V (fixed)
  - Overcurrent detection voltage 3      1.2 V (fixed)
- (3) Delay times (overcharge, overdischarge, overcurrent) are generated by an internal circuit (external capacitors are unnecessary).
- (4) Charge/discharge operation can be inhibited via the control pin.
- (5) 0 V battery charge function available/unavailable are selectable.
- (6) High-voltage withstand devices      Absolute maximum rating: 26 V
- (7) Wide operating voltage range      2 V to 24 V
- (8) Wide operating temperature range       $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- (9) Low current consumption
  - Operation mode      28  $\mu\text{A}$  max. ( $+25^{\circ}\text{C}$ )
  - Power-down mode      0.1  $\mu\text{A}$  max. ( $+25^{\circ}\text{C}$ )

### ■ Applications

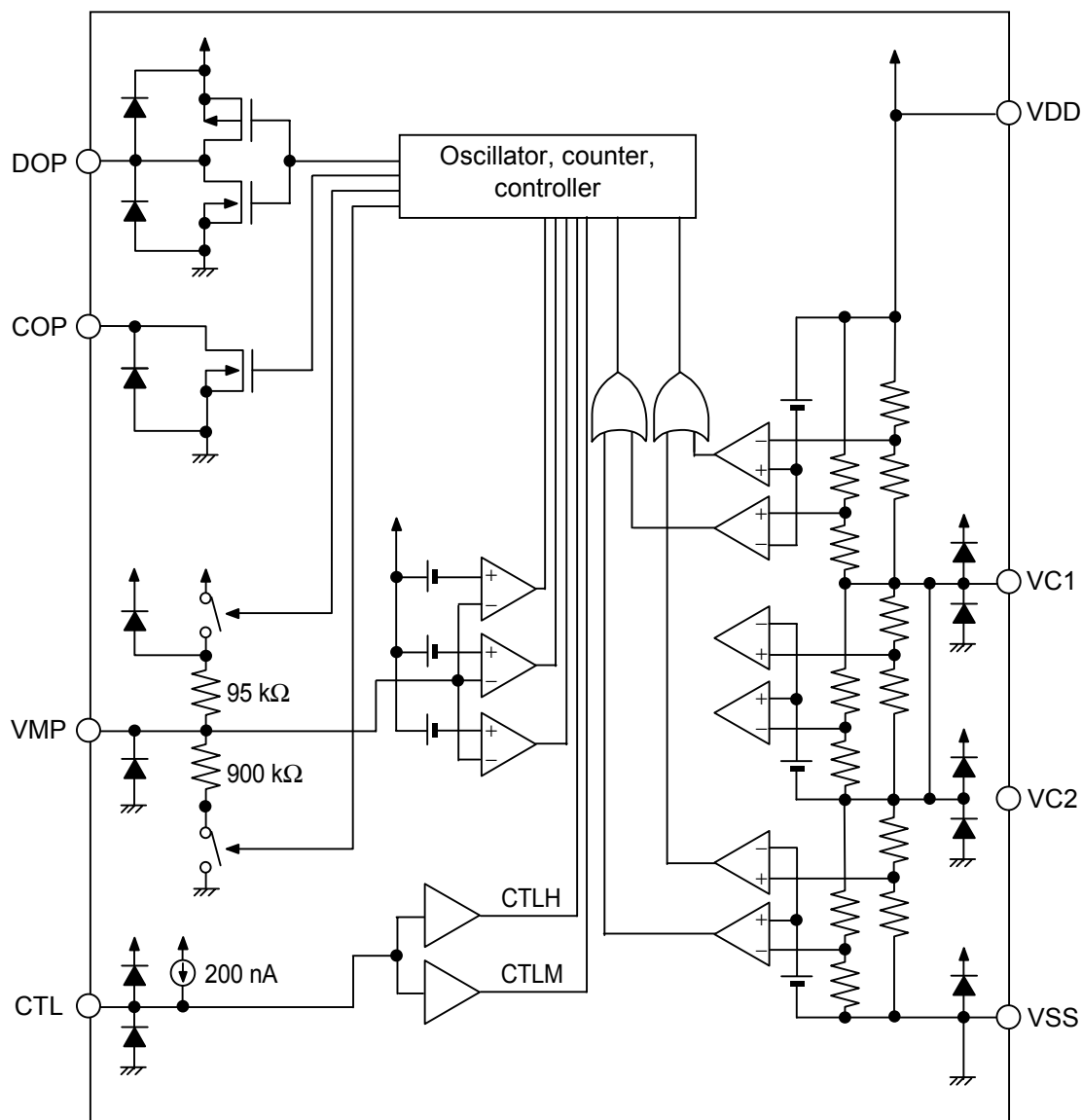
- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

### ■ Package

- 8-Pin TSSOP (Package drawing code: FT008-D)

■ **Block Diagram**

(1) S-8253A Series



**Figure 1 Block Diagram (S-8253A Series)**

(2) S-8253B Series

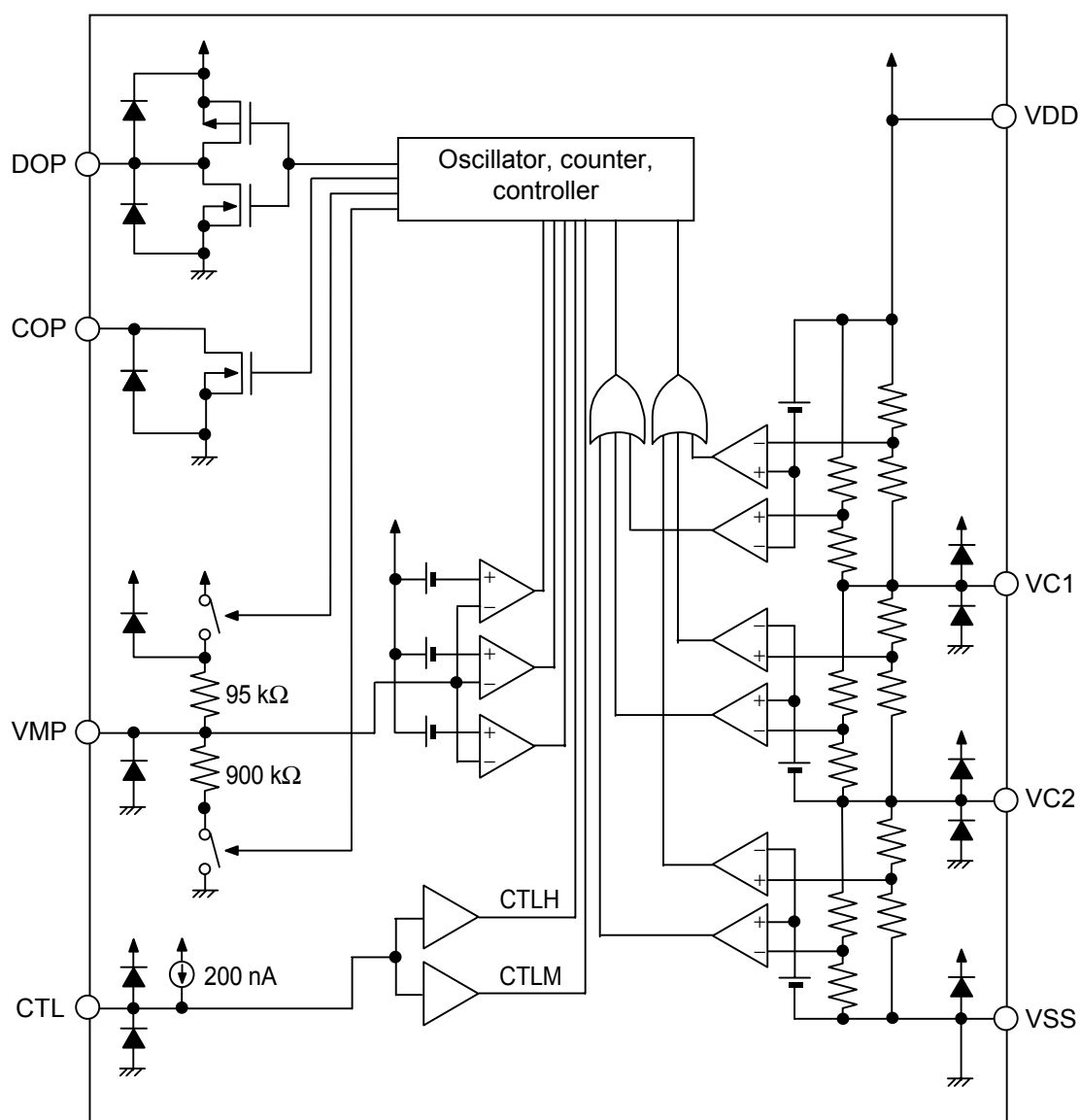
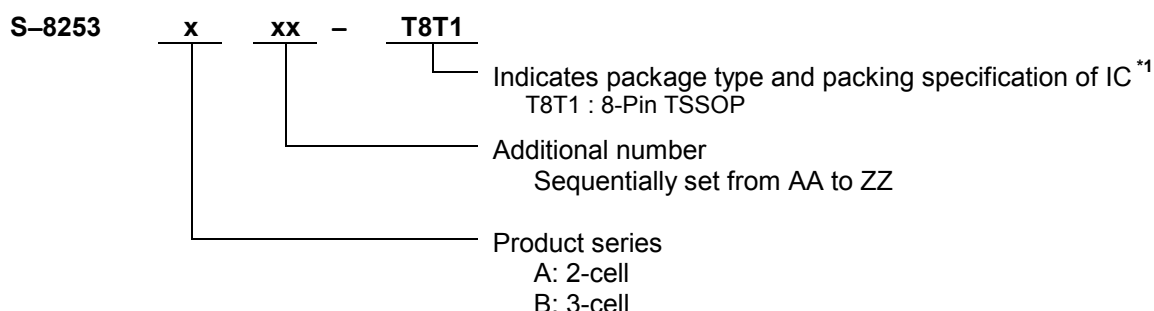


Figure 2 Block Diagram (S-8253B Series)

## ■ Product Code Structure

### 1. Product Name



\*1. Refer to the taping drawing.

### 2. Product Name List

**Table 1 S-8253A Series (for 2-Serial Cell)**

Product Name/Parameter	Overcharge Detection Voltage $V_{CU}$	Overcharge Release Voltage $V_{CL}$	Overdischarge Detection Voltage $V_{DL}$	Overdischarge Release Voltage $V_{DU}$	Overcurrent Detection Voltage 1 $V_{IOV1}$	0 V Battery Charge
S-8253AAA-T8T1	$4.35 \pm 0.025$ V	$4.05 \pm 0.050$ V	$2.40 \pm 0.080$ V	$2.70 \pm 0.100$ V	$0.30 \pm 0.025$ V	Available

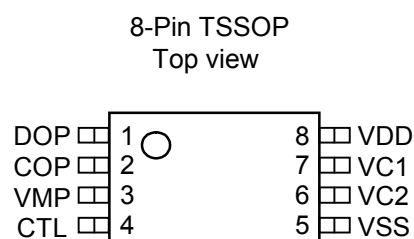
**Remark** If a product with the required detection voltage does not appear in the above list, contact our sales office.

**Table 2 S-8253B Series (for 3-Serial Cell)**

Product Name/Parameter	Overcharge Detection Voltage $V_{CU}$	Overcharge Release Voltage $V_{CL}$	Overdischarge Detection Voltage $V_{DL}$	Overdischarge Release Voltage $V_{DU}$	Overcurrent Detection Voltage 1 $V_{IOV1}$	0 V Battery Charge
S-8253BAA-T8T1	$4.35 \pm 0.025$ V	$4.05 \pm 0.050$ V	$2.40 \pm 0.080$ V	$2.70 \pm 0.100$ V	$0.30 \pm 0.025$ V	Available

**Remark** If a product with the required detection voltage does not appear in the above list, contact our sales office.

### ■ Pin Assignment



**Figure 3**

**Table 3 S-8253A Series**

Pin No.	Pin Name	Function
1	DOP	Connection of discharge control FET gate (CMOS output)
2	COP	Connection of charge control FET gate (Nch open-drain output)
3	VMP	Voltage detection between VDD and VMP (overcurrent detection pin)
4	CTL	Input of charge/discharge control signal, pin for shortening test time (L: Normal operation, H: Charge/discharge inhibited, M ( $V_{DD} \times 1/2$ ): Test time reduced)
5	VSS	Negative power supply input, negative voltage connection for battery 2
6	VC2	No connection <sup>*1</sup>
7	VC1	Connection for negative voltage of battery 1 and positive voltage of battery 2
8	VDD	Connection for positive power supply input and positive voltage of battery 1

<sup>\*1</sup>. No connection is electrically open.

This pin can be connected to VDD or VSS.

**Remark** For the external views, refer to package drawings.

**Table 4 S-8253B Series**

Pin No.	Pin Name	Function
1	DOP	Connection of discharge control FET gate (CMOS output)
2	COP	Connection of charge control FET gate (Nch open-drain output)
3	VMP	Voltage detection between VDD and VMP (overcurrent detection pin)
4	CTL	Input of charge/discharge control signal, pin for shortening test time (L: Normal operation, H: Charge/discharge inhibited, M ( $V_{DD} \times 1/2$ ): Test time reduced)
5	VSS	Connection for negative power supply input and negative voltage of battery 3
6	VC2	Connection for negative voltage of battery 2 and positive voltage of battery 3
7	VC1	Connection for negative voltage of battery 1 and positive voltage of battery 2
8	VDD	Connection for positive power supply input and positive voltage of battery 1

**Remark** For the external views, refer to package drawings.

■ **Absolute Maximum Ratings**

**Table 5**

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Applicable Pins	Rating	Unit
Input voltage between VDD and VSS	$V_{DS}$	—	$V_{SS} - 0.3$ to $V_{SS} + 26$	V
Input pin voltage	$V_{IN}$	VC1, VC2	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
VMP pin input voltage	$V_{VMP}$	VMP	$V_{SS} - 0.3$ to $V_{SS} + 26$	
DOP pin output voltage	$V_{DOP}$	DOP	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
COP pin output voltage	$V_{COP}$	COP	$V_{SS} - 0.3$ to $V_{VMP} + 0.3$	
CTL input pin voltage	$V_{IN\_CTL}$	CTL	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
Power dissipation	$P_D$	—	300	mW
Operating temperature range	$T_{opr}$	—	-40 to +85	°C
Storage temperature range	$T_{stg}$	—	-40 to +125	

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

# BATTERY PROTECTION IC FOR 2-SERIAL OR 3-SERIAL-CELL PACK

Rev.2.1\_00

S-8253A/B Series

## ■ Electrical Characteristics

Table 6

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Conditions	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage n	V <sub>CU<sub>n</sub></sub>	3.90 to 4.40 V, adjustable	V <sub>CU<sub>n</sub></sub> - 0.025	V <sub>CU<sub>n</sub></sub>	V <sub>CU<sub>n</sub></sub> + 0.025	V	1	1
Overcharge release voltage n	V <sub>CL<sub>n</sub></sub>	3.80 to 4.40 V, adjustable	V <sub>CL<sub>n</sub></sub> - 0.05	V <sub>CL<sub>n</sub></sub>	V <sub>CL<sub>n</sub></sub> + 0.05	V	1	1
		V <sub>CL</sub> = V <sub>CU</sub>	V <sub>CL<sub>n</sub></sub> - 0.025	V <sub>CL<sub>n</sub></sub>	V <sub>CL<sub>n</sub></sub> + 0.025			
Overdischarge detection voltage n	V <sub>DL<sub>n</sub></sub>	2.0 to 3.0 V, adjustable	V <sub>DL<sub>n</sub></sub> - 0.080	V <sub>DL<sub>n</sub></sub>	V <sub>DL<sub>n</sub></sub> + 0.080	V	1	1
Overdischarge release voltage n	V <sub>DU<sub>n</sub></sub>	2.0 to 3.40 V, adjustable	V <sub>DU<sub>n</sub></sub> - 0.10	V <sub>DU<sub>n</sub></sub>	V <sub>DU<sub>n</sub></sub> + 0.10	V	1	1
		V <sub>DL</sub> = V <sub>DU</sub>	V <sub>DU<sub>n</sub></sub> - 0.08	V <sub>DU<sub>n</sub></sub>	V <sub>DU<sub>n</sub></sub> + 0.08			
Overcurrent detection voltage 1	V <sub>IOV1</sub>	0.05 to 0.3 V, adjustable	V <sub>IOV1</sub> - 0.025	V <sub>IOV1</sub>	V <sub>IOV1</sub> + 0.025	V	2	1
Overcurrent detection voltage 2	V <sub>IOV2</sub>	—	V <sub>DD</sub> - 0.60	V <sub>DD</sub> - 0.50	V <sub>DD</sub> - 0.40	V	2	1
Overcurrent detection voltage 3	V <sub>IOV3</sub>	—	V <sub>DD</sub> - 1.5	V <sub>DD</sub> - 1.2	V <sub>DD</sub> - 0.9	V	2	1
Temperature coefficient 1	T <sub>COE1</sub>	Ta = 0 to 50°C <sup>*1</sup>	-1.0	0	1.0	mv/°C	—	—
Temperature coefficient 2	T <sub>COE2</sub>	Ta = 0 to 50°C <sup>*2</sup>	-0.5	0	0.5	mv/°C	—	—
DELAY TIME								
Overcharge detection delay time	t <sub>CU</sub>	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t <sub>DL</sub>	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t <sub>IOV1</sub>	—	7.2	9	10.8	ms	4	1
Overcurrent detection delay time 2	t <sub>IOV2</sub>	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t <sub>IOV3</sub>	FET gate capacitance = 2000 pF	150	320	540	μs	4	1
0 V BATTERY CHARGE FUNCTION								
0 V charge starting charger voltage	V <sub>0CHA</sub>	0 V charge available	—	0.8	1.5	V	12	5
0 V battery charge inhibition battery voltage	V <sub>0INH</sub>	0 V charge un available	0.4	0.7	1.1	V	12	5
INTERNAL RESISTANCE								
Resistance between VMP and VDD	R <sub>VMD</sub>	V1 = V2 = V3 = 3.5 V V <sub>VMP</sub> = V <sub>SS</sub>	70	95	120	kΩ	6	2
Resistance between VMP and VSS	R <sub>VMS</sub>	V1 = V2 = V3 = 1.8 V V <sub>VMP</sub> = V <sub>DD</sub>	450	900	1800	kΩ	6	2
INPUT VOLTAGE								
Operating voltage between VDD and VSS	V <sub>DSOP</sub>	Output voltage of DOP and COP fixed	2	—	24	V	—	—
CTL input voltage, high	V <sub>CTLH</sub>	—	V <sub>DD</sub> - 0.5	—	—	V	7	1
CTL input voltage, low	V <sub>CTLL</sub>	—	—	—	V <sub>SS</sub> + 0.5	V	7	1
INPUT CURRENT								
Current consumption during operation	I <sub>OPe</sub>	V1 = V2 = V3 = 3.5 V	—	14	28	μA	5	2
Current consumption at power down	I <sub>PDN</sub>	V1 = V2 = V3 = 1.5 V	—	—	0.1	μA	5	2
VC1 pin current	I <sub>VC1</sub>	V1 = V2 = V3 = 3.5 V	-0.3	0	0.3	μA	9	3
VC2 pin current	I <sub>VC2</sub>	V1 = V2 = V3 = 3.5 V	-0.3	0	0.3	μA	9	3
CTL pin current, high	I <sub>CTLH</sub>	V1 = V2 = V3 = 3.5 V V <sub>CTL1</sub> = V <sub>DD</sub>	—	—	0.1	μA	8	3
CTL pin current, low	I <sub>CTLL</sub>	V1 = V2 = V3 = 3.5 V V <sub>CTL1</sub> = V <sub>SS</sub>	-0.4	-0.2	—	μA	8	3
OUTPUT CURRENT								
COP pin leakage current	I <sub>COH</sub>	V <sub>COP</sub> = 24 V	—	—	0.1	μA	10	4
COP pin sink current	I <sub>COL</sub>	V <sub>COP</sub> = V <sub>SS</sub> + 0.5 V	10	—	—	μA	10	4
DOP pin source current	I <sub>DOH</sub>	V <sub>DOP</sub> = V <sub>DD</sub> - 0.5 V	10	—	—	μA	11	4
DOP pin sink current	I <sub>DOL</sub>	V <sub>DOP</sub> = V <sub>SS</sub> + 0.5 V	10	—	—	μA	11	4

\*1. Voltage temperature coefficient 1: Overcharge detection voltage

\*2. Voltage temperature coefficient 2: Overcurrent detection voltage 1

## ■ Test Circuits

### 1. Overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, overdischarge release voltage

#### (Test condition 1, test circuit 1)

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP and DOP pins are low ( $V_{DD} \times 0.1\text{ V}$  or lower) (this status is referred to as the initial status).

- **Overcharge detection voltage 1 ( $V_{CU1}$ ), overcharge release voltage 1 ( $V_{CL1}$ )**

Overcharge detection voltage 1 ( $V_{CU1}$ ) is the voltage of V1 when the voltage of the COP pin is high ( $V_{DD} \times 0.9\text{ V}$  or more) after the V1 voltage has been gradually increased starting at the initial status. Overcharge release voltage 1 ( $V_{CL1}$ ) is the voltage of V1 when the voltage at the COP pin is low after the V1 voltage has been gradually decreased.

- **Overdischarge detection voltage 1 ( $V_{DL1}$ ), overdischarge release voltage 1 ( $V_{DU1}$ )**

Overdischarge detection voltage 1 ( $V_{DL1}$ ) is the voltage of V1 when the voltage of the DOP pin is high after the V1 voltage has been gradually decreased starting at the initial status. Overdischarge release voltage 1 ( $V_{DU1}$ ) is the voltage of V1 when the voltage at the DOP pin is low after the V1 voltage has been gradually increased.

By changing  $V_n$  ( $n = 2$ : S-8253A Series,  $n = 2, 3$ : S-8253B Series) the overcharge detection voltage ( $V_{CUn}$ ), overcharge release voltage ( $V_{CLn}$ ), overdischarge detection voltage ( $V_{DLn}$ ), and overdischarge release voltage ( $V_{DU n}$ ) can be measured in the same way as when  $n = 1$ .

### 2. Overcurrent detection voltage

#### (Test condition 2, test circuit 1)

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP and DOP pins are low (this status is referred to as the initial status).

- **Overcurrent detection voltage 1 ( $V_{IOV1}$ )**

Overcurrent detection voltage 1 ( $V_{IOV1}$ ) is the voltage of V5 when the voltages of the COP and DOP pins are high after the V5 voltage has been gradually increased starting at the initial status.

- **Overcurrent detection voltage 2 ( $V_{IOV2}$ )**

Overcurrent detection voltage 2 ( $V_{IOV2}$ ) is the voltage of V5 when the voltages of the COP and DOP pins are high within the minimum and maximum values of overcurrent detection time 2 ( $t_{IOV2}$ ) after the voltage of V5 was instantaneously increased (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.

- **Overcurrent detection voltage 3 ( $V_{IOV3}$ )**

Overcurrent detection voltage 3 ( $V_{IOV3}$ ) is the voltage of V5 when the voltages of the COP and DOP pins are high within the minimum and maximum values of overcurrent detection time 3 ( $t_{IOV3}$ ) after the voltage of V5 was instantaneously increased (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.



**3. Overcharge detection delay time, overdischarge detection delay time****(Test condition 3, test circuit 1)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP and DOP pins are low (this status is referred to as the initial status).

- **Overcharge detection delay time ( $t_{CU}$ )**

The overcharge detection delay time ( $t_{CU}$ ) is the time it takes for the voltage of the COP pin to change from low to high after the voltage of  $V1$  is instantaneously changed from overcharge detection voltage 1 ( $V_{CU1}$ ) – 0.2 V to overcharge detection voltage 1 ( $V_{CU1}$ ) + 0.2 V (within 10  $\mu\text{s}$ ) starting at the initial status.

- **Overdischarge detection delay time ( $t_{DL}$ )**

The overdischarge detection delay time ( $t_{DL}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of  $V1$  is instantaneously changed from overdischarge detection voltage 1 ( $V_{DL1}$ ) + 0.2 V to overdischarge detection voltage 1 ( $V_{DL1}$ ) – 0.2 V (within 10  $\mu\text{s}$ ) starting at the initial status.

**4. Overcurrent detection delay time****(Test condition 4, test circuit 1)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP and DOP pins are low (this status is referred to as the initial status).

- **Overcurrent detection delay time 1 ( $t_{IOV1}$ )**

Overcurrent detection delay time 1 ( $t_{IOV1}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of  $V5$  is instantaneously changed to 0.35 V (within 10  $\mu\text{s}$ ) starting at the initial status.

- **Overcurrent detection delay time 2 ( $t_{IOV2}$ )**

Overcurrent detection delay time 2 ( $t_{IOV2}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of  $V5$  is instantaneously changed to 0.7 V (within 10  $\mu\text{s}$ ) starting at the initial status.

- **Overcurrent detection delay time 3 ( $t_{IOV3}$ )**

Overcurrent detection delay time 3 ( $t_{IOV3}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of  $V5$  is instantaneously changed to 1.6 V (within 10  $\mu\text{s}$ ) starting at the initial status.

**5. Power consumption during operation, power consumption at power-down****(Test condition 5, test circuit 2)**

- **Power consumption during operation ( $I_{OPE}$ ), power consumption at power-down ( $I_{PDN}$ )**

The power consumption during operation ( $I_{OPE}$ ) is the current of the VSS pin ( $I_{SS}$ ) when  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $S1 = \text{ON}$ , and  $S2 = \text{OFF}$ .

The power consumption at power-down ( $I_{PDN}$ ) is the current of the VSS pin ( $I_{SS}$ ) when  $V1 = V2 = 1.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 1.5\text{ V}$  (S-8253B Series),  $S1 = \text{OFF}$ , and  $S2 = \text{ON}$ .

## **6. Resistance between VMP and VDD, resistance between VMP and VSS**

### **(Test condition 6, test circuit 2)**

Confirm that  $V1 = V2 = 3.5 \text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5 \text{ V}$  (S-8253B Series),  $S1 = \text{ON}$ , and  $S2 = \text{OFF}$  (this status is referred to as the initial status).

- **Resistance between VMP and VDD ( $R_{\text{VMD}}$ )**

The resistance between VMP and VDD ( $R_{\text{VMD}}$ ) is determined based on the current of the VMP pin ( $I_{\text{VMD}}$ ) after  $S1$  and  $S2$  are switched to OFF and ON, respectively, starting at the initial status.

S-8253A Series:  $R_{\text{VMD}} = (V1 + V2)/I_{\text{VMD}}$

S-8253B Series:  $R_{\text{VMD}} = (V1 + V2 + V3)/I_{\text{VMD}}$

- **Resistance between VMP and VSS ( $R_{\text{VMS}}$ )**

The resistance between VMP and VSS ( $R_{\text{VMS}}$ ) is determined based on the current of the VMP pin ( $I_{\text{VMS}}$ ) after  $V1 = V2 = 1.8 \text{ V}$  (S-8253A Series) or  $V1 = V2 = V3 = 1.8 \text{ V}$  (S-8253B Series) are set starting at the initial status.

S-8253A Series:  $R_{\text{VMS}} = (V1 + V2)/I_{\text{VMS}}$

S-8253B Series:  $R_{\text{VMS}} = (V1 + V2 + V3)/I_{\text{VMS}}$

## **7. CTL pin input voltage**

### **(Test condition 7, test circuit 1)**

Confirm that  $V1 = V2 = 3.5 \text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5 \text{ V}$  (S-8253B Series),  $V4 = 0 \text{ V}$ ,  $V5 = 0 \text{ V}$ , and the COP and DOP pins are low (this status is referred to as the initial status).

- **CTL pin input voltage (high) ( $V_{\text{CTLH}}$ )**

The CTL pin input voltage (high) ( $V_{\text{CTLH}}$ ) is the voltage of  $V4$  when the voltages of the COP and DOP pins are high after the voltage of  $V4$  has been gradually increased starting at the initial status.

Confirm that  $V1 = V2 = 3.5 \text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5 \text{ V}$  (S-8253B Series),  $V4 = 0 \text{ V}$ ,  $V5 = 0.35 \text{ V}$ , and the COP and DOP pins are high (this status is referred to as the initial status).

- **CTL pin input voltage (low) ( $V_{\text{CTLL}}$ )**

The CTL pin input voltage (low) ( $V_{\text{CTLL}}$ ) is the voltage of  $V4$  when the voltages of the COP and DOP pins are low after the voltage of  $V4$  has been gradually decreased starting at the initial status.

## **8. CTL pin current**

### **(Test condition 8, test circuit 3)**

- **CTL current (high) ( $I_{\text{CTLH}}$ ), CTL pin current (low) ( $I_{\text{CTLL}}$ )**

The CTL pin current (high) ( $I_{\text{CTLH}}$ ) is the current that flows through the CTL pin when  $V1 = V2 = 3.5 \text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5 \text{ V}$  (S-8253B Series), and  $S3 = \text{ON}$ ,  $S4 = \text{OFF}$ . The CTL current (low) ( $I_{\text{CTLL}}$ ) is the current that flows through the CTL pin when  $S3 = \text{OFF}$  and  $S4 = \text{ON}$  after that.

**9. VC1 pin current, VC2 pin current**

**(Test condition 9, test circuit 3)**

- **VC1 pin current ( $I_{VC1}$ ), VC2 pin current ( $I_{VC2}$ )**

The VC1 pin current ( $I_{VC1}$ ) is the current that flows through the VC1 pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series), and  $S3 = \text{OFF}$ ,  $S4 = \text{ON}$ . Similarly, the VC2 pin current ( $I_{VC2}$ ) is the current that flows through the VC2 pin under these conditions (S-8253B Series only).

**10. COP pin leakage current, COP pin sink current**

**(Test condition 10, test circuit 4)**

- **COP pin leakage current ( $I_{COH}$ ), COP pin sink current ( $I_{COL}$ )**

The COP pin leakage current ( $I_{COH}$ ) is the current that flows through the COP pin when  $V1 = V2 = 12\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 8\text{ V}$  (S-8253B Series),  $S6 = S7 = S8 = \text{OFF}$ , and  $S5 = \text{ON}$ .

The COP pin sink current ( $I_{COL}$ ) is the current that flows through the COP pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $V6 = 0.5\text{ V}$ ,  $S5 = S7 = S8 = \text{OFF}$ , and  $S6 = \text{ON}$ .

**11. DOP pin source current, DOP pin sink current**

**(Test condition 11, test circuit 4)**

- **DOP pin source current ( $I_{DOH}$ ), DOP pin sink current ( $I_{DOL}$ )**

The DOP pin source current ( $I_{DOH}$ ) is the current that flows through the DOP pin when  $V1 = V2 = 1.8\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 1.8\text{ V}$  (S-8253B Series),  $V7 = 0.5\text{ V}$ ,  $S5 = S6 = S8 = \text{OFF}$ , and  $S7 = \text{ON}$ .

The DOP pin sink current ( $I_{DOL}$ ) is the current that flows through the DOP pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253B Series),  $V8 = 0.5\text{ V}$ ,  $S5 = S6 = S7 = \text{OFF}$ , and  $S8 = \text{ON}$ .

**12. 0 V charge start battery charger voltage or 0 V charge inhibition battery voltage**

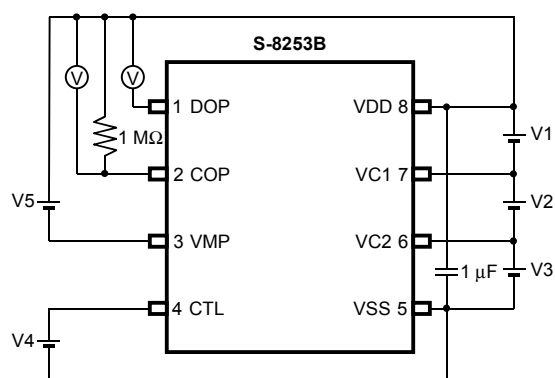
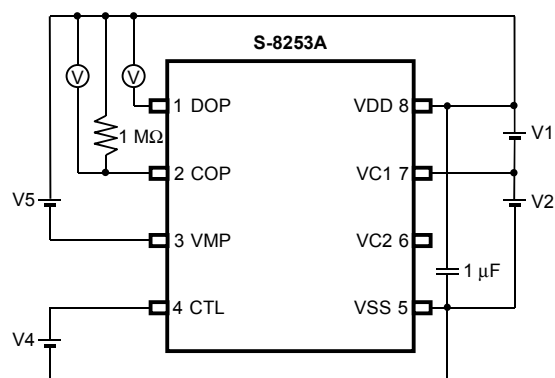
**(Test condition 12, test circuit 5)**

- **0 V charge start battery charger voltage ( $V_{0CHA}$ ): Products that available 0 V charge**

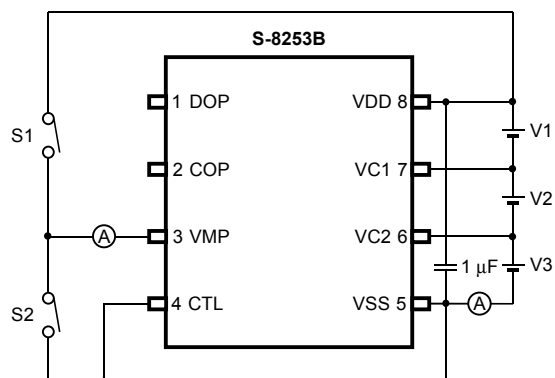
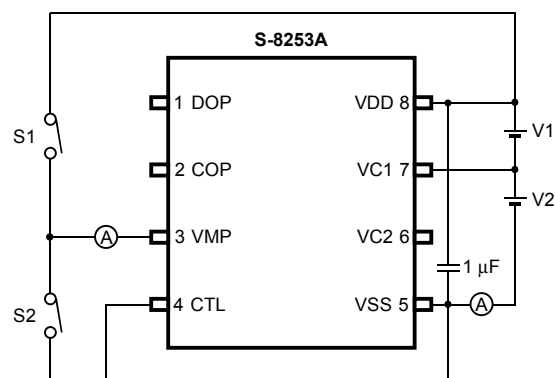
The COP pin voltage should be lower than  $V_{0CHA\text{ max.}} - 1\text{ V}$  when  $V1 = V2 = 0\text{ V}$  (S-8253A Series),  $V1 = V2 = V3 = 0\text{ V}$  (S-8253B Series), and  $V9 = V_{VMP} = V_{0CHA\text{ max.}}$ .

- **0 V charge inhibition battery voltage ( $V_{0INH}$ ): Products that unavailable 0 V charge**

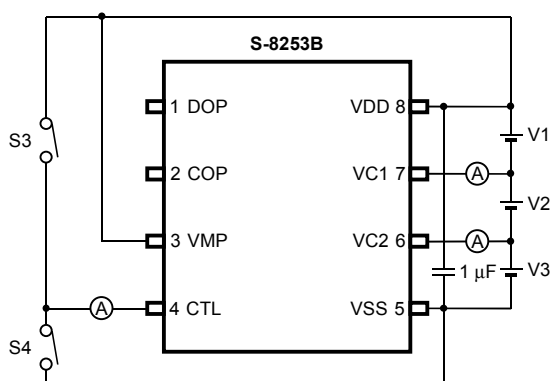
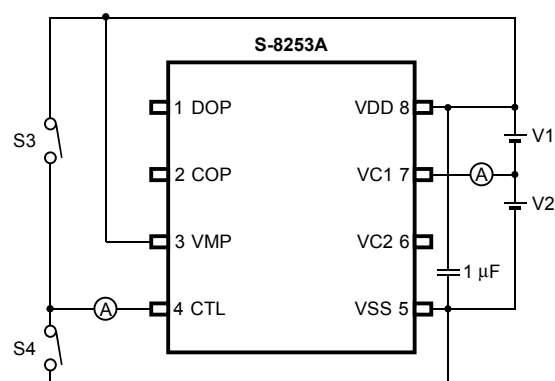
The COP pin voltage should be higher than  $V_{VMP} - 1\text{ V}$  when  $V1 = V2 = V_{0INH\text{ min.}}$  (S-8253A Series),  $V1 = V2 = V3 = V_{0INH\text{ min.}}$  (S-8253B Series), and  $V9 = V_{VMP} = 24\text{ V}$ .



**Test Circuit 1**



**Test Circuit 2**



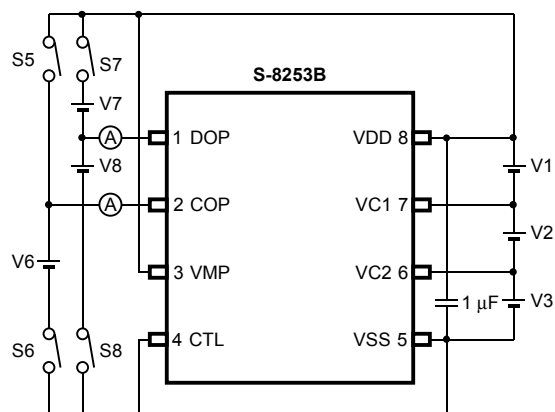
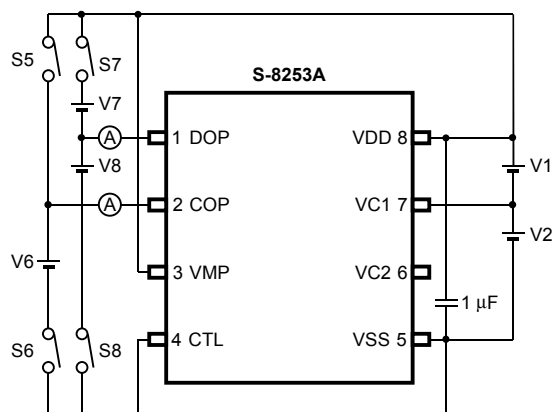
**Test Circuit 3**

**Figure 4 Test Circuit (1/2)**

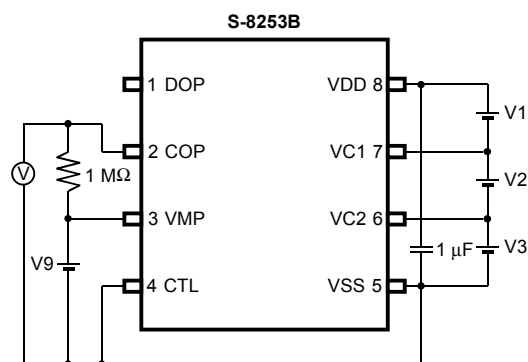
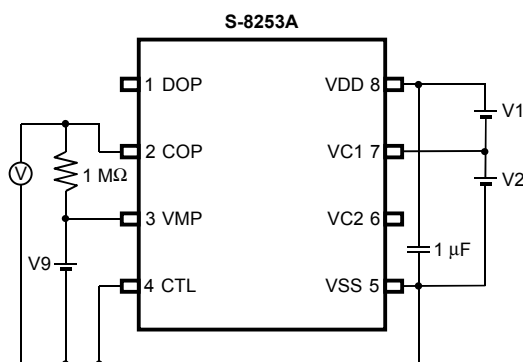
# BATTERY PROTECTION IC FOR 2-SERIAL OR 3-SERIAL-CELL PACK

## S-8253A/B Series

Rev.2.1\_00



Test Circuit 4



Test Circuit 5

Figure 4 Test Circuit (2/2)

## ■ Description of Operation

**Remark** Refer to “ ■ Standard Circuit “.

### 1. Normal status

When all of the battery voltages are in the range from  $V_{DLn}$  to  $V_{CUn}$  and the discharge current is lower than the specified value (the VMP pin voltage is higher than  $V_{DD} - V_{IOV1}$ ), the charging and discharging FETs are turned on.

**Caution** When the battery is connected for the first time, discharging may not be enabled. In this case, short the VMP and VDD pins or connect the charger to restore the normal status.

### 2. Overcharge status

When any one of the battery voltages becomes higher than  $V_{CUn}$  and the state continues for  $t_{CU}$  or longer, the COP pin becomes high impedance. Because the COP pin is pulled up to the EB+ pin voltage by an external resistor, the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

- a) All battery voltages become  $V_{CLn}$  or lower.
- b) All of the battery voltages are  $V_{CUn}$  or lower, and the VMP pin voltage is  $V_{DD} - V_{IOV1}$  or lower (Since the discharge current flows through the body diode of the charging FET immediately after discharging is started when the charger is removed and a load is connected, the VMP pin voltage momentarily decreases by approximately 0.6 V from the VDD pin voltage. The IC detects this voltage and releases the overcharging status.)

### 3. Overdischarge status

When any one of the battery voltages becomes lower than  $V_{DLn}$  and the state continues for  $t_{DL}$  or longer, the DOP pin voltage becomes  $V_{DD}$  level, and the discharging FET is turned off to stop discharging. This is called the overdischarging status. After discharging is stopped due to the overdischarge status, the S-8253A/B Series enters the power-down status.

### 4. Power-down status

When discharging has stopped due to the overdischarge status, the VMP pin is pulled down to the  $V_{SS}$  level by the RVSM resistor. When the VMP pin voltage is lower than  $V_{DD}/2$ , the S-8253A/B Series enters the power-down status. In the power-down status, almost all the circuits of the S-8253A/B Series stop and the current consumption is  $I_{PDN}$  or lower. The conditions of each output pin are as follows.

- a) COP      Hi-Z
- b) DOP       $V_{DD}$

The power-down status is released when the following condition holds.

- a) The VMP pin voltage is  $V_{DD}/2$  or higher. (A charger is connected.)

The overdischarging status is released when the following condition holds.

- a) All of the battery voltages are  $V_{DLn}$  or higher, and the VDD pin voltage is  $V_{DD}/2$  or higher. (A charger is connected.)

**5. Overcurrent status**

The S-8253A/B Series has three overcurrent detection levels ( $V_{IOV1}$ ,  $V_{IOV2}$ , and  $V_{IOV3}$ ) and three overcurrent detection delay times ( $t_{IOV1}$ ,  $t_{IOV2}$ , and  $t_{IOV3}$ ) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the difference of the voltages of the VMP and VDD pins is greater than  $V_{IOV1}$ ) and the state continues for  $t_{IOV1}$  or longer, the S-8253A/B Series enters the overcurrent status, in which the DOP pin voltage becomes  $V_{DD}$  level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the  $V_{DD}$  voltage by the internal resistor RVMD. Operation of overcurrent detection levels 2, 3 ( $V_{IOV2}$ ,  $V_{IOV3}$ ) and overcurrent detection delay times 2, 3 ( $t_{IOV2}$ ,  $t_{IOV3}$ ) are the same as for  $V_{IOV1}$  and  $t_{IOV1}$ .

The overcurrent status is released when the following condition holds.

- a) The VMP pin voltage is  $V_{DD} - V_{IOV1}$  or higher because a charger is connected or the load is released.

**Caution** The impedance that enables automatic restoration varies depending on the battery voltage and set value of overcurrent detection voltage 1.

**6. 0 V battery charge function**

Regarding the charging of a self-discharged battery (0 V battery), the S-8253A/B Series has two functions from which one should be selected.

- a) 0 V battery charging is allowed (0 V battery charging is available)  
When the charger voltage is higher than  $V_{0CHA}$ , the 0 V battery can be charged.
- b) 0 V battery charging is prohibited (0 V battery charging is unavailable)  
When one of the battery voltages is lower than  $V_{0INH}$ , the 0 V battery cannot be charged.

**Caution** When the VDD pin voltage is lower than the minimum value of  $V_{DSOP}$ , the operation of the S-8253A/B Series is not guaranteed.

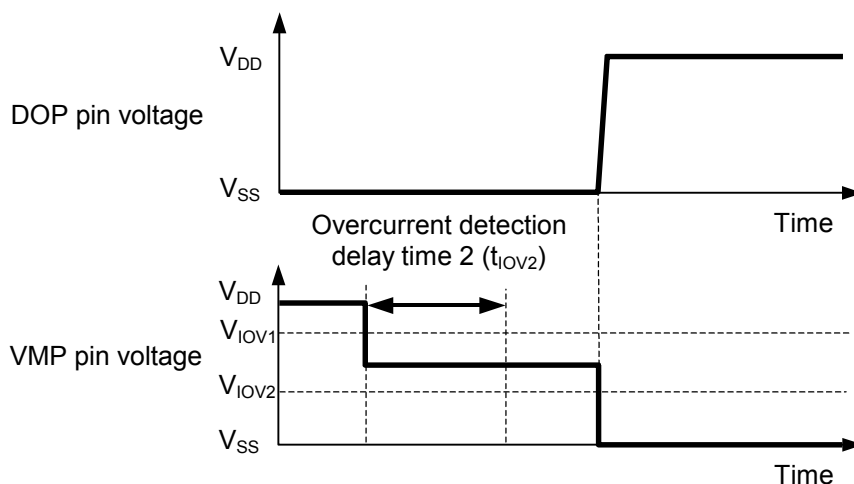
## 7. Delay circuit

The following detection delay times are determined by dividing a clock of approximately 3.57 kHz by the counter.

(Example)

Oscillator clock cycle ( $T_{CLK}$ ): 280  $\mu$ s  
 Overcharge detection delay time ( $t_{CU}$ ): 1.15 s  
 Overdischarge detection delay time ( $t_{DL}$ ): 144 ms  
 Overcurrent detection delay time 1 ( $t_{IOV1}$ ): 9 ms  
 Overcurrent detection delay time 2 ( $t_{IOV2}$ ): 4.5 ms

**Caution** The overcurrent detection delay time 2 ( $t_{IOV2}$ ) and overcurrent detection delay time 3 ( $t_{IOV3}$ ) start when the overcurrent detection voltage 1 ( $V_{IOV1}$ ) is detected. As soon as the overcurrent detection voltage 2 ( $V_{IOV2}$ ) or overcurrent detection voltage 3 ( $V_{IOV3}$ ) is detected over the detection delay time for overcurrent 2 ( $t_{IOV2}$ ) or overcurrent 3 ( $t_{IOV3}$ ) after the detection of overcurrent 1, the S-8253A/B turns the discharging control FET off.



## 8. CTL pin

The S-8253A/B Series has a control pin for charge/discharge control and reducing test time. The levels, “L”, “H”, and “M”, of the voltage input to the CTL pin determine the status of the S-8253A/B Series: normal operation, charge/discharge inhibition, or test time reduction. The CTL pin takes precedence over the battery protection circuit. During normal use, short the CTL and VSS pins.

**Table 7 Conditions Set by CTL Pin**

CTL Pin Potential	Status of IC	COP Pin	DOP Pin
Open	Charge/discharge inhibited status	Hi-Z	$V_{DD}$
High ( $V_{CTL} \geq V_{CTLH}$ )	Charge/discharge inhibited status	Hi-Z	$V_{DD}$
Middle ( $V_{CTLL} < V_{CTL} < V_{CTLH}$ )	Delay time reduced status <sup>*1</sup>	(*2)	(*2)
Low ( $V_{CTLL} \geq V_{CTL}$ )	Normal status	(*2)	(*2)

<sup>\*1</sup>. In the delay time reduced status, delay times are reduced in 1/60 to 1/30 scale.

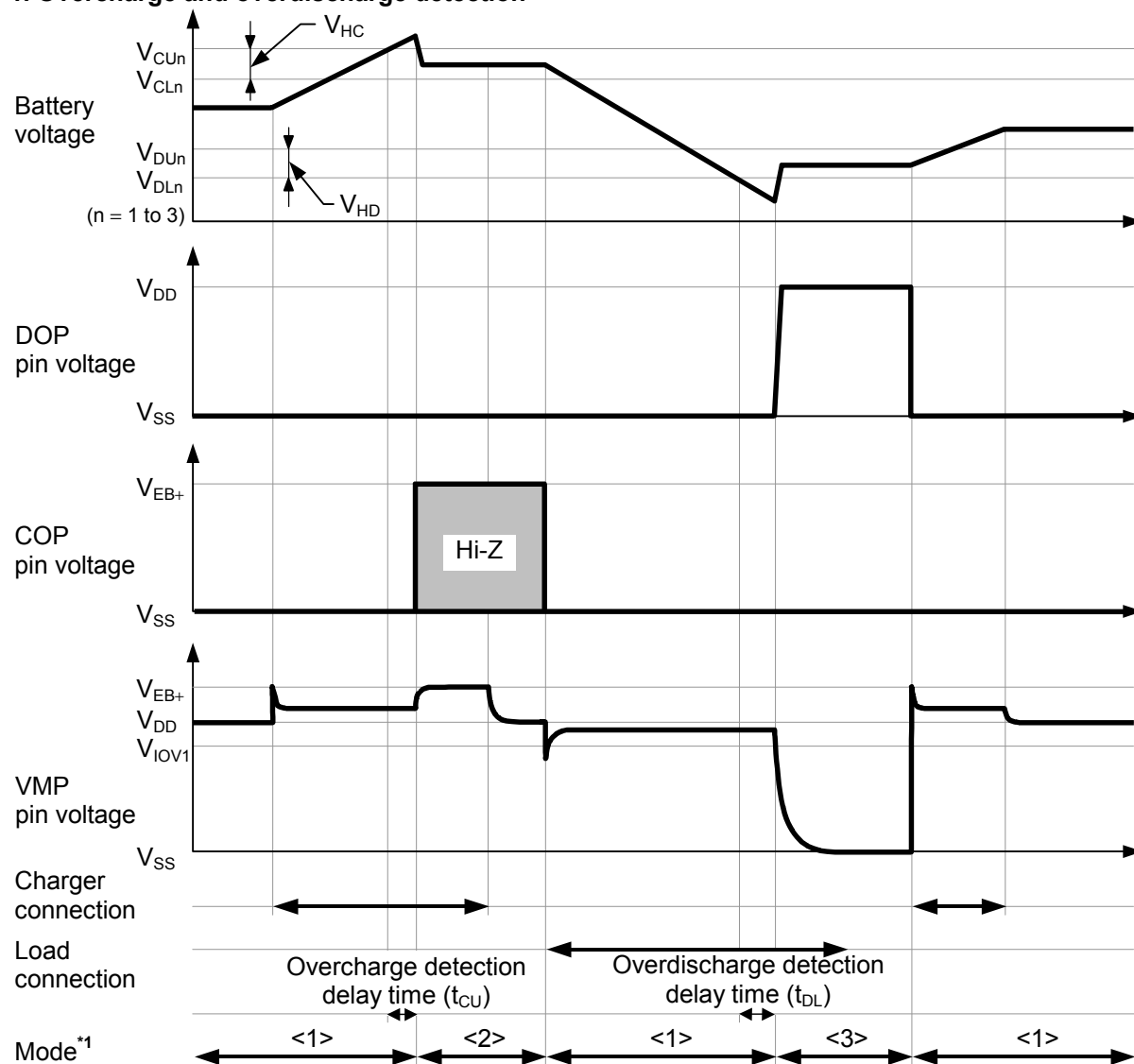
<sup>\*2</sup>. The pin status is controlled by the voltage detection circuit.

- Caution1.** If the potential of the CTL pin is middle, overcurrent detection voltage 1 ( $V_{IOV1}$ ) does not operate.
- 2.** If you use the middle potential of the CTL pin, contact our sales office.



## ■ Operation Timing Chart

### 1. Overcharge and overdischarge detection

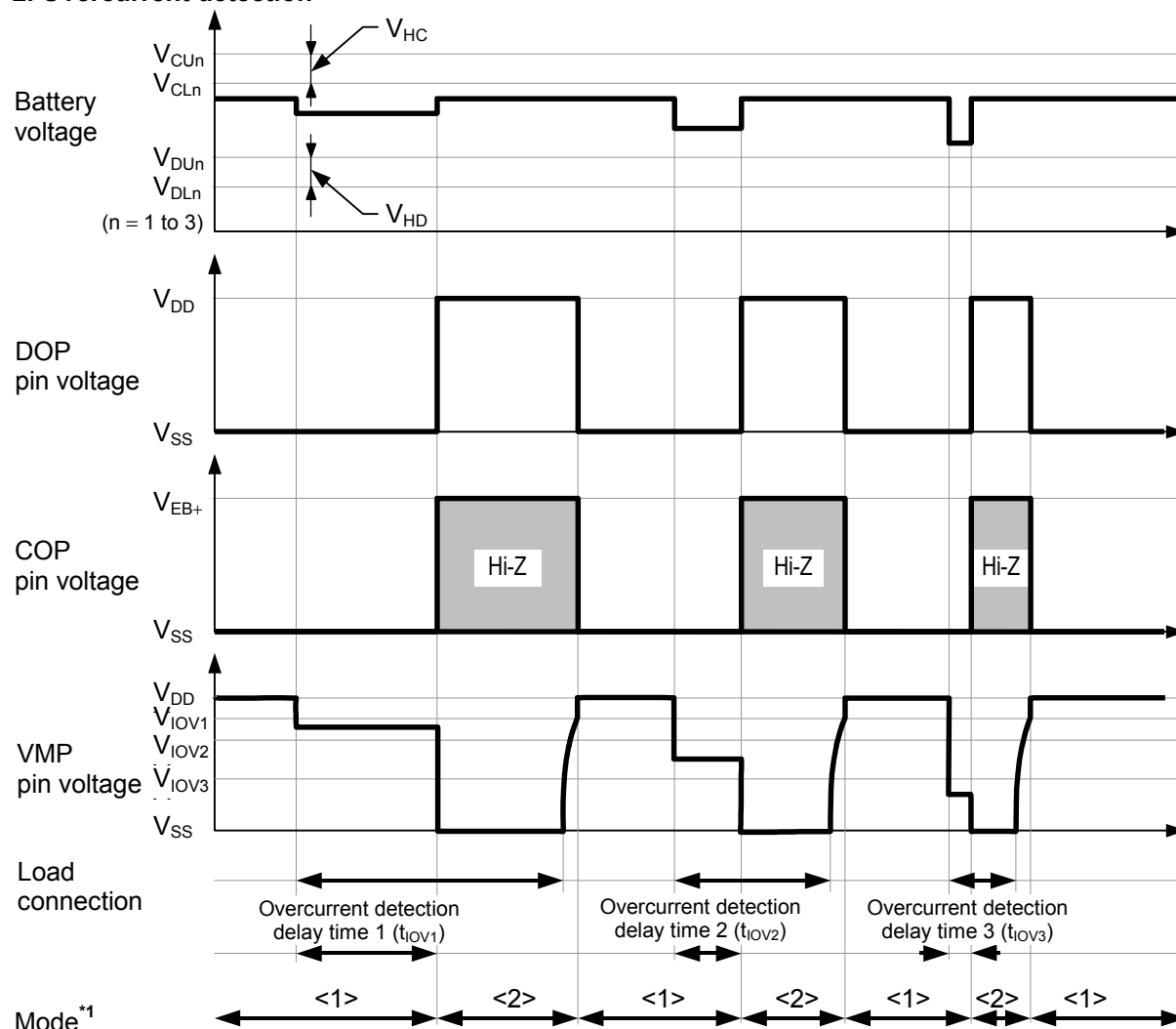


- \*1. <1>: Normal mode  
 <2>: Overcharge mode  
 <3>: Overdischarge mode

**Remark** The charger is assumed to charge with a constant current.  $V_{EB+}$  indicates the open voltage of the charger.

Figure 5

## 2. Overcurrent detection



\*1.  $<1>$ : Normal mode  
 $<2>$ : Overcurrent mode

**Remark** The charger is assumed to charge with a constant current.  $V_{EB+}$  indicates the open voltage of the charger.

**Figure 6**

## ■ Standard Circuit

### (1) S-8253A Series

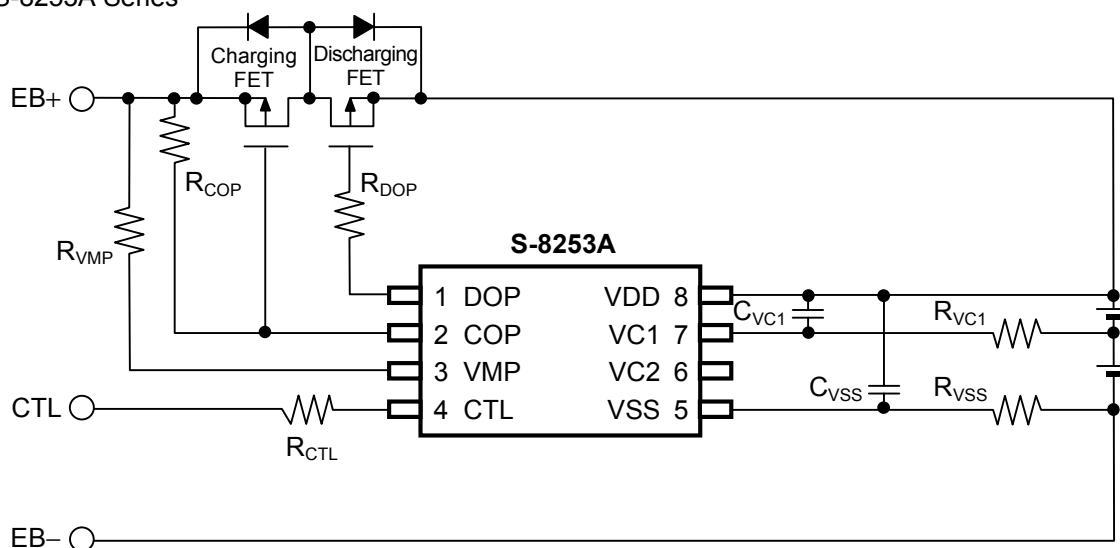


Figure 7

### (2) S-8253B Series

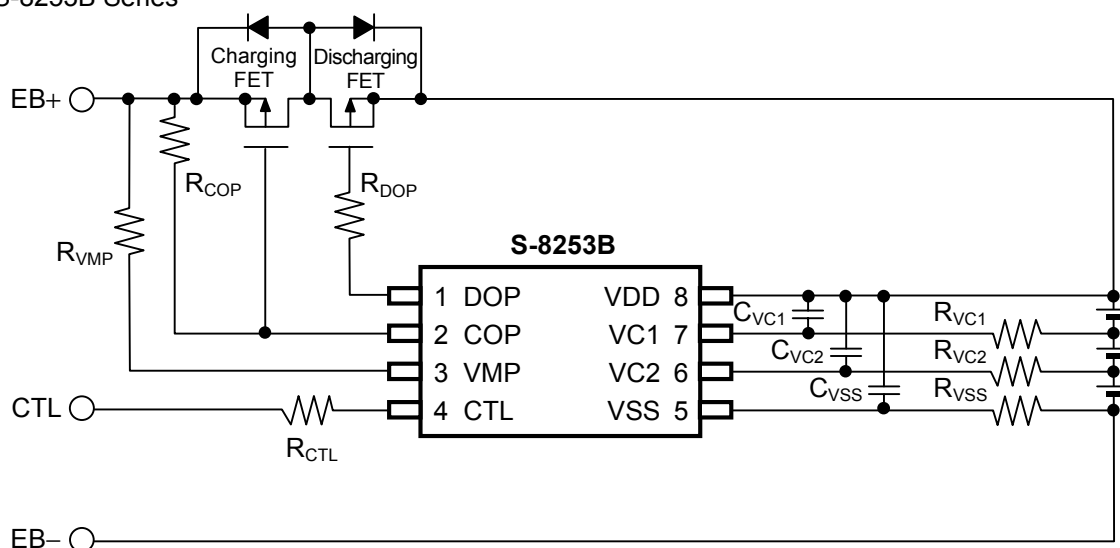


Figure 8

**Table 8 Recommended Value for External Parts**

No.	Symbol	Recommended Value	Range	Unit
1	$R_{VC1}$	1	0 to 1	$k\Omega$
2	$R_{VC2}$	1	0 to 1	$k\Omega$
3	$R_{DOP}$	5.1	2 to 10	$k\Omega$
4	$R_{COP}$	1	0.1 to 1	$M\Omega$
5	$R_{VMP}$	5.1	1 to 10	$k\Omega$
6	$R_{CTL}$	0	0 to 100	$k\Omega$
7	$R_{VSS}$	0	0 to 51	$\Omega$
8	$C_{VC1}$	0.1	0 to 0.33	$\mu F$
9	$C_{VC2}$	0.1	0 to 0.33	$\mu F$
10	$C_{VSS}$	1	0 to 10	$\mu F$

**Caution** The standard circuit above does not guarantee proper operation.  
Evaluation in the actual application is needed to determine the correct constants.

## ■ Precautions

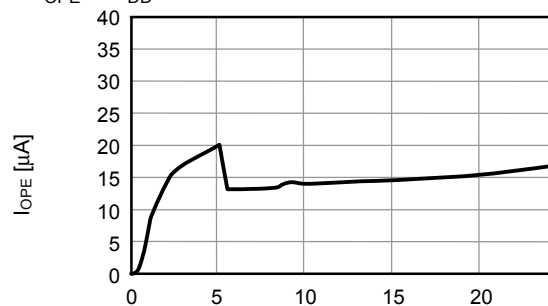
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP and VDD pins or connect the battery charger to return to the normal mode.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Characteristics (Typical Data)

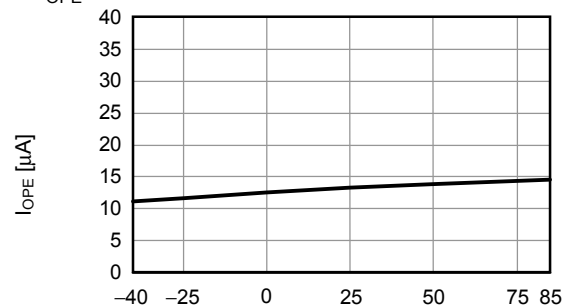
(1) Current consumption

(a) S-8253AAA

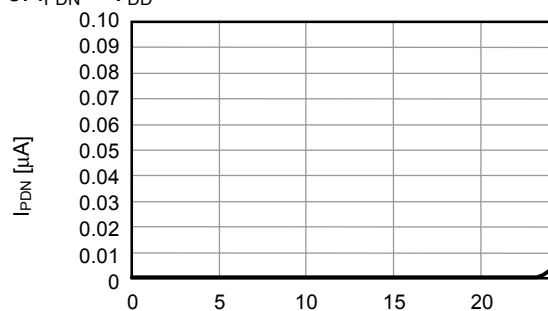
1.  $I_{OPE} - V_{DD}$



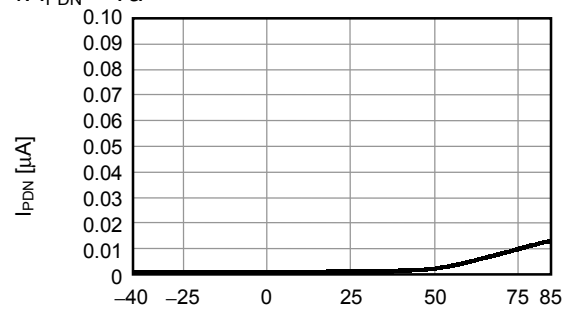
2.  $I_{OPE} - T_a$



3.  $I_{PDN} - V_{DD}$

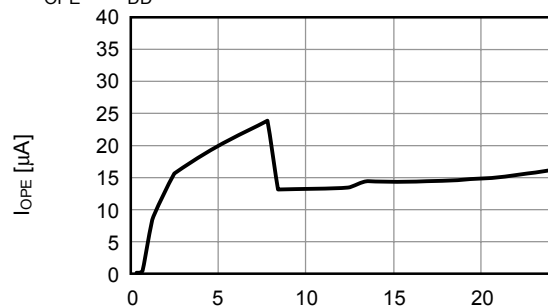


4.  $I_{PDN} - T_a$

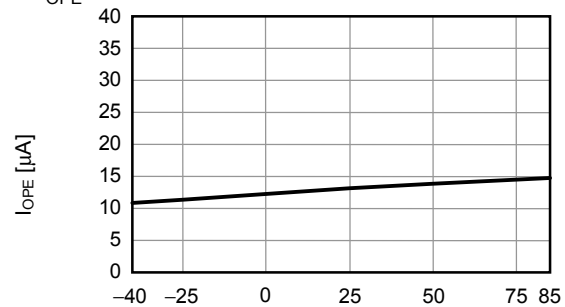


(b) S-8253BAA

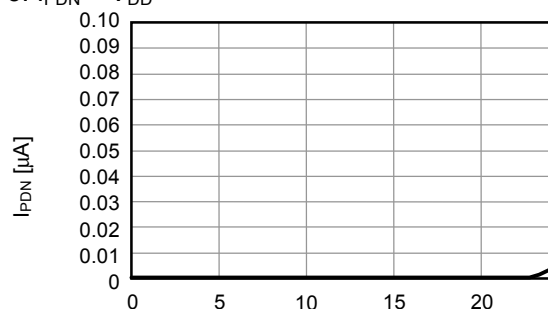
1.  $I_{OPE} - V_{DD}$



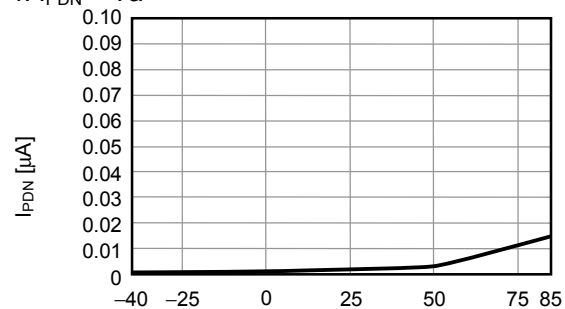
2.  $I_{OPE} - T_a$



3.  $I_{PDN} - V_{DD}$



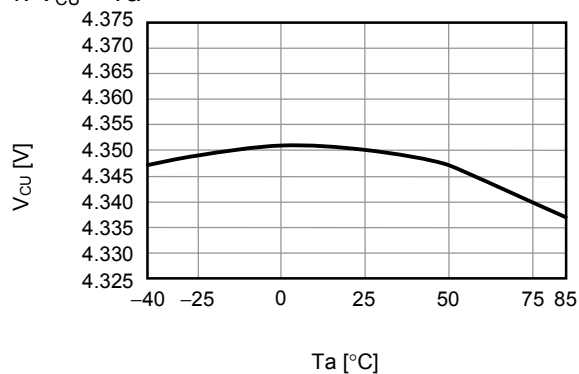
4.  $I_{PDN} - T_a$



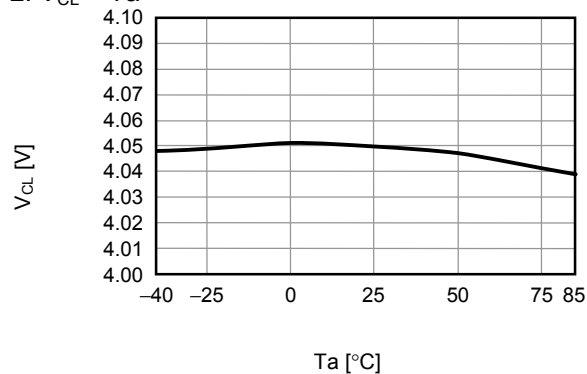
(2) Overcharge detection/release voltage, overdischarge detection/release voltage, overcurrent detection voltage, and delay times

S-8253AAA, S-8253BAA

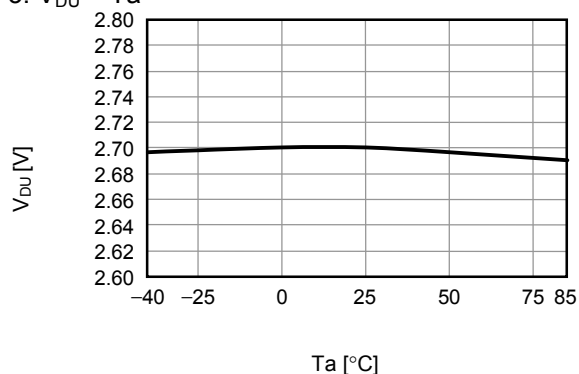
1.  $V_{CU} - T_a$



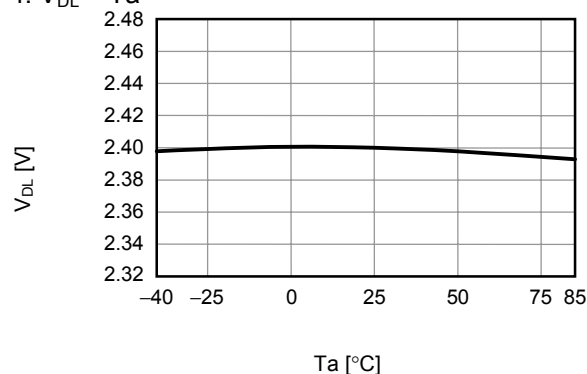
2.  $V_{CL} - T_a$



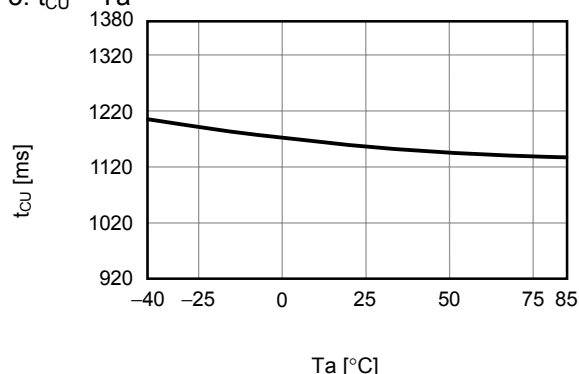
3.  $V_{DU} - T_a$



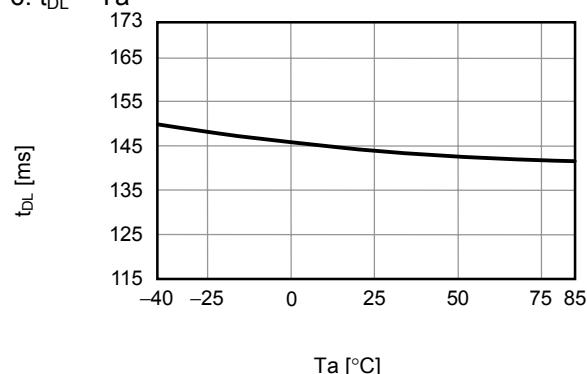
4.  $V_{DL} - T_a$



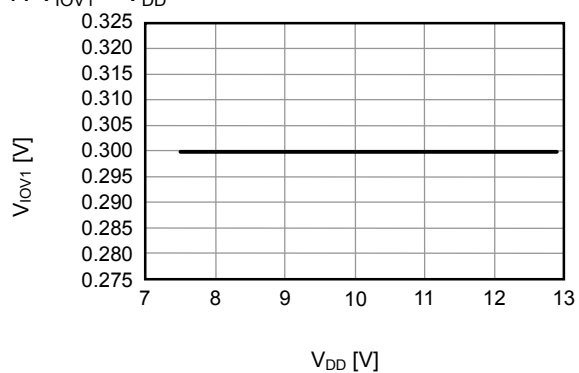
5.  $t_{CU} - T_a$



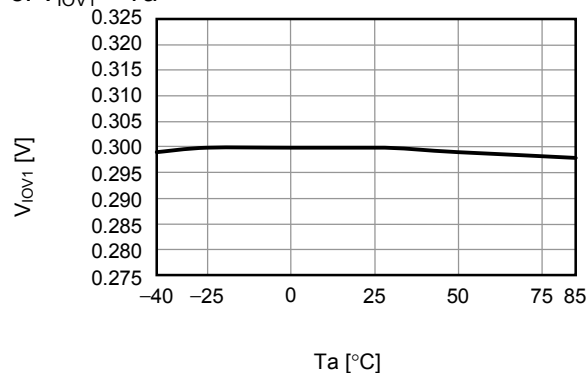
6.  $t_{DL} - T_a$



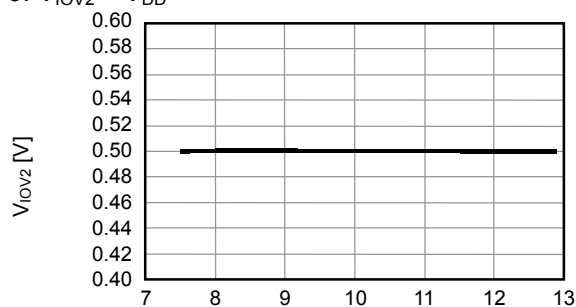
7.  $V_{IOV1} - V_{DD}$



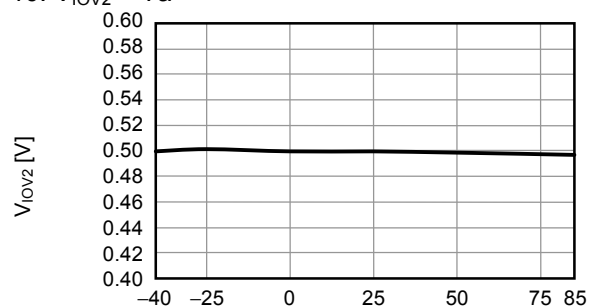
8.  $V_{IOV1} - T_a$



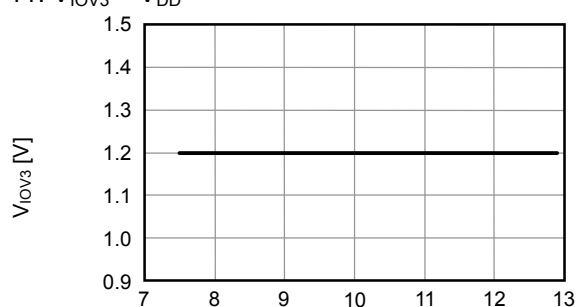
9.  $V_{IOV2} - V_{DD}$



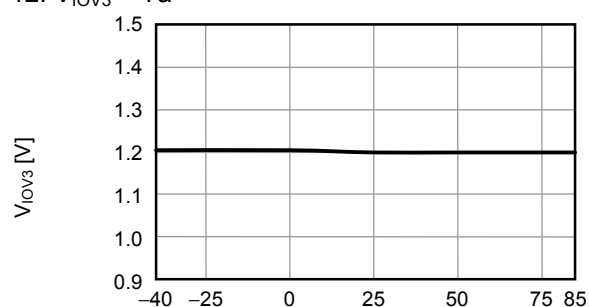
10.  $V_{IOV2} - T_a$



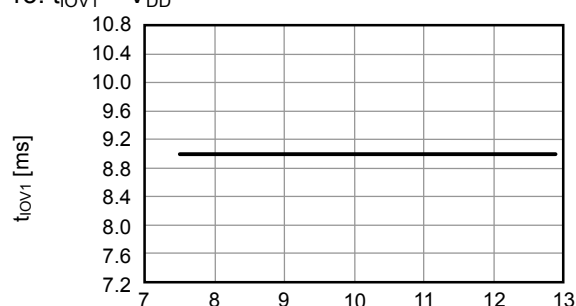
11.  $V_{IOV3} - V_{DD}$



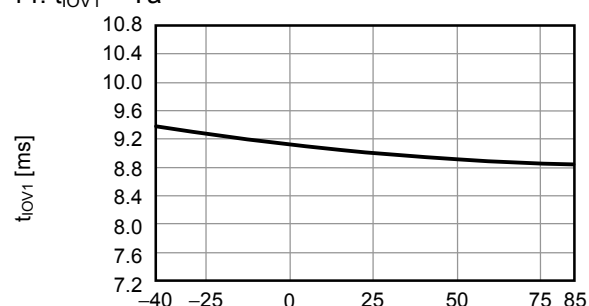
12.  $V_{IOV3} - T_a$



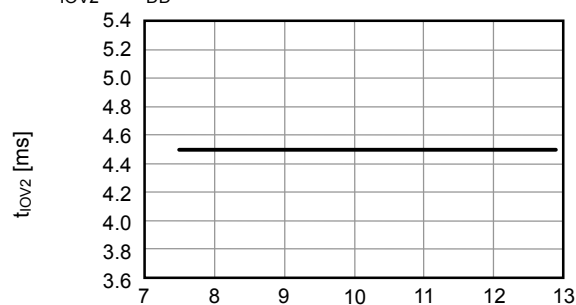
13.  $t_{IOV1} - V_{DD}$



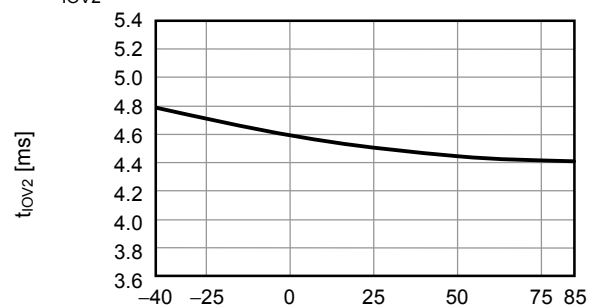
14.  $t_{IOV1} - T_a$



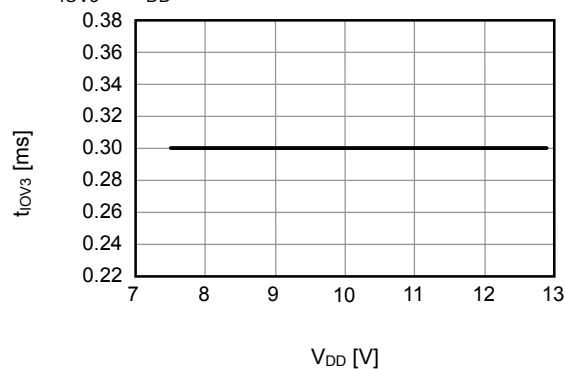
15.  $t_{IOV2} - V_{DD}$



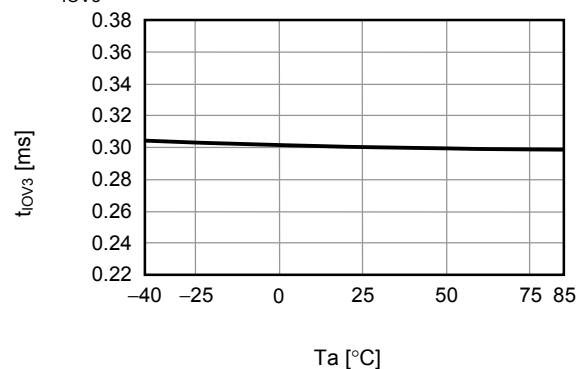
16.  $t_{IOV2} - T_a$



17.  $t_{IOV3} - V_{DD}$

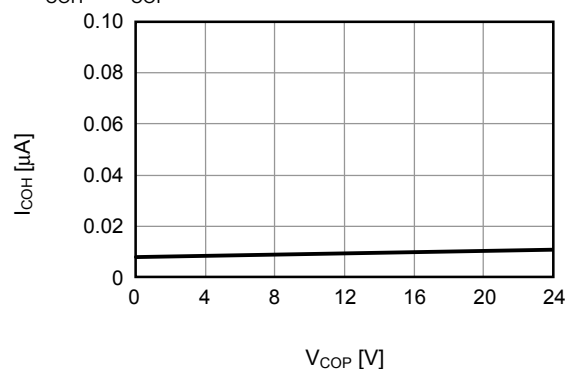


18.  $t_{IOV3} - T_a$

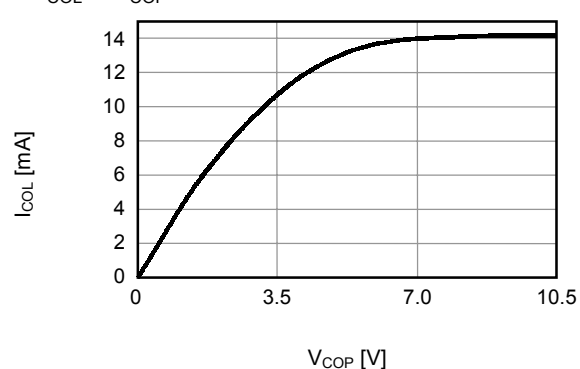


(3) COP/DOP pin  
S-8253AAA, S-8253BAA

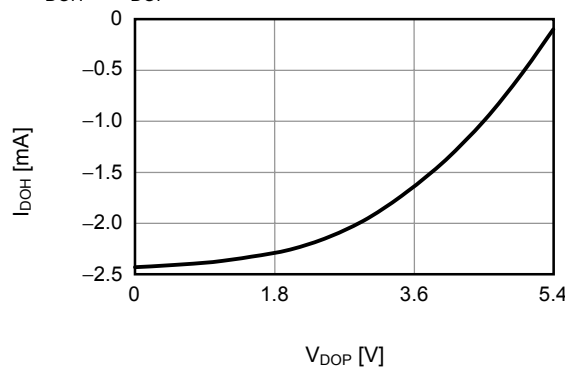
1.  $I_{COH} - V_{COP}$



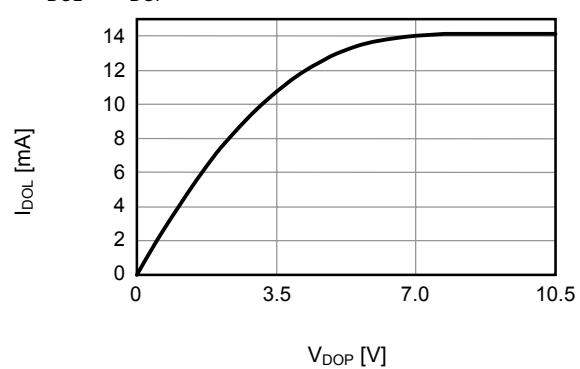
2.  $I_{COL} - V_{COP}$



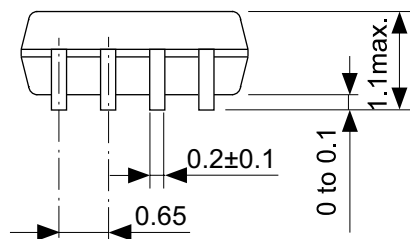
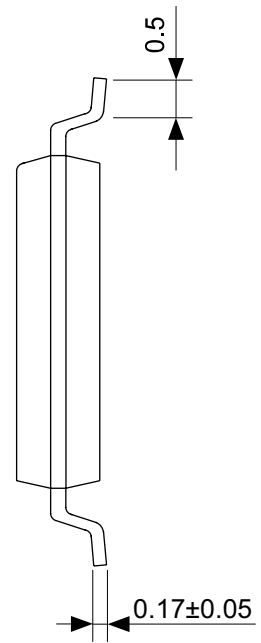
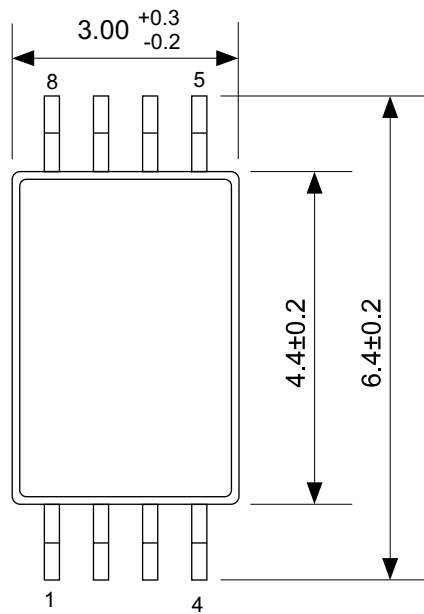
3.  $I_{DOH} - V_{DOP}$



4.  $I_{DOL} - V_{DOP}$

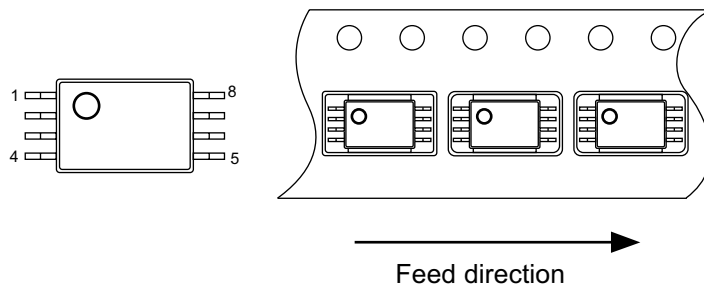
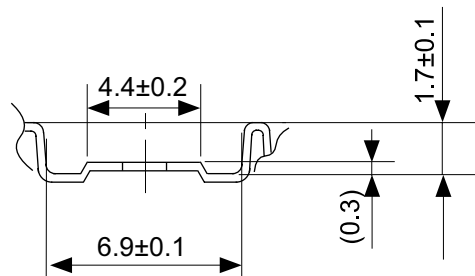
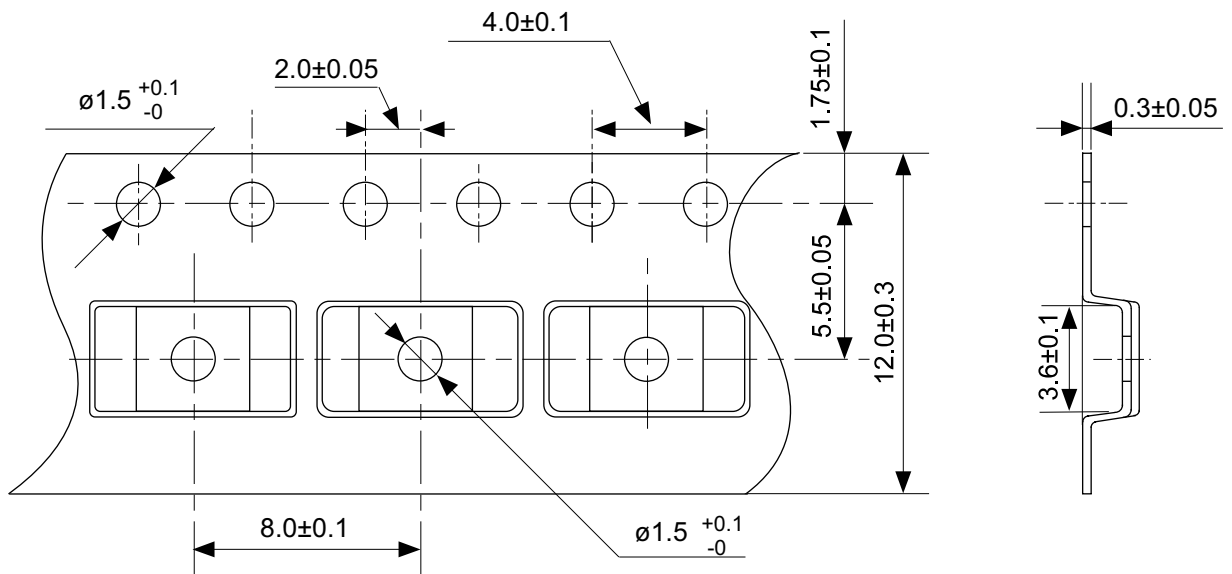






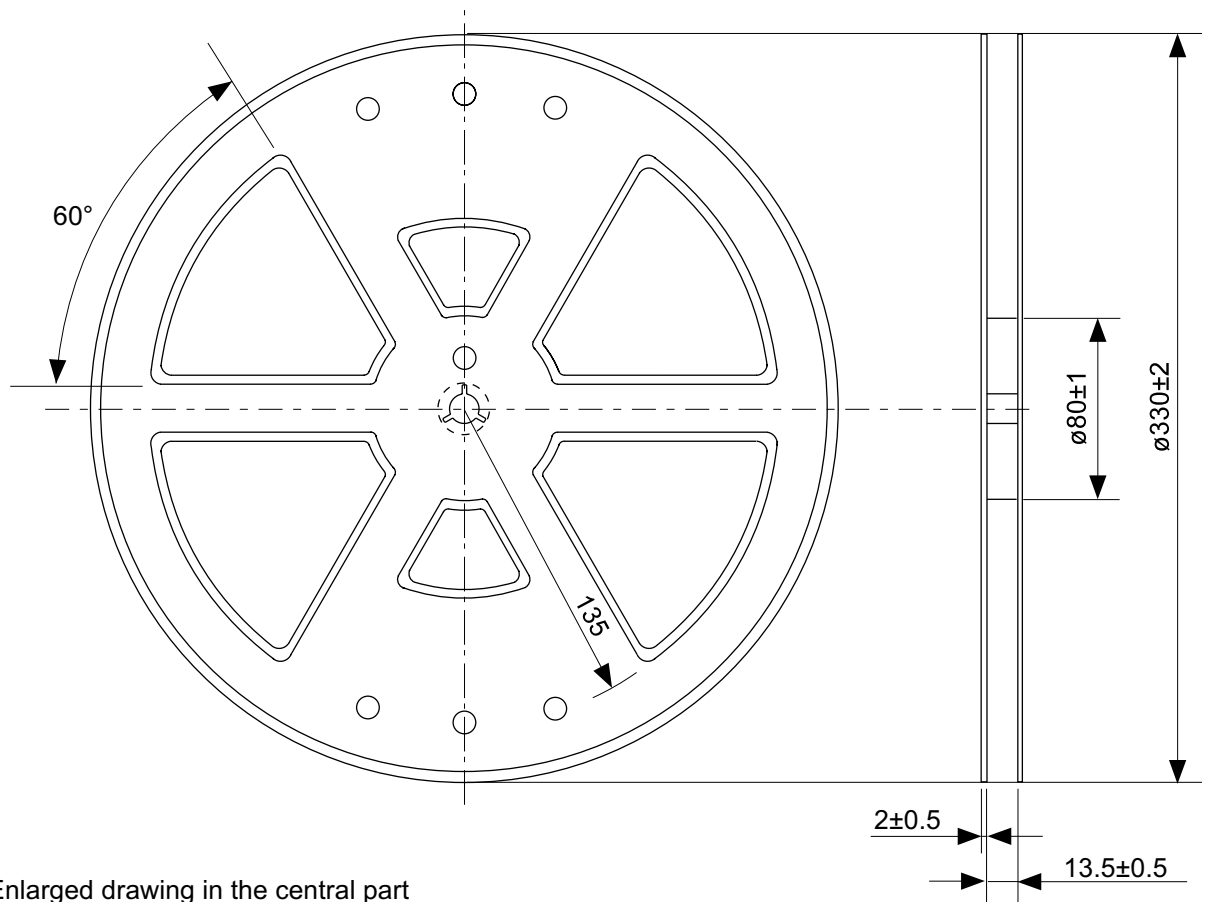
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UNIT	mm
Seiko Instruments Inc.	

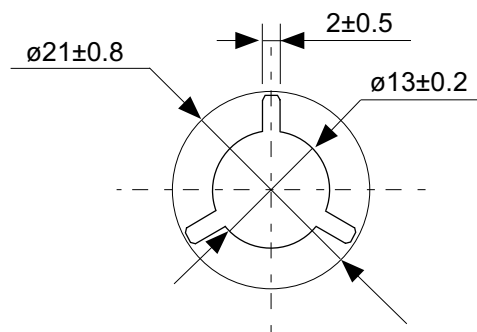


No. FT008-D-C-SD-1.0

TITLE	TSSOP8-D-Carrier Tape
No.	FT008-D-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-D-R-SD-1.0

TITLE	TSSOP8-D-Reel		
No.	FT008-D-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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