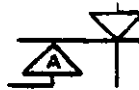


High Power 77 mm THYRISTORS

C781
C782 / C785
C784 / C787

$$I_{T(AV)} = 1650 - 2500A / V_{DRM}, V_{RRM} = 1800V - 4400V$$

AMPLIFYING GATE



The C781, C782, & C784 group of reverse blocking thyristors feature a nominal 77mm silicon junction design having an exclusive linear amplifying gate. These are manufactured by the proven multi-diffusion process to optimize high blocking voltage capability with low on state voltage and recovery characteristics.

These are commonly used for phase controlled applications such as DC motor control power supplies, cycloconverters and load commutated inverters.



THYRISTOR (SCR) PRESSPAK

See package styles on page 8
height
1.0 inch C785, C787
1.4 inch C781, C782, C784

MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE V_{DRM}/V_{RRM}^1 $T_J = -40^\circ C$ to $+125^\circ C$	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE V_{DRM}/V_{RRM}^1 $T_J = 0^\circ C$ to $+125^\circ C$	V_{TM}^2 @ 2 KA $T_J = 125^\circ C$	I_{TSM}^3	I_{AV}^4 $T_C = 70^\circ C$
				8.3ms/10ms	
C784DD	4400 Volts	4500 Volts	1.85 V	26KA/24KA	1650A
C784DC	4300	4400			
C784DB	4200	4300			
C784DA	4100	4200			
C784DP	4000	4100			
C784CT	3900	4000			
C784CN	3800	3900			
C784CS	3700	3800			
C784CM	3600	3700			
C782LS	2700	2800	1.35V	35KA/32KA	2300A
C782LM	2600	2700			
C782LE	2500	2600			
C782LD	2400	2500			
C781LA	2100 Volt	2200 Volt	1.20V	45KA/41.5KA	2500A
C781L	2000	2100			
C781PT	1900	2000			
C781PN	1800	1900			

Externally applied mounting force..... 7000-9000 lb. 31.1-40.0 KN

DC Thermal Resistance Junction to case, R_{thj-c} $0.012^\circ C/W$

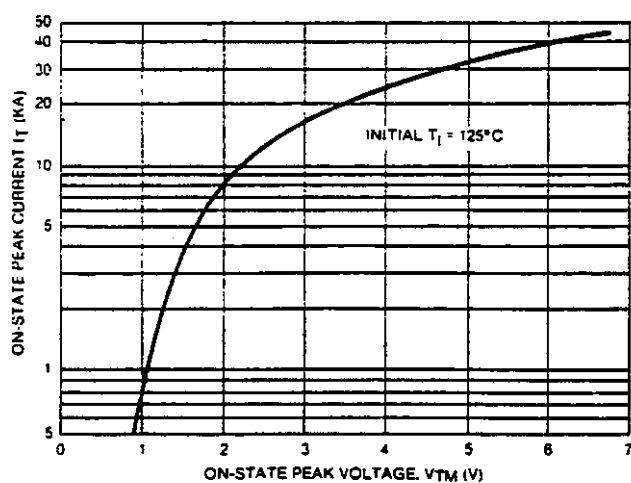
Storage Temperature -40° to $+150^\circ C$

NOTES:

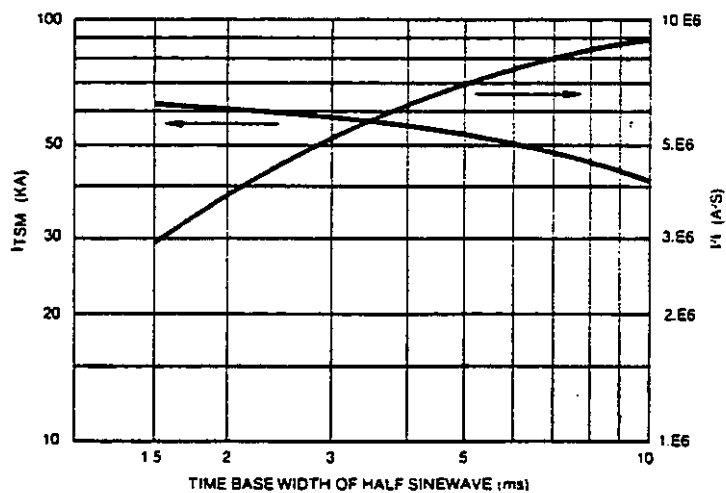
1. Sinusoidal waveform 50/60Hz. Device under test must be assembled with recommended mounting force to a heat dissipator at less than $0.3^\circ C/W$.
2. Instantaneous peak values, half sine (8.3 ms - 10 ms) or trapezoidal (30 A/ μs , ≤ 2.5 msec)
3. Non-repetitive surge current rating - crest of half sinewave.
4. Full cycle average current - continuous half sinewave @ 50/60Hz (see mounting instruction).

C781 CHARACTERISTICS

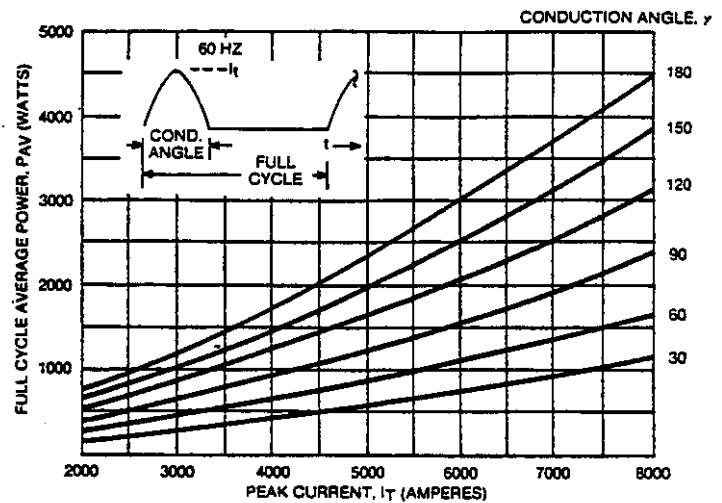
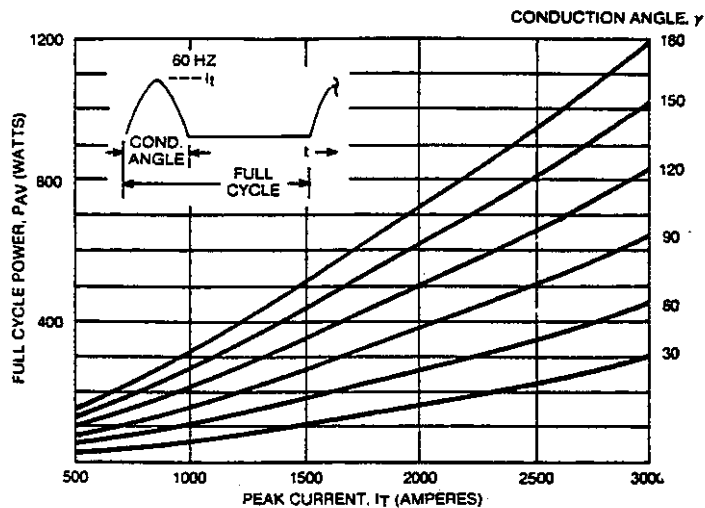
CHARACTERISTIC	SYMBOL	UNITS	MIN.	TYPE	MAX.	TEST CONDITIONS
Peak Off-state Current	I_{DRM} I_{DRM}	ma ma			10 150	$T_j = 25^\circ\text{C}$ Gate Opened $= 125^\circ\text{C}$ Gate Opened
Peak Reverse Current	I_{RRM} I_{RRM}	ma ma			10 150	$T_j = 25^\circ\text{C}$ Gate Opened $= 125^\circ\text{C}$ Gate Opened
Critical exponential rate of rise of off-state voltage (higher rates may cause destructive switching).	dv/dt	$\text{V}/\mu\text{s}$	500			$T_j = 125^\circ\text{C}$ $V_D = 0.8V_{DRM}$ open gate
Delay Time	t_d	μs	1.5	2.5	3.0	$T_j = 125^\circ\text{C}$, $V_D = 1500\text{V}$
Gate Trigger Current	I_{GT}	ma			250	$T_j = 25^\circ\text{C}$, $V_D = 12\text{V DC}$
Gate Trigger Voltage	V_{GT}	V			4.2	
Non-Trigger Current	I_{GDM}	ma	15			$T_j = 125^\circ\text{C}$, $V_D = 1000\text{V}$ AC Crest
Non-Trigger Voltage	V_{GDM}	V	0.5			
Operational Gate Current. Voltage requirement	I_{GA} V_{GA}	A V	1.1 13			Gate source: - open circuit - 30V - short circuit - 2A - rise time $\approx 0.5\mu\text{s}$ - duration $t_p > t_d$
Conventional Circuit Commutating Turn-off time (with reverse voltage)	t_q	μs		250	400	$T_j = 125^\circ\text{C}$, $I_T = 2000\text{ A}$ $t_p > 2\text{ms}$ $di/dt = 5\text{A}/\mu\text{s}$ $V_r = 100\text{V}$ $dv/dt = 1000\text{V}/\mu\text{s}$ V reapplied = 1000V
Holding Current	I_H	ma	40 24 20	60 36 30	150 90 75	$T_j = 25^\circ\text{C}$, $di/dt = -5\text{ma}/\mu\text{s}$ 105°C , $E_{rms} = 7.5\text{Vrms}$ 125°C , $R = 10\text{ ohms}$ Freq = 60Hz
Latching Current	I_L	ma	250 155 130	400 250 210	1000 620 530	$T_j = 25^\circ\text{C}$, Gate Drive 105°C , 30V 10 ohms 125°C , duration 15 μs



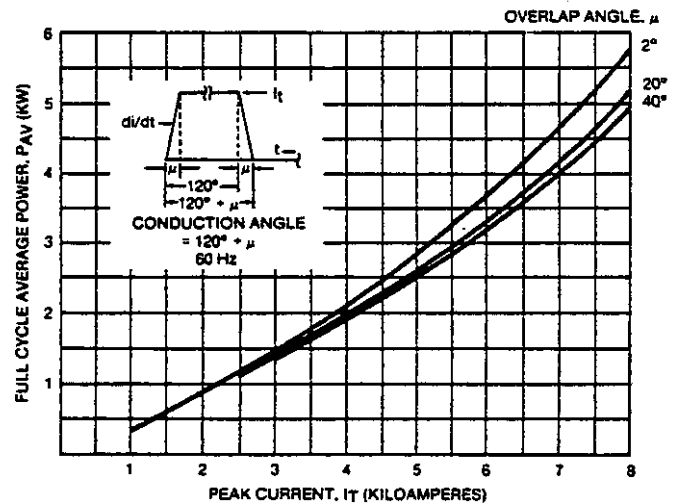
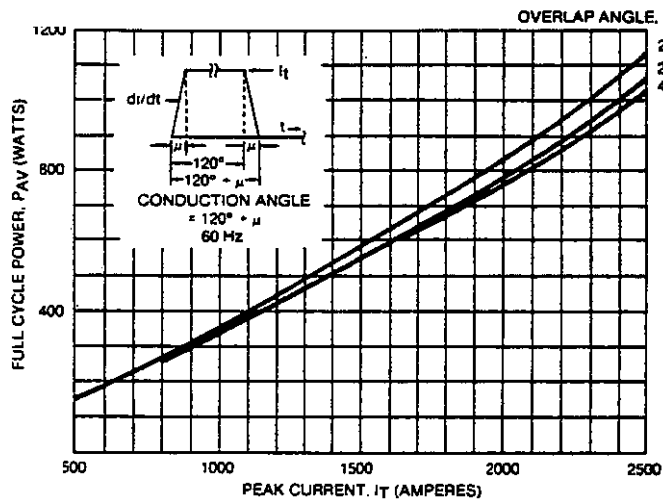
**MAXIMUM FORWARD CONDUCTION
CHARACTERISTIC ON-STATE**



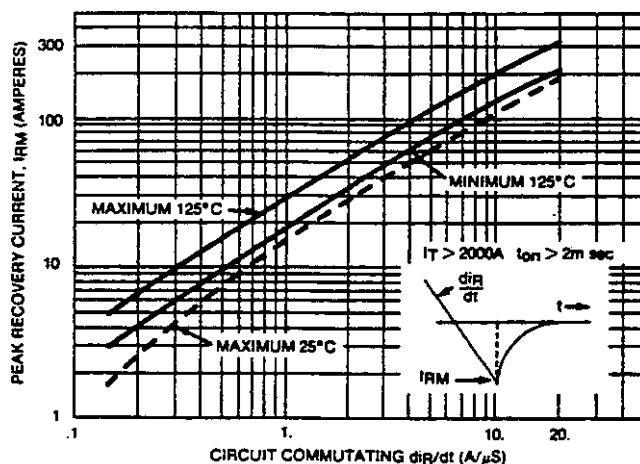
**NON-REPETITIVE I_{TSM} and I^2t CAPABILITY
FOR FUSE COORDINATION**



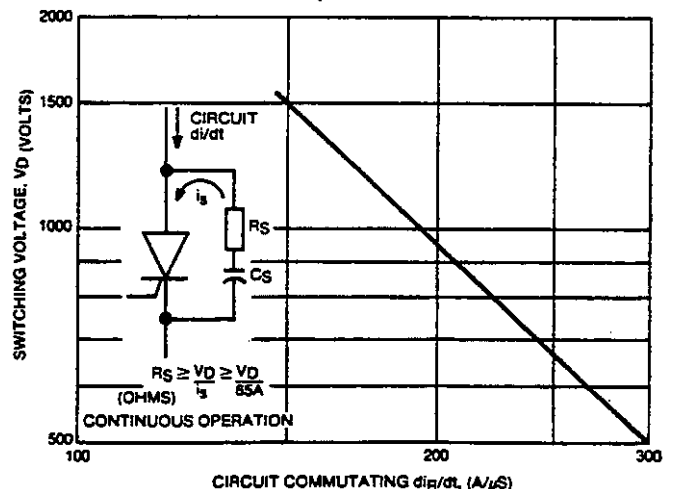
MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR SINEWAVE CURRENT AT VARIOUS CONDUCTING ANGLES. EFFECT OF VARIABLE CONDUCTING AREA IS INCLUDED. (DIGITAL DATA IS AVAILABLE)



MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR THREE PHASE RECTIFIER (120° CONDUCTION) AT SEVERAL OVERLAP ANGLES, " μ ". EFFECT OF VARIABLE CONDUCTING AREA IS INCLUDED. (DIGITAL DATA IS AVAILABLE)



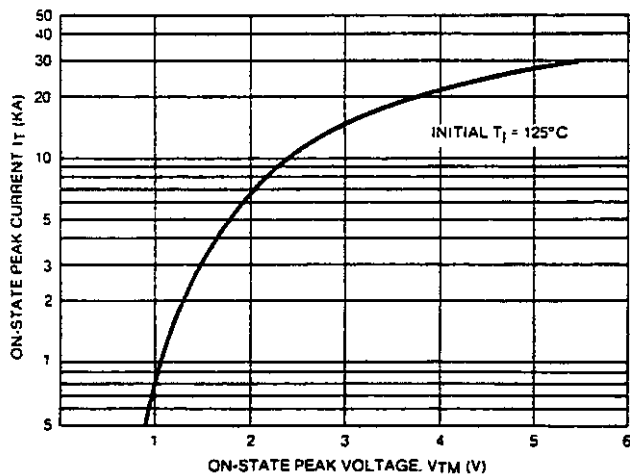
PEAK RECOVERY CURRENT VERSUS COMMUTATING CIRCUIT DI/DT



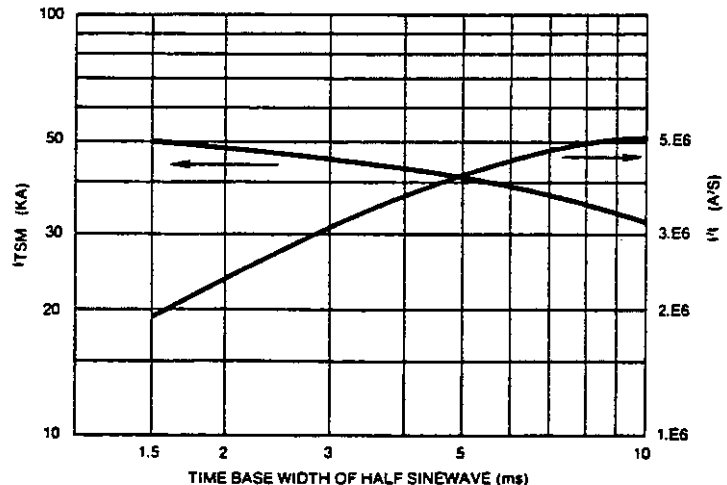
MAXIMUM ALLOWABLE REPETITIVE DI/DT AS FUNCTION OF ANODE VOLTAGE BIAS. LIMITATION ON ADDITIONAL SNUBBER DISCHARGE IS INDICATED.

C782 / C785 CHARACTERISTICS

CHARACTERISTIC	SYMBOL	UNITS	MIN.	TYPE	MAX.	TEST CONDITIONS
Peak Off-state Current	I_{DRM} I_{DRM}	ma ma			10 150	$T_j = 25^\circ\text{C}$ Gate Opened $= 125^\circ\text{C}$ Gate Opened
Peak Reverse Current	I_{RRM} I_{RRM}	ma ma			10 150	$T_j = 25^\circ\text{C}$ Gate Opened $= 125^\circ\text{C}$ Gate Opened
Critical exponential rate of rise of off-state voltage (higher rates may cause destructive switching).	dv/dt	$V/\mu s$	500			$T_j = 125^\circ\text{C}$, $V_D = 0.8V_{DRM}$ open gate
Delay Time	t_d	μs	1.5	2.5	3.0	$T_j = 125^\circ\text{C}$, $V_D = 1800V$
Gate Trigger Current	I_{GT}	ma			250	$T_j = 25^\circ\text{C}$, $V_D = 12V$ DC
Gate Trigger Voltage	V_{GT}	V			4.2	
Non-Trigger Current	I_{GDM}	ma	15			$T_j = 125^\circ\text{C}$, $V_D = 1300V$ AC Crest
Non-Trigger Voltage	V_{GDM}	V	0.5			
Operational Gate Current - Voltage requirement	I_{GA} V_{GA}	A V	1.1 13			Gate source: - open circuit - 30V - short circuit - 2A - rise time $\approx 0.5\mu s$ - duration $t_p > t_d$
Conventional Circuit Commutating Turn-off time (with reverse voltage)	t_q	μs		250	400	$T_j = 125^\circ\text{C}$, $I_T = 2000$ A $t_p > 2ms$ $di/dt = 5A/\mu s$ $V_r = 100V$ $dv/dt = 1000V/\mu s$ V reappplied = 1500V
Holding Current	I_H	ma	40 24 20	70 42 35	200 120 100	$T_j = 25^\circ\text{C}$, $di/dt = -.5ma/\mu s$ 105°C , $E_{rms} = 7.5V_{rms}$ 125°C , $R = 10$ ohms Freq = 60Hz
Latching Current	I_L	ma	300 210 190	600 420 375	1000 700 630	$T_j = 25^\circ\text{C}$, Gate Drive 105°C , 30V / 10 ohms 125°C , duration 15 μs



**MAXIMUM FORWARD CONDUCTION
CHARACTERISTIC ON-STATE**

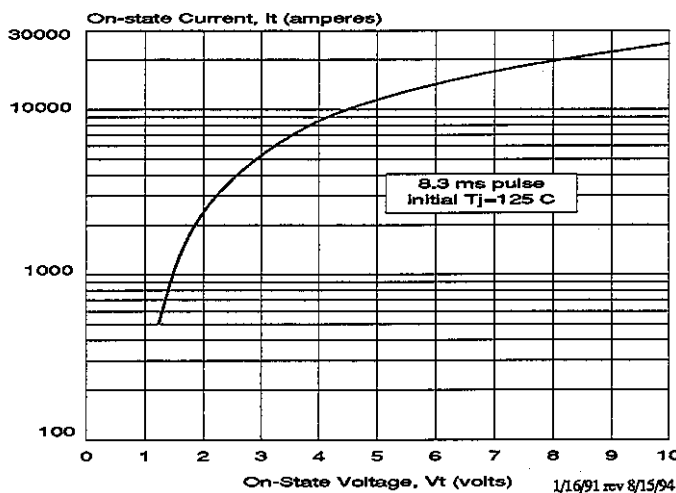


**NON-REPETITIVE I_{TSM} and I^2t CAPABILITY
FOR FUSE COORDINATION**

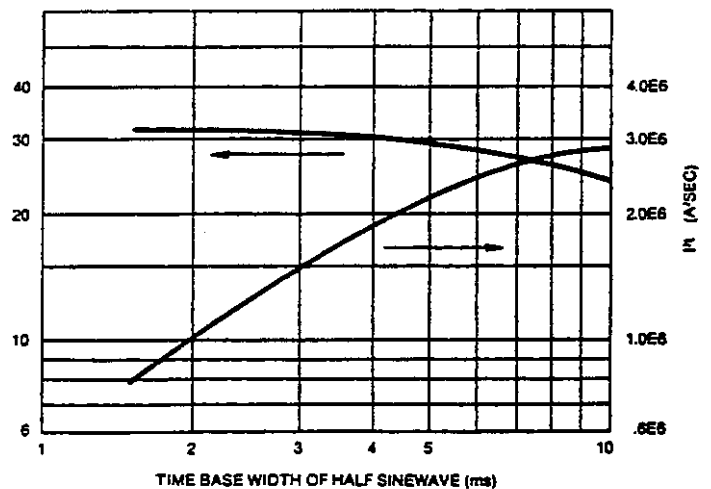
C784 / C787 CHARACTERISTICS

CHARACTERISTIC	SYMBOL	UNITS	MIN.	TYPE	MAX.	TEST CONDITIONS
Peak Off-state Current	I_{DRM} I_{DRM}	ma ma			20 300	$T_j = 25^\circ\text{C}$ Gate Opened $= 125^\circ\text{C}$ Gate Opened
Peak Reverse Current	I_{RRM} I_{RRM}	ma ma			20 200	$T_j = 25^\circ\text{C}$ Gate Opened $= 125^\circ\text{C}$ Gate Opened
Critical exponential rate of rise of off-state voltage (higher rates may cause destructive switching).	dv/dt	$\text{V}/\mu\text{s}$	1000			$T_j = 125^\circ\text{C}$, $V_D = 0.7V_{DRM}$ open gate
Delay Time	t_d	μs	1.5	2.5	3.0	$T_j = 125^\circ\text{C}$, $V_D = 2000\text{V}$
Gate Trigger Current*	I_{GT}	ma			300	$T_j = 25^\circ\text{C}$, $V_D = 12\text{V DC}$
Gate Trigger Voltage*	V_{GT}	V			4.5	
Non-Trigger Current	I_{GDM}	ma	15			$T_j = 115^\circ\text{C}$, $V_D = 2000\text{V}$ AC Crest
Non-Trigger Voltage	V_{GDM}	V	0.8			
Operational Gate Current. Voltage requirement	I_{GA} V_{GA}	A V	1.5 25			Gate source: - open circuit - 40V - short circuit - 4A - rise time $\approx 0.5\mu\text{s}$ - duration $t_p > t_d$
Conventional Circuit Commutating Turn-off time (with reverse voltage)	t_q	μs			400	$T_j = 100^\circ\text{C}$, $I_T = 2000\text{A}$ $t_p > 2\text{ms}$ $di/dt = 5\text{A}/\mu\text{s}$ $V_r = 100\text{V}$ $dv/dt = 1000\text{V}/\mu\text{s}$ V reapplied = 2000V
Holding Current	I_H	ma	45 27 22	80 48 40	250 150 125	$T_j = 25^\circ\text{C}$, $di/dt = -5\text{ma}/\mu\text{s}$ 105°C , $E = 7.5\text{Vrms}$ 125°C , $R = 10\text{ ohms}$ Freq = 60Hz
Latching Current	I_L	ma	300 225 205	450 340 310	1000 750 690	$T_j = 25^\circ\text{C}$ Gate Drive 105°C 30V/10 ohms 125°C duration 15 μs

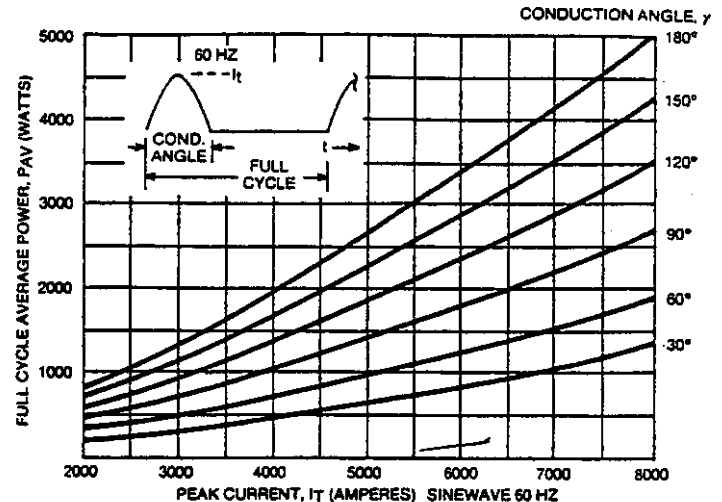
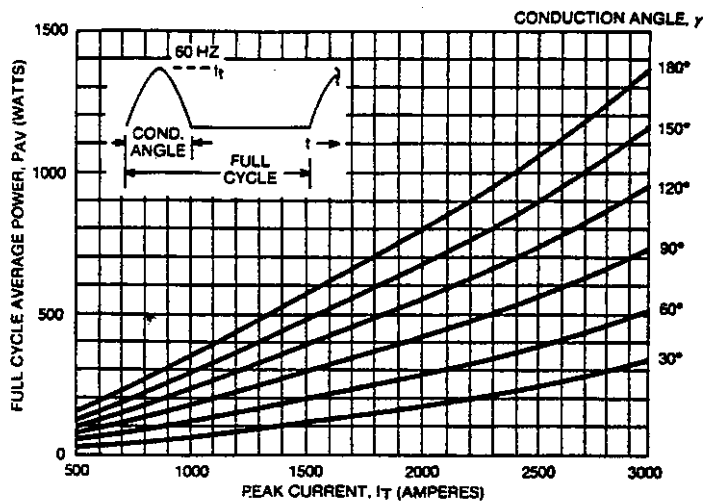
*DC trigger current and voltage are indicated as a characteristic. Turn-on in this manner will not support rated di/dt .



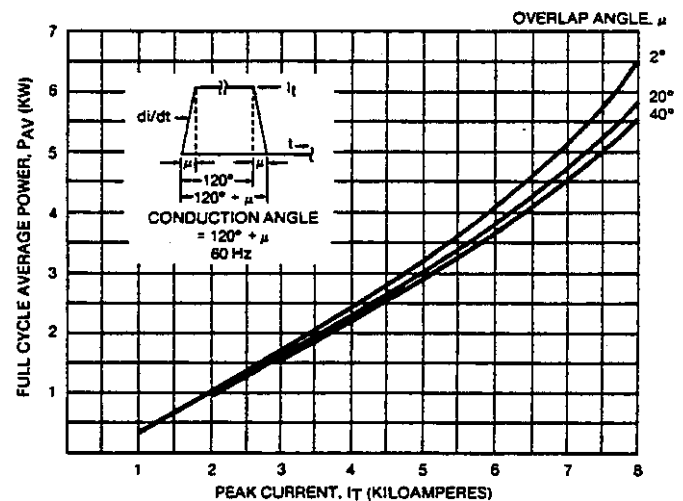
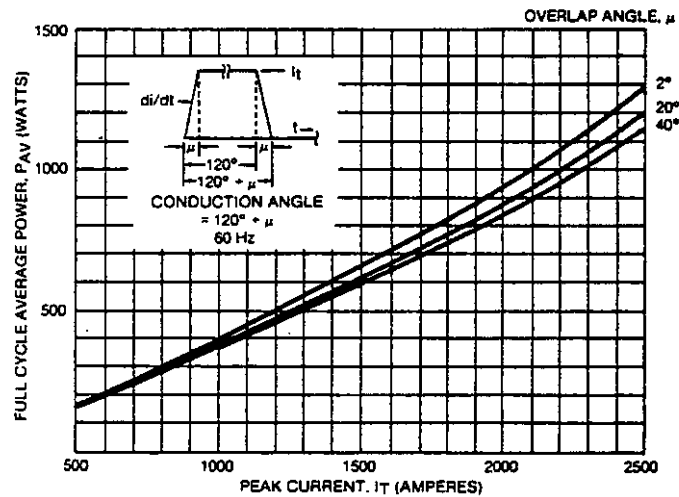
**MAXIMUM FORWARD CONDUCTION
CHARACTERISTIC ON-STATE**



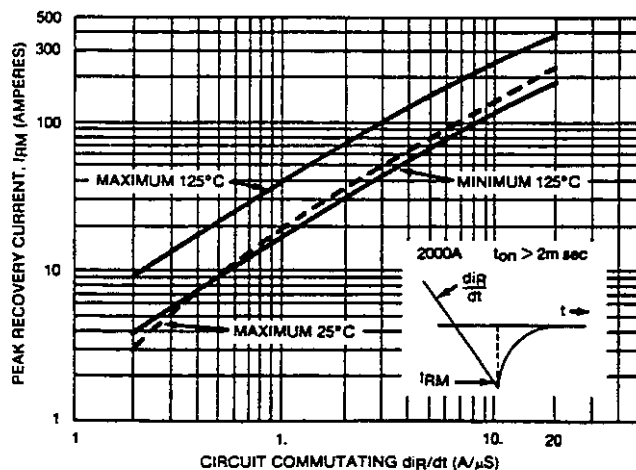
**NON-REPETITIVE I_{TSM} and I_t^2t CAPABILITY
FOR FUSE COORDINATION**



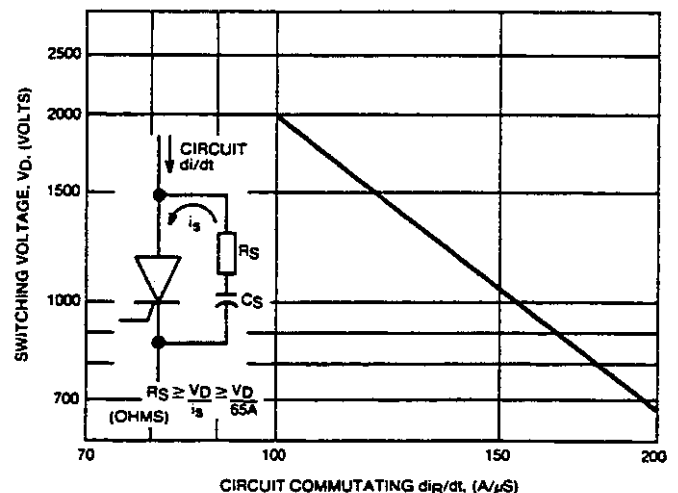
MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR SINEWAVE CURRENT AT VARIOUS CONDUCTING ANGLES. EFFECT OF VARIABLE CONDUCTING AREA IS INCLUDED. (DIGITAL DATA IS AVAILABLE)



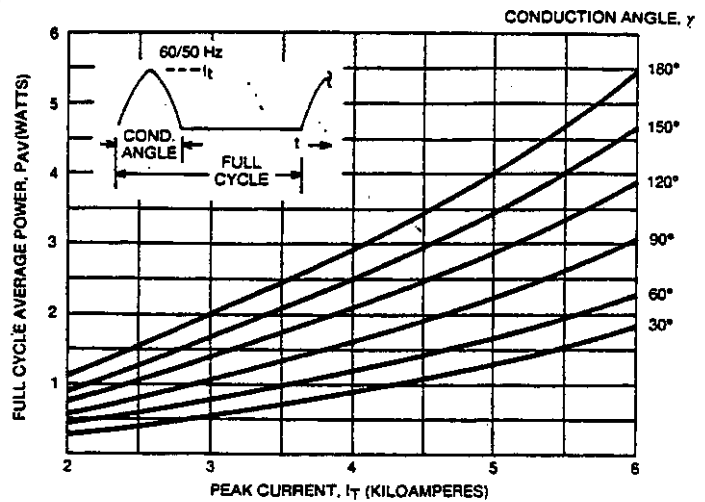
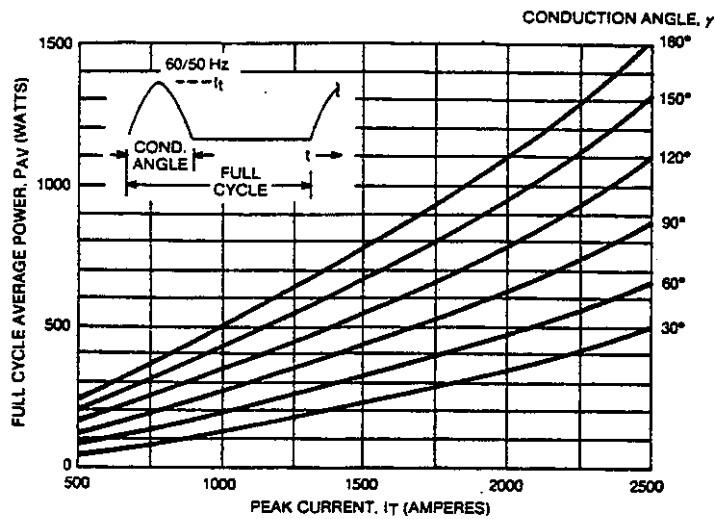
MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR THREE PHASE RECTIFIER (120° CONDUCTION) AT SEVERAL OVERLAP ANGLES, " μ ". EFFECT OF VARIABLE CONDUCTING AREA IS INCLUDED. (DIGITAL DATA IS AVAILABLE)



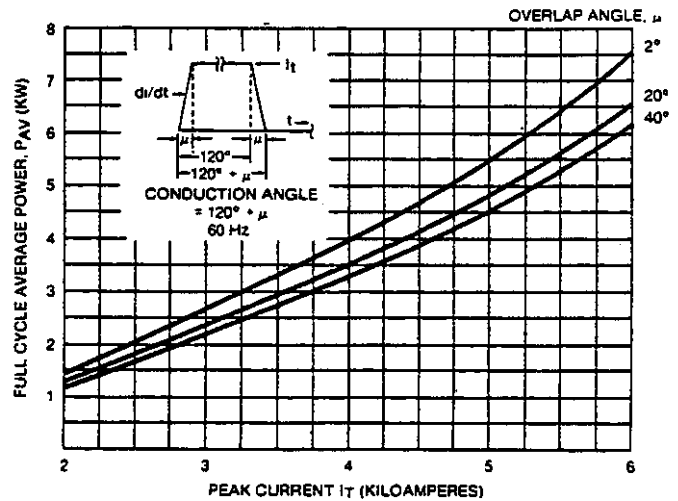
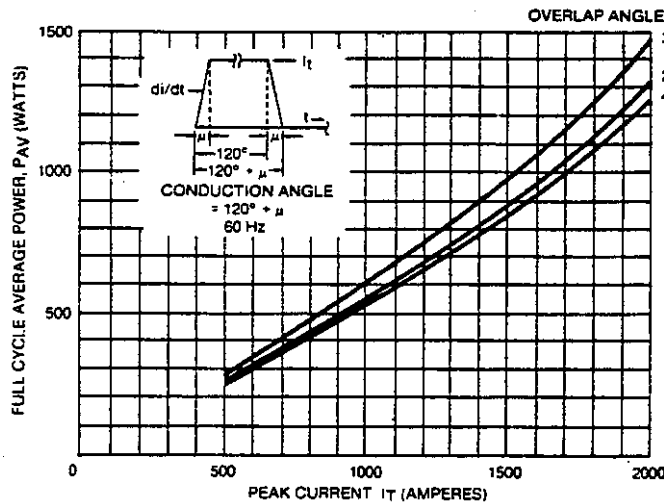
PEAK RECOVERY CURRENT VERSUS COMMUTATING CIRCUIT DI/DT



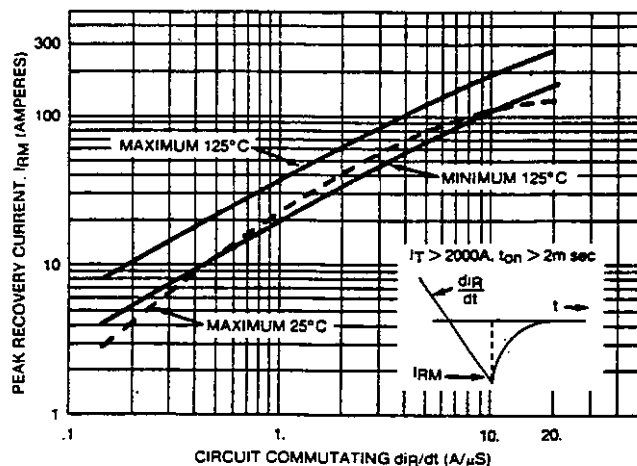
MAXIMUM ALLOWABLE REPETITIVE DI/DT AS FUNCTION OF ANODE VOLTAGE BIAS. LIMITATION ON ADDITIONAL SNUBBER DISCHARGE IS INDICATED.



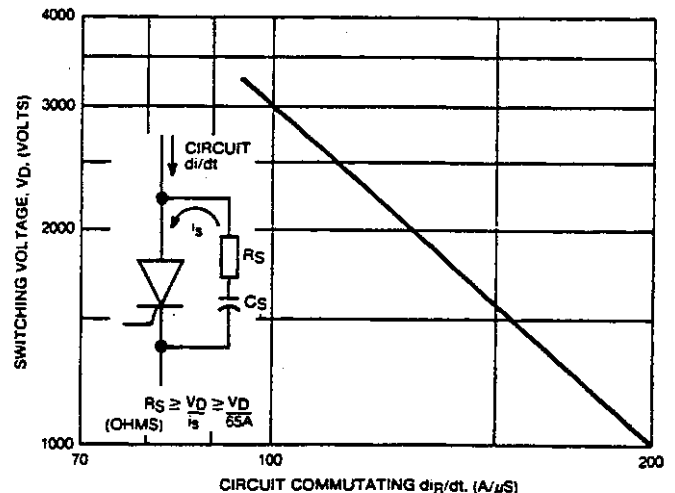
MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR SINEWAVE CURRENT AT VARIOUS CONDUCTING ANGLES. EFFECT OF VARIABLE CONDUCTING AREA IS INCLUDED. (DIGITAL DATA IS AVAILABLE)



MAXIMUM FULL CYCLE AVERAGE POWER DISSIPATION FOR THREE PHASE RECTIFIER (120° CONDUCTION) AT SEVERAL OVERLAP ANGLES, " μ ". EFFECT OF VARIABLE CONDUCTING AREA IS INCLUDED. (DIGITAL DATA IS AVAILABLE)

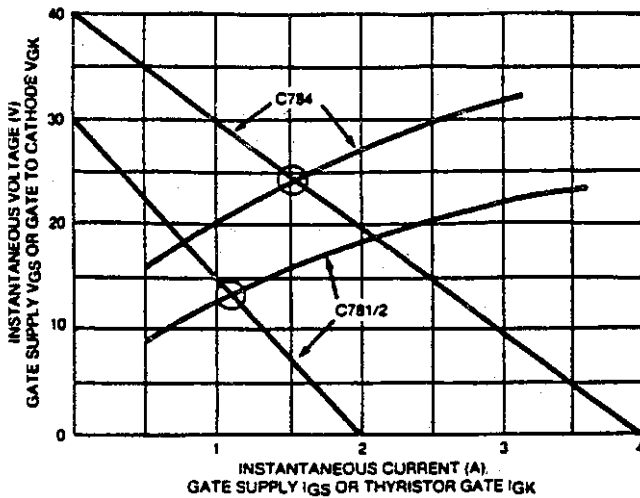


PEAK RECOVERY CURRENT VERSUS COMMUTATING CIRCUIT DI/DT



MAXIMUM ALLOWABLE REPETITIVE DI/DT AS FUNCTION OF ANODE VOLTAGE BIAS. LIMITATION ON ADDITIONAL SNUBBER DISCHARGE IS INDICATED.

GATE CHARACTERISTICS AND GATE SUPPLY REQUIREMENTS



Thyristor Gate Impedance

- This is enhanced by fast rising gate voltage, increasing anode bias and temperature.
- It is at a minimum for dc voltage, zero bias and low temperature (not shown).
- The maximum impedances expected for C784 and C781/C782 are indicated as curves of gate current versus gate voltage.

Gate Supply

- Load lines for 40V/10Ω and 30V/15Ω are shown. The short circuit current rise time should be approximately 0.5μs and the duration longer than the delay time expected for the thyristor.

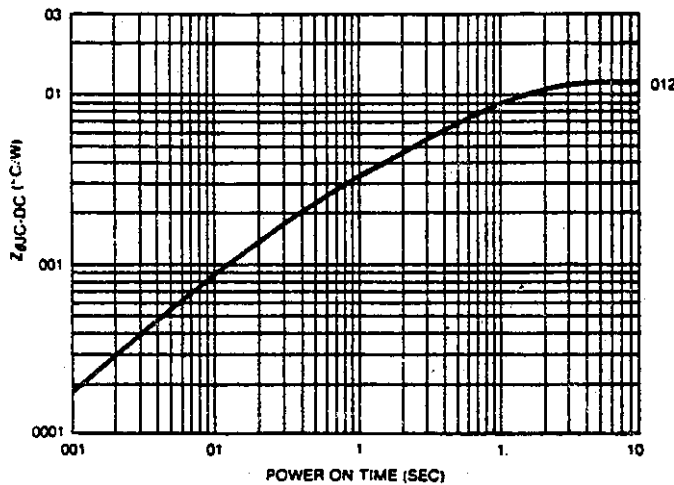
Minimum Acceptable Gate Current

- The intersection of load line and gate characteristic (encircled) indicates the minimum value of actual current flowing into the gate that is required during the delay time interval needed for the published di/dt and snubber discharge ratings.

Additional Gate Ratings (maximums)

- Peak gate power, P_{GM} (100μs) 250W
- Average gate power, $P_{G(AV)}$ 35W
- Peak gate current 20A
- Peak reverse voltage V_{GRM} 20V

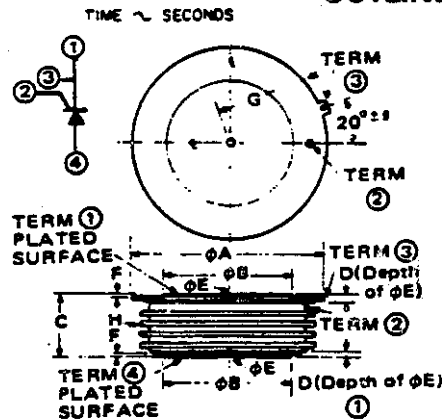
THERMAL AND MECHANICAL INFORMATION



NOTES:

- Add .002°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R_{θJS} = .014°C/W$. See Mounting Instructions.
- DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
 - end of conducting portion of cycle
 - 120° sq. wave add .0012°C/W along entire curve
 - 180° sq. wave add .0010°C/W along entire curve
 - 180° sine wave add .0005°C/W along entire curve
 - end of full cycle
 - any wave, subtract .0005°C/W along entire curve.
- Ask for general mounting instructions.

OUTLINE DRAWING



Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
φA	—	4.350	—	110.49
φB	2.876	2.880	73.05	73.15
C	1.387	1.447	35.23	36.75
D	.080	—	2.03	—
φE	0.136	0.146	3.45	3.71
F	.020	—	0.86	—
G	2.403	2.418	61.16	61.42
H	—	—	—	—

*** for C785 & C787 only ***
 "C" = 1.000 - 1.070 in.
 25.40 - 27.18 mm
 surface creepage = 1.00 in.

- Anode-Cathode Pole Faces ① ① Nickel Plated Copper.
- Mounting Force, 7000 - 9000 lb / 31.1 - 40.0 kN
- Electrical Insulation, Glazed Ceramic, Creepage 1.6 in. (40.6mm), Strike 1.0 in. (25.4mm)
- Gate Leads ② ② 18 in. #22 Terminated Nickel Plated with #8 Ring Terminal