

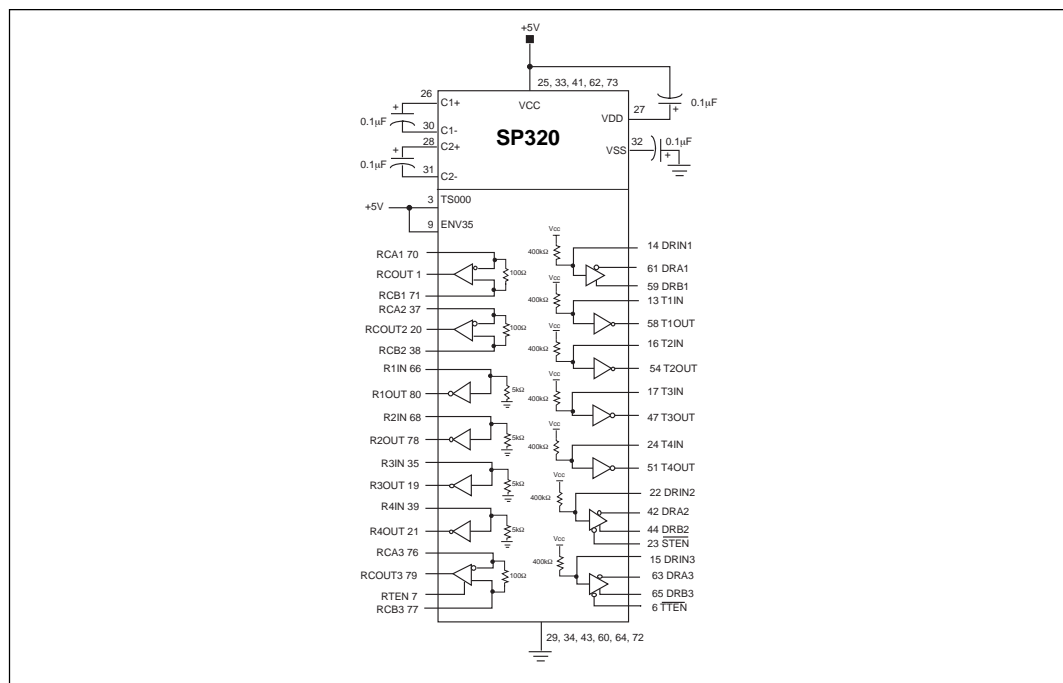
## Complete +5V-Only V.35 Interface with RS-232 (V.28) Control Lines

- 10Mbps Data Throughput
- +5V-Only, Single Supply Operation
- 3 Drivers, 3 Receivers – V.35
- 4 Drivers, 4 Receivers – RS-232
- 80-pin QFP Surface Mount Packaging
- Pin Compatible with SP319



### DESCRIPTION

The **SP320** is a complete V.35 interface transceiver offering 3 drivers and 3 receivers of V.35, and 4 drivers and 4 receivers of RS-232 (V.28). A **Sipex** patented charge pump allows +5V only low power operation. RS-232 drivers and receivers are specified to operate at 120kbps, all V.35 drivers and receivers operate up to 5Mbps.



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V <sub>CC</sub> .....	+7V
Input Voltages	
Logic.....	-0.3V to (V <sub>CC</sub> +0.5V)
Drivers.....	-0.3V to (V <sub>CC</sub> +0.5V)
Receivers.....	±30V at ≤100mA
Output Voltages	
Logic.....	-0.3V to (V <sub>CC</sub> +0.5V)
Drivers.....	±14V
Receivers.....	-0.3V to (V <sub>CC</sub> +0.5V)
Storage Temperature.....	-65°C to +150°C
Power Dissipation.....	1500mW
Package Derating	
θ <sub>JC</sub> .....	16 °C/W
θ <sub>JA</sub> .....	46 °C/W

## SPECIFICATIONS

T<sub>MIN</sub> to T<sub>MAX</sub> and V<sub>CC</sub> = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>V.35 DRIVER</b>					
TTL Input Levels					
V <sub>IL</sub>	2.0		0.8	Volts	
V <sub>IH</sub>				Volts	
Voltage Outputs					
Differential Outputs	±0.44	±0.55	±0.66	Volts	R <sub>L</sub> =100Ω from A to B
Source Impedance	50	100	150	Ohms	Measured from A=B to Gnd, V <sub>OUT</sub> =-2V to +2V
Short Circuit Impedance	135	150	165	Ohms	
Voltage Output Offset	-0.6		+0.6	Volts	V <sub>Offset</sub> ={ V <sub>A</sub>  + V <sub>B</sub>  }/2}
AC Characteristics					
Transition Time	5	40		ns	Rise/fall time, 10% to 90%
Maximum Transmission Rate				Mbps	R <sub>L</sub> =100Ω, V <sub>DIFF OUT</sub> = 0.55V±20%
Propagation Delay					
t <sub>PHL</sub>		150	250	ns	Measured from 1.5V of V <sub>IN</sub> to 50% of V <sub>OUT</sub>
t <sub>PLH</sub>		150	250	ns	Measured from 1.5V of V <sub>IN</sub> to 50% of V <sub>OUT</sub>
<b>V.35 RECEIVER</b>					
TTL Output Levels					
V <sub>OL</sub>	2.4		0.4	Volts	I <sub>OUT</sub> =-3.2mA I <sub>OUT</sub> =1.0mA
V <sub>OH</sub>				Volts	
Receiver Inputs					
Differential Input	-0.3		+0.3	Volts	Measured from A=B to Gnd V <sub>IN</sub> =-2V to +2V
Threshold				Volts	
Input Impedance	90	100	110	Ohms	
Short Circuit Impedance	135	150	165	Ohms	
AC Characteristics					
Maximum Transmission Rate	5			Mbps	V <sub>IN</sub> = ±0.55V ±20%
Propagation Delay					
t <sub>PHL</sub>		150	250	ns	Measured from 50% of V <sub>IN</sub> to 1.5V of R <sub>OUT</sub>
t <sub>PLH</sub>		150	250	ns	Measured from 50% of V <sub>IN</sub> to 1.5V of R <sub>OUT</sub>

## SPECIFICATIONS (CONTINUED)

$T_{MIN}$  to  $T_{MAX}$  and  $V_{CC} = 5V \pm 5\%$  unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>RS-232 DRIVER</b>					
TTL Input Levels					
$V_{IL}$			0.8	Volts	
$V_{IH}$	2.0			Volts	
Voltage Outputs					
High Level Output	+5.0		+15.0	Volts	$R_L = 3k\Omega$ to Gnd
Low Level Output	-15.0		-5.0	Volts	$R_L = 3k\Omega$ to Gnd
Open Circuit Output	-15		+15	Volts	$R_L = \infty$
Short Circuit Current	-100		+100	mA	$R_L = \text{Gnd}$
Power Off Impedance	300			Ohms	$V_{CC} = 0V$ ; $V_{OUT} = \pm 2V$
AC Characteristics					
Slew Rate			30	V/ $\mu s$	$R_L = 3k\Omega$ , $C_L = 50pF$ ; From +3V to -3V or -3V to +3V, $T_A = 25^\circ C$ , $V_{CC} = +5V$
Maximum Transmission Rate	120			kbps	$R_L = 3k\Omega$ , $C_L = 2500pF$
Transition Time			1.56	$\mu s$	Rise/fall time, between $\pm 3V$
Propagation Delay					$R_L = 3k\Omega$ , $C_L = 2500pF$
$t_{PHL}$		2	8	$\mu s$	$R_L = 3k\Omega$ , $C_L = 2500pF$ ; From 1.5V of $T_{IN}$ to 50% of $V_{OUT}$
$t_{PLH}$		2	8	$\mu s$	$R_L = 3k\Omega$ , $C_L = 2500pF$ ; From 1.5V of $T_{IN}$ to 50% of $V_{OUT}$
<b>RS-232 RECEIVER</b>					
TTL Output Levels					
$V_{OL}$			0.4	Volts	
$V_{OH}$	2.4			Volts	
Receiver Input					
Input Voltage Range	-15		+15	Volts	
High Threshold		1.7	3.0	Volts	
Low Threshold	0.8	1.2		Volts	
Hysteresis	0.2	0.5	1	Volts	$V_{CC} = 5V$ ; $T_A = +25^\circ C$
Receiver Input Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	kOhms	$V_{IN} = \pm 15V$
AC Characteristics					
Maximum Transmission Rate	120			kbps	
Propagation Delay					
$t_{PHL}$		0.1	1	$\mu s$	From 50% of $R_{IN}$ to 1.5V of $R_{OUT}$
$t_{PLH}$		0.1	1	$\mu s$	From 50% of $R_{IN}$ to 1.5V of $R_{OUT}$
<b>POWER REQUIREMENTS</b>					
No Load $V_{CC}$ Supply Current		35	70	mA	No load; $V_{CC} = 5.0V$ ; $T_A = 25^\circ C$
Full Load $V_{CC}$ Supply Current		60		mA	RS-232 drivers $R_L = 3k\Omega$ to Gnd; DC Input
					V.35 drivers $R_L = 100\Omega$ from A to B; DC Input
Shutdown Current		1.5		mA	TS000 = ENV35 = 0V

## THEORY OF OPERATION

The **SP320** is a single chip +5V-only serial transceiver that supports all the signals necessary to implement a full V.35 interface. Three V.35 drivers and three V.35 receivers make up the clock and data signals. Four RS-232 (V.28) drivers and four RS-232 (V.28) receivers are used for control line signals for the interface.

### V.35 Drivers

The V.35 drivers are +5V-only, low power voltage output transmitters. The drivers do not require any external resistor networks, and will meet the following requirements:

1. Source impedance in the range of  $50\Omega$  to  $150\Omega$ .
2. Resistance between short-circuited terminals and ground is  $150\Omega \pm 15\Omega$ .
3. When terminated with a  $100\Omega$  resistive load the terminal to terminal voltage will be 0.55 Volts  $\pm 20\%$  so that the A terminal is positive to the B terminal when binary 0 is transmitted, and the conditions are reversed to transmit binary 1.
4. The arithmetic mean of the voltage of the A terminal with respect to ground, and the B terminal with respect to ground will not exceed 0.6 Volts when terminated as in 3 above.

The V.35 drivers can operate at data rates as high as 5Mbps. The driver outputs are protected against short-circuits between the A and B outputs and short circuits to ground.

Two of the V.35 drivers, DRIN2 and DRIN3 are equipped with enable control lines. When the enable pins are high the driver outputs are disabled, the output impedance of a disabled driver will nominally be  $300\Omega$ . When the enable pins are low, the drivers are active.

### V.35 Receivers

The V.35 receivers are +5V only, low power differential receivers which meet the following requirements:

1. Input impedance in the range of  $100\Omega \pm 10\Omega$ .
2. Resistance to ground of  $150\Omega \pm 15\Omega$ , measured from short-circuited terminals.

All of the V.35 receivers can operate at data rates as high as 5Mbps. The sensitivity of the V.35 receiver inputs is  $\pm 300\text{mV}$ .

### RS-232 (V.28) Drivers

The RS-232 drivers are inverting transmitters, which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 9\text{V}$  with no load, and  $\pm 5\text{V}$  minimum with full load. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

In the power off state, the output impedance of the RS-232 drivers will be greater than  $300\Omega$  over a  $\pm 2\text{V}$  range. Should the input of a driver be left open, an internal  $400\text{k}\Omega$  pullup resistor to  $V_{CC}$  forces the input high, thus committing the output to a low state. The slew rate of the transmitter output is internally limited to a maximum of  $30\text{V}/\mu\text{s}$  in order to meet the EIA standards. The RS-232 drivers are rated for 120kbps data rates.

### RS-232 (V.28) Receivers

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the effects of noisy transmission lines. The inputs also have a  $5\text{k}\Omega$  resistor to ground; in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain  $3\text{k}\Omega$ - $7\text{k}\Omega$  over a  $\pm 15\text{V}$  range. The maximum operating voltage range for the receiver is  $\pm 30\text{V}$ , under these conditions the input current to the receiver must be limited to less than 100mA. The RS-232 receivers can operate to beyond 120kbps.

### CHARGE PUMP

The charge pump is a **Sipex** patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical  $\pm 10\text{V}$  power supplies. The capacitors can be as low as  $0.1\mu\text{F}$  with a 16 Volt rating. Polarized or non-polarized capacitors can be used.

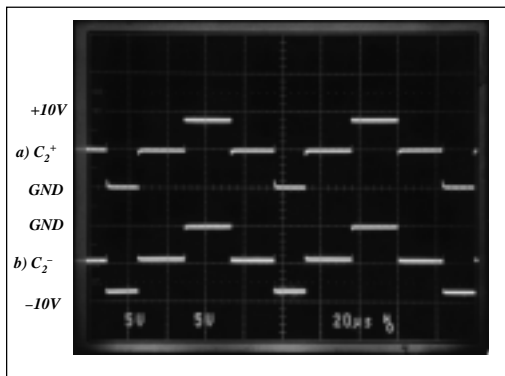


Figure 1. Charge Pump Waveforms

Figure 1a shows the waveform found on the positive side of capacitor C2, and Figure 1b shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

#### Phase 1

**-Vss charge storage-** During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and the charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

#### Phase 2

**-Vss transfer-** Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

#### Phase 3

**-Vdd charge storage-** The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is +10V.

#### Phase 4

**-Vdd transfer-** The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated +10V across C2 to C4, the Vdd storage capacitor. Again, simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 0.1μF with a 16V breakdown rating.

#### Shutdown Mode

The **SP320** can be put into a low power shutdown mode by bringing both TS000 (pin 3) and ENV35 (pin 9) low. In shutdown mode, the **SP320** will draw less than 2mA of supply current. For normal operation, both pins should be connected to +5V.

#### External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V- pins. The value of the external supply voltages must be no greater than ±10V. The current drain from the ±10V supplies is used for the RS-232 drivers. For the RS-232 driver the current requirement will be 3.5mA per driver. It is critical the external power supplies provide a power supply sequence of : +10V, +5V, and then -10V.

#### Applications Information

The **SP320** is a single chip device that can implement a complete V.35 interface. Three (3) V.35 drivers and three (3) V.35 receivers are used for clock and data signals and four (4) RS-232 (V.28) drivers and four (4) RS-232 (V.28) receivers can be used for the control signals of the interface. The following examples show the **SP320** configured in either a DTE or DCE application.

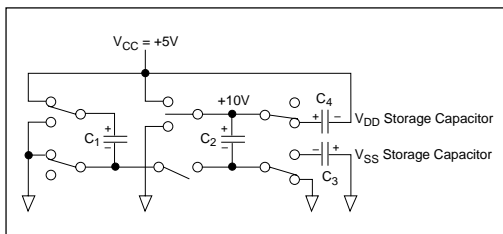


Figure 2. Charge Pump Phase 1

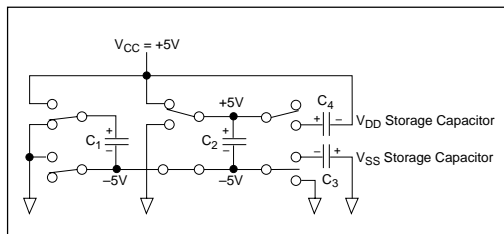


Figure 3. Charge Pump Phase 2

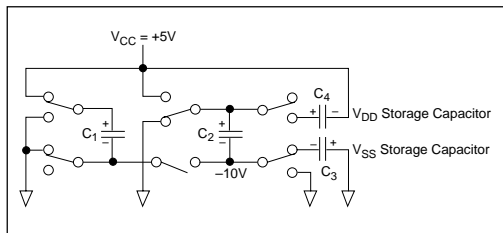


Figure 4. Charge Pump Phase 3

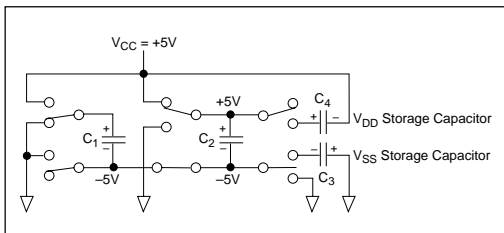


Figure 5. Charge Pump Phase 4

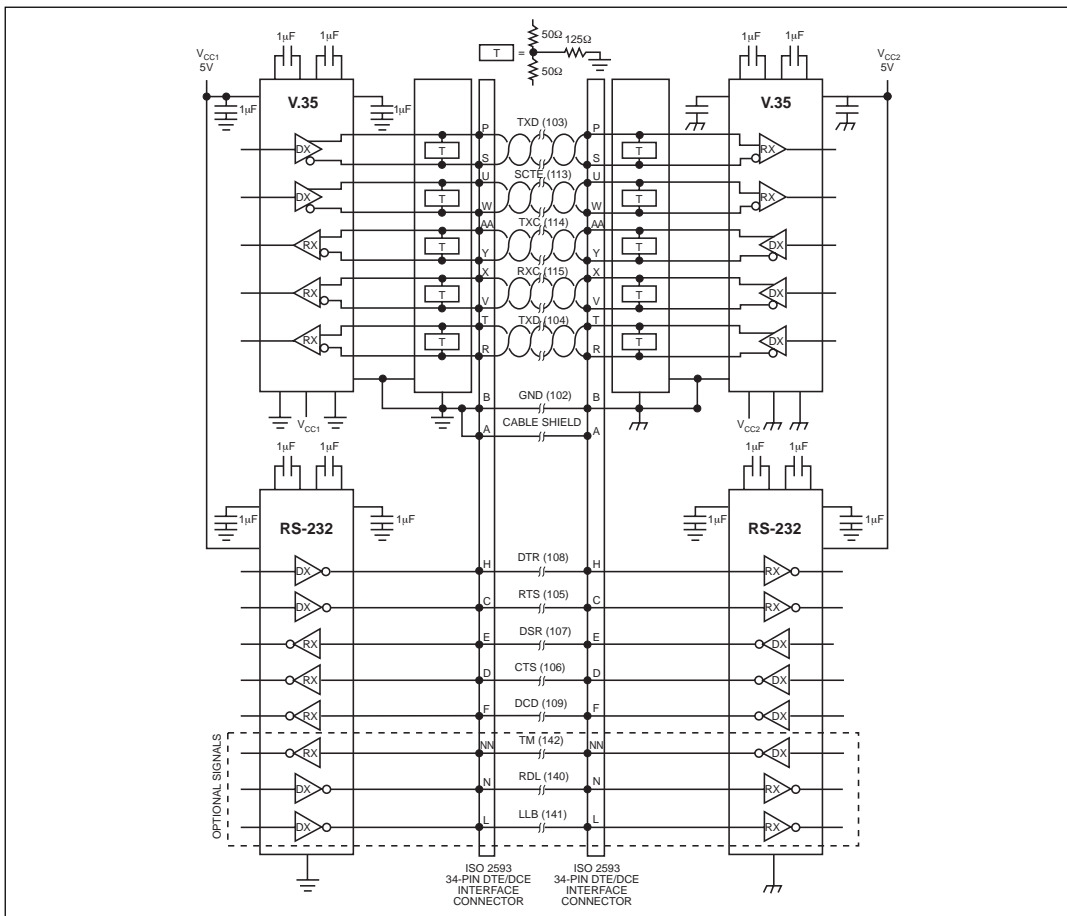
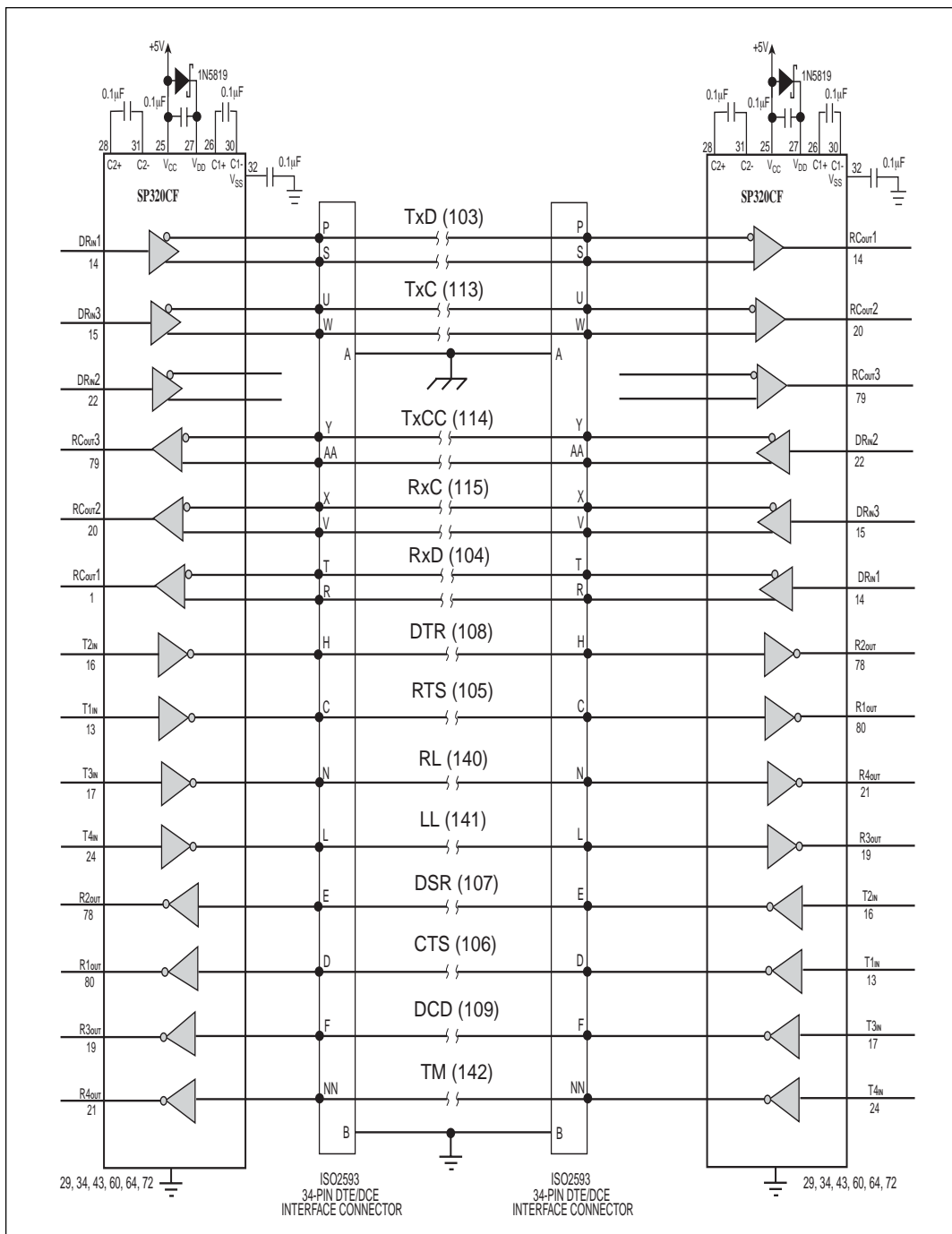


Figure 6. A Competitor's Typical V.35 Solution Using Six Components.

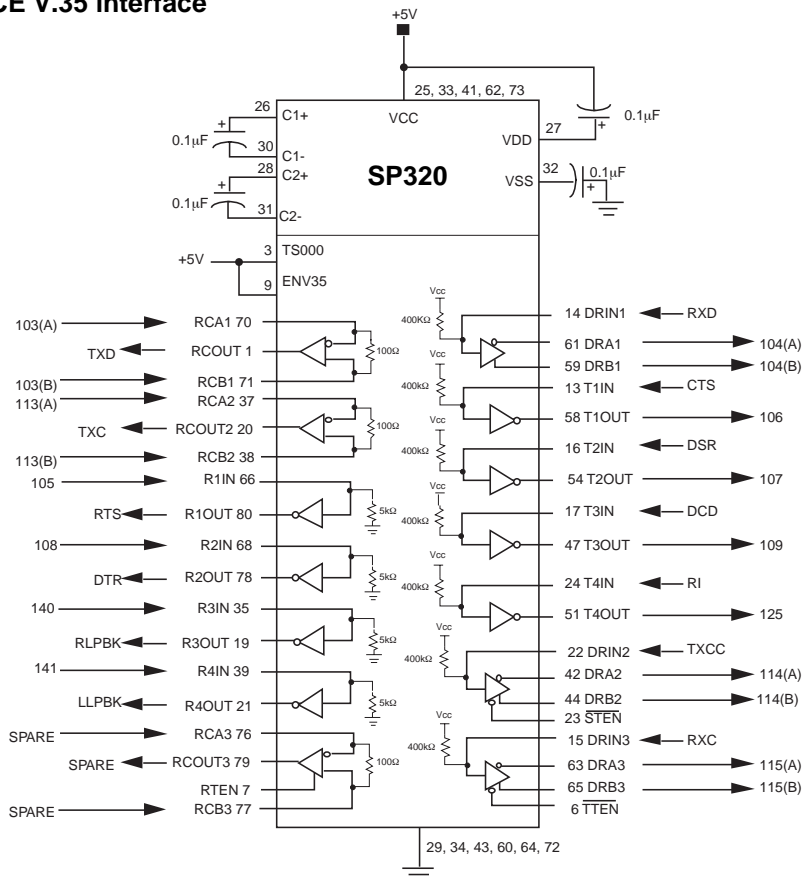


**Figure 7. Typical DTE-DCE V.35 Connection with the SP320**

## ISO-2593 connector pin out

Signal Ground	B		A	Chasis Ground
Clear to Send	D		C	Request to Send
Data Carrier Detect	F		E	DCE Ready (DSR)
Ring Indicator	J		H	DTE Ready (DTR)
Local Loopback	L		K	Unassigned---
Remote Loopback	N		M	Unassigned---
Receive Data (A)	R		P	Transmitted Data (A)
Receive Data (B)	T		S	Transmitted Data (B)
Receive Timing (A)	V		U	Terminal Timing (A) } 113(A)
Receive Timing (B)	X		W	Terminal Timing (B) } 113(B)
Unassigned---	Z		Y	Transmit Timing (A) } 114(A)
Unassigned---	BB		AA	Transmit Timing (B) } 114(B)
Unassigned---	DD		CC	Unassigned---
Unassigned---	FF		EE	Unassigned---
Unassigned---	JJ		HH	Unassigned---
Unassigned---	LL		KK	Unassigned---
Test Mode	NN		MM	Unassigned---

## Typical DCE V.35 interface

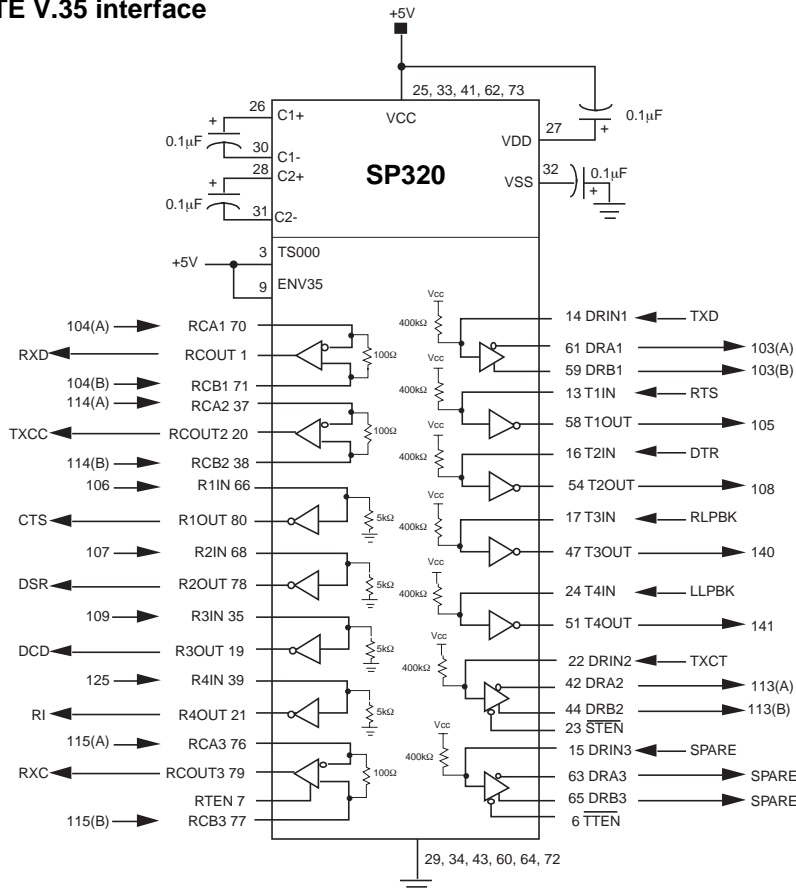




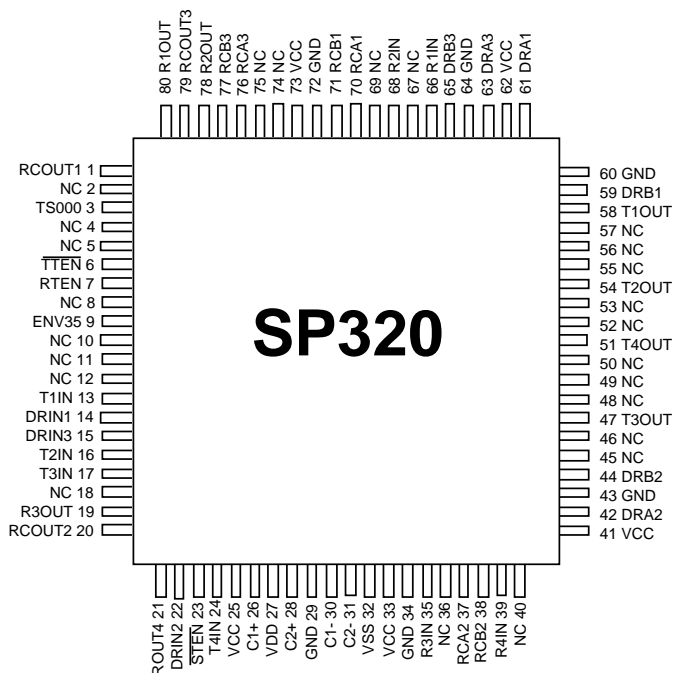
## ISO-2593 connector pin out

Signal Ground	B		A	Chasis Ground
Clear to Send	D		C	Request to Send
Data Carrier Detect	F		E	DCE Ready (DSR)
Ring Indicator	J		H	DTE Ready (DTR)
Local Loopback	L		K	Unassigned---
Remote Loopback	N		M	Unassigned---
Receive Data (A)	R		P	Transmitted Data (A)
Receive Data (B)	T		S	Transmitted Data (B)
Receive Timing (A)	V		U	Terminal Timing (A) } 113(A)
Receive Timing (B)	X		W	Terminal Timing (B) } 113(B)
Unassigned---	Z		Y	Transmit Timing (A) } 114(A)
Unassigned---	BB		AA	Transmit Timing (B) } 114(B)
Unassigned---	DD		CC	Unassigned---
Unassigned---	FF		EE	Unassigned---
Unassigned---	JJ		HH	Unassigned---
Unassigned---	LL		KK	Unassigned---
Test Mode	NN		MM	Unassigned---

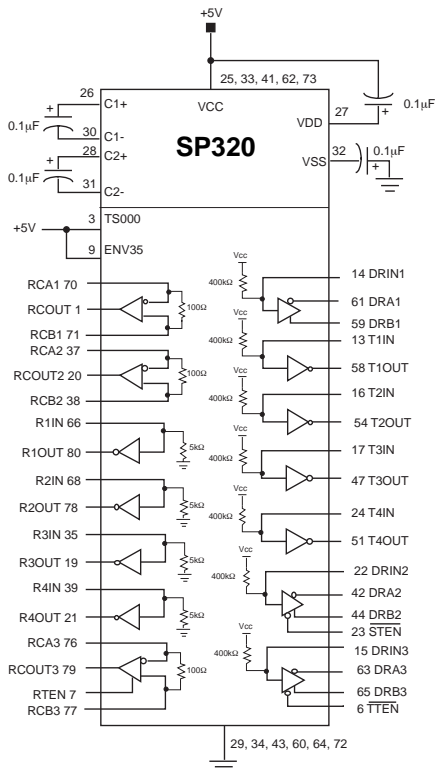
## Typical DTE V.35 interface



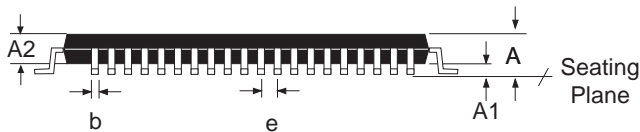
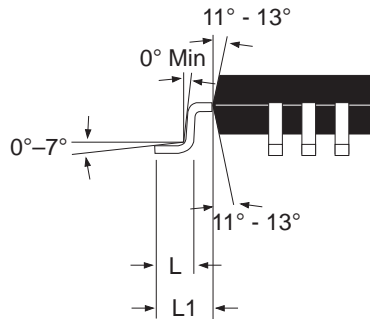
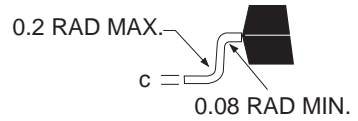
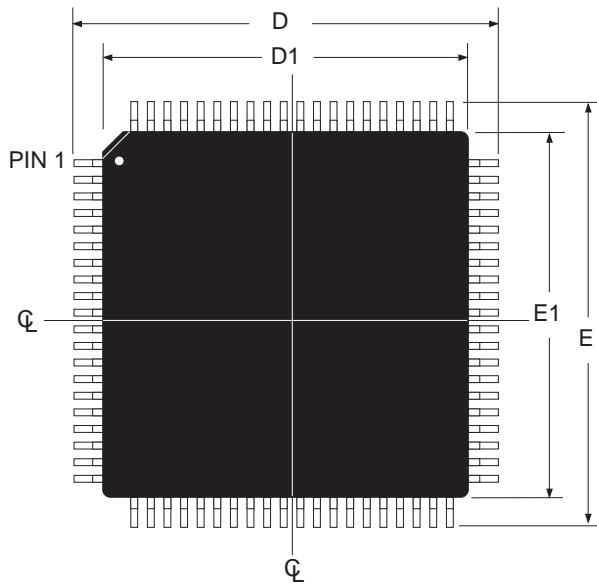
## Typical application circuit



## Rev. 7/9/03



# PACKAGE: 80 Pin LQFP

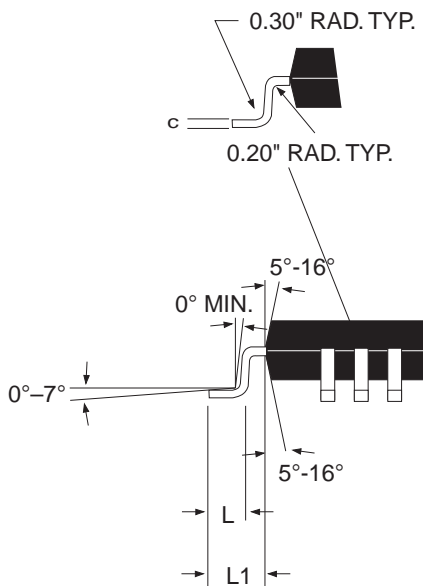
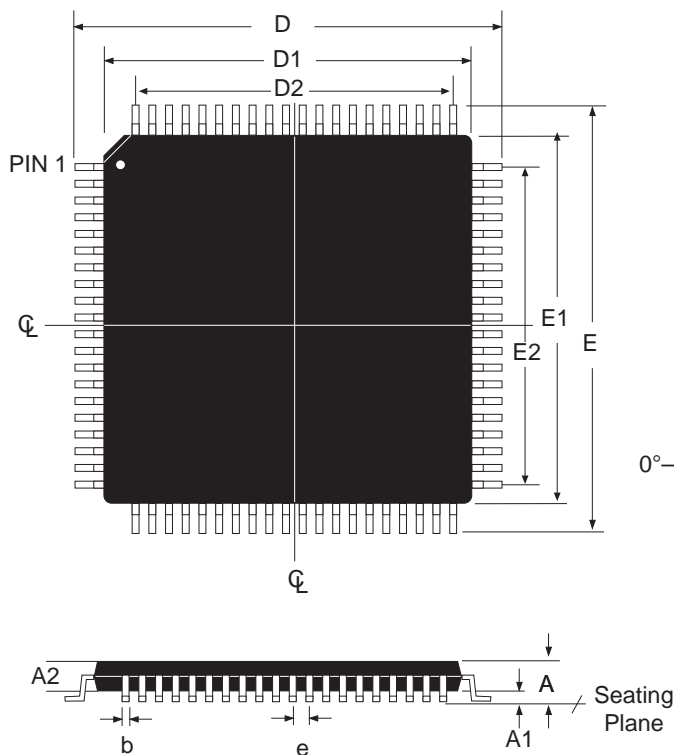


DIMENSIONS Minimum/Maximum (mm)	80-PIN LQFP JEDEC MS-026 (BEC) Variation		
SYMBOL	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
D	16.00 BSC		
D1	14.00 BSC		
e	0.65 BSC		
E	16.00 BSC		
E1	14.00 BSC		
N	80		

COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
c	0.11		23.00
L	0.45	0.60	0.75
L1	1.00 BASIC		

80 PIN LQFP

# PACKAGE: 80 Pin MQFP



DIMENSIONS Minimum/Maximum (mm)	80-PIN MQFP JEDEC MS-22 (BEC) Variation		
SYMBOL	MIN	NOM	MAX
A			2.45
A1	0.00		0.25
A2	1.80	2.00	2.20
b	0.22		0.40
D	17.20 BSC		
D1	14.00 BSC		
D2	12.35 REF		
E	17.20 BSC		
E1	14.00 BSC		
E2	12.35 REF		
e	0.65 BSC		
N	80		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.73	0.88	1.03
L1	1.60 BASIC		

80 PIN MQFP (MS-022 BC)

ORDERING INFORMATION		
Model	Temperature Range	Package Types
SP320ACF .....	0°C to +70°C .....	80-pin JEDEC (BE-2 Outline) MQFP
SP320ACM .....	0°C to +70°C .....	80-pin JEDEC (BE-2 Outline) LQFP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation reserves the right to make changes to any products described herein. Sipex does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.