

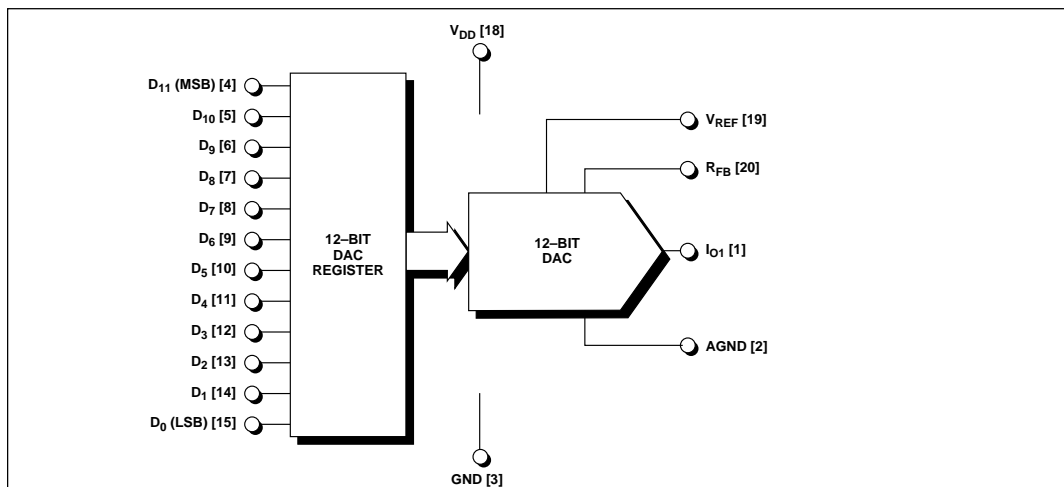
## 12-Bit, Buffered Multiplying DAC

- $\pm 1.0$  LSB Relative Accuracy Over Temperature
- Monotonic to 12-Bits Over Temperature
- High Stability, Segmented Architecture
- Proprietary, Low TCR Thin-Film Resistor Technology
- Operates With +5V to +15V Power Supplies
- On-Board, Level-Triggered Latches
- 2kVESD Protection on all Digital Inputs



### DESCRIPTION...

The **SP7545** is a low-cost, high stability 12-bit CMOS multiplying DAC with on-board data latches. The **SP7545** is constructed using a proprietary low-TCR thin-film process that requires no laser-trimming to achieve 12-bit performance. With no laser-trimming, inherent high stability, and a segmented (decoded) DAC architecture, the **SP7545** retains its performance over time and temperature. The **SP7545** is available for use in commercial and industrial temperature ranges. It is available in 20-pin plastic DIP and PLCC packages.



## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

|   |   |
|---|---|
| $V_{DD}$ to GND .....   | -0.3V, +17V                                 |
| Digital Input Voltage to GND .....                            | -0.3V, $V_{DD} + 0.3\text{V}$               |
| $V_{REF}$ or $V_{REFB}$ to GND .....                          | $\pm 25\text{V}$                            |
| Output Voltage (Pin 1, Pin 2) .....                           | -0.3V, $V_{DD} + 0.3\text{V}$               |
| Power Dissipation (Any Package to $+75^\circ\text{C}$ ) ..... | 450mW                                       |
| Derates above $75^\circ\text{C}$ by .....                     | 6mW/ $^\circ\text{C}$                       |
| Die Junction Temperature .....                                | $+150^\circ\text{C}$                        |
| Storage Temperature .....                                     | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 60 seconds) .....                | $+300^\circ\text{C}$                        |



### CAUTION:

ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## SPECIFICATIONS

( $T_A = 25^\circ\text{C}$ ;  $V_{DD} = +5\text{V}$  or  $+15\text{V}$  as noted;  $V_{REF} = +10\text{V}$ ;  $I_{O1} = \text{AGND} = \text{GND} = 0\text{V}$ ; unipolar unless otherwise noted.)

| PARAMETER                             | MIN. | TYP.        | MAX.       | UNIT                  | CONDITIONS                              |
|---------------------------------------|------|-------------|------------|-----------------------|---|
| <b>STATIC PERFORMANCE</b>             |      |             |            |                       |   |
| Resolution                            | 12   |             |            | Bits                  | Note 6                                  |
| Integral Non-Linearity                |      |             |            |                       | Note 5; 11-bit relative accuracy        |
| -J                                    |      |             | $\pm 2.0$  | LSB                   | Note 5; 12-bit relative accuracy        |
| -K                                    |      |             | $\pm 1.0$  | LSB                   | Note 7                                  |
| Differential Non-Linearity            |      |             |            |                       | Note 5; monotonic to 12-bits            |
| -J                                    |      |             | $\pm 4.0$  | LSB                   | Note 5; monotonic to 12-bits            |
| -K                                    |      |             | $\pm 1.0$  | LSB                   | Note 16                                 |
| Gain Error                            |      |             |            |                       | $V_{DD} = +5\text{V}$ ; Note 5          |
| -J                                    |      |             | $\pm 20$   | LSB                   | $V_{DD} = +15\text{V}$                  |
| -K                                    |      |             | $\pm 25$   | LSB                   | $V_{DD} = +5\text{V}$                   |
|                                       |      |             | $\pm 10$   | LSB                   | $V_{DD} = +15\text{V}$                  |
|                                       |      |             | $\pm 15$   | LSB                   | At $I_{O1}$ (Pin 1); Note 5 and 17      |
| Output Leakage Current                |      |             | $\pm 10$   | nA                    |   |
| <b>AC PERFORMANCE CHARACTERISTICS</b> |      |             |            |                       |   |
| Propagation Delay                     |      |             | 300        | ns                    | Output Amplifier HOS-050; Note 10       |
|                                       |      |             | 250        | ns                    | $V_{DD} = +5\text{V}$ ; Note 11         |
| Current Settling Time                 |      |             | 2.0        | $\mu\text{s}$         | $V_{DD} = +15\text{V}$ ; Note 11        |
| Output Capacitance                    |      | 50          | 200        | pF                    | Full scale transition; Note 12          |
|                                       |      |             | 200        | pF                    | WR, CS = 0V; data inputs $V_{DD}$       |
|                                       |      | 25          | 70         | pF                    | Note 5; data inputs $V_{DD}$            |
|                                       |      |             | 70         | pF                    | Data inputs 0V                          |
| Glitch Energy                         |      | 250         |            | nV-s                  | Note 5; data inputs 0V                  |
| Multiplying Feedthrough Error         |      | 2.0         |            | mV <sub>P-P</sub>     | Note 13                                 |
|                                       |      | 0.2         |            | mV <sub>P-P</sub>     | Measured at output $I_{O1}$ ; Note 14   |
|                                       |      |             |            |                       | Measured at output $I_{O1}$ ; Note 15   |
| <b>STABILITY</b>                      |      |             |            |                       |   |
| Gain Error TC                         |      | $\pm 1.0$   | $\pm 2.0$  | ppm/ $^\circ\text{C}$ | Note 5                                  |
|                                       |      |             | $\pm 2.0$  | ppm/ $^\circ\text{C}$ |   |
| Integral Non-Linearity TC             |      | $\pm 0.1$   | $\pm 1.0$  | ppm/ $^\circ\text{C}$ | Note 5                                  |
|                                       |      |             | $\pm 1.0$  | ppm/ $^\circ\text{C}$ |   |
| Differential Non-Linearity TC         |      | $\pm 0.1$   | $\pm 1.0$  | ppm/ $^\circ\text{C}$ | Note 5                                  |
|                                       |      |             | $\pm 1.0$  | ppm/ $^\circ\text{C}$ |   |
| Power Supply Rejection                |      | $\pm 0.002$ | $\pm 0.01$ | %/%                   | Note 5                                  |
|                                       |      |             | $\pm 0.02$ | %/%                   | %/0.005% change in power supply voltage |
|                                       |      |             |            |                       | Note 5                                  |
| <b>REFERENCE INPUT</b>                |      |             |            |                       |   |
| Input Resistance                      | 7    | 10          | 15         | K $\Omega$            | Pin 19 to GND                           |
| Input Resistance TC                   |      | $\pm 150$   |            | ppm/ $^\circ\text{C}$ | Note 5 and 8                            |
| Voltage Range                         |      |             | $\pm 25$   | Volts                 |   |

## SPECIFICATIONS (continued)

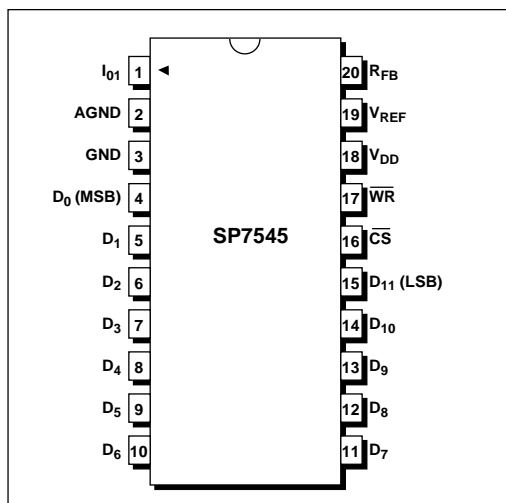
( $T_A = 25^\circ\text{C}$ ;  $V_{DD} = +5\text{V}$ ,  $V_{REF} = +10\text{V}$ ;  $I_{O1} = \text{AGND} = \text{GND} = 0\text{V}$ ; unipolar unless otherwise noted.)

| PARAMETER                           | MIN. | TYP.               | MAX.             | UNIT             | CONDITIONS                              |
|-------------------------------------|------|--------------------|------------------|------------------|---|
| <b>DIGITAL INPUTS</b>               |      |                    |                  |                  |   |
| Logic Levels                        |      |                    |                  |                  |   |
| $V_{IH}$                            | 2.4  |                    | $V_{DD}$<br>2.4  | Volts            | $V_{DD} = +5\text{V}$                   |
|                                     | 13.5 |                    | $V_{DD}$<br>13.5 | Volts            | $V_{DD} = +5\text{V}$ ; Note 5          |
|                                     |      |                    |                  | Volts            | $V_{DD} = +15\text{V}$                  |
|                                     |      |                    |                  | Volts            | $V_{DD} = +15\text{V}$ ; Note 5         |
| $V_{IL}$                            | -0.3 |                    | 0.8              | Volts            | $V_{DD} = +5\text{V}$                   |
|                                     |      |                    | 0.8              | Volts            | $V_{DD} = +5\text{V}$ ; Note 5          |
|                                     |      |                    | 1.5              | Volts            | $V_{DD} = +15\text{V}$                  |
|                                     | -0.3 |                    | 1.5              | Volts            | $V_{DD} = +15\text{V}$ ; Note 5         |
| Input Current                       |      |                    | $\pm 1.0$        | $\mu\text{A}$    | $V_{IN} = 0\text{V}$ or $V_{DD}$        |
|                                     |      |                    | $\pm 10$         | $\mu\text{A}$    | Note 5 and 9                            |
| Input Capacitance                   |      |                    |                  |                  | $V_{IN} = 0$ ; Note 5 and 8             |
| Bits 1—12                           |      |                    | 5                | pF               |   |
| WR, CS                              |      |                    | 20               | pF               |   |
| Coding                              |      |                    |                  |                  |   |
| Unipolar                            |      | Binary             |                  |                  |   |
| Bipolar                             |      | Offset Binary      |                  |                  |   |
| <b>POWER REQUIREMENTS</b>           |      |                    |                  |                  |   |
| Supply Current                      |      |                    | 2.0              | mA               | All digital inputs $V_{IL}$ or $V_{IH}$ |
|                                     |      |                    | 2.0              | mA               | Note 5; all digital inputs              |
|                                     |      |                    | 0.5              | mA               | $V_{IL}$ or $V_{IH}$                    |
|                                     |      |                    |                  | mA               | Note 18                                 |
|                                     |      |                    |                  |                  | Note 5 and 18                           |
| <b>ENVIRONMENTAL AND MECHANICAL</b> |      |                    |                  |                  |   |
| Operating Temperature               |      |                    |                  |                  |   |
| Commercial                          | 0    |                    | +70              | $^\circ\text{C}$ |   |
| Industrial                          | -40  |                    | +85              | $^\circ\text{C}$ |   |
| Storage Temperature                 | -65  |                    | +150             | $^\circ\text{C}$ |   |
| Package                             |      |                    |                  |                  |   |
|                                     |      | 20-pin Plastic DIP |                  |                  |   |
|                                     |      | 20-pin Plastic LCC |                  |                  |   |

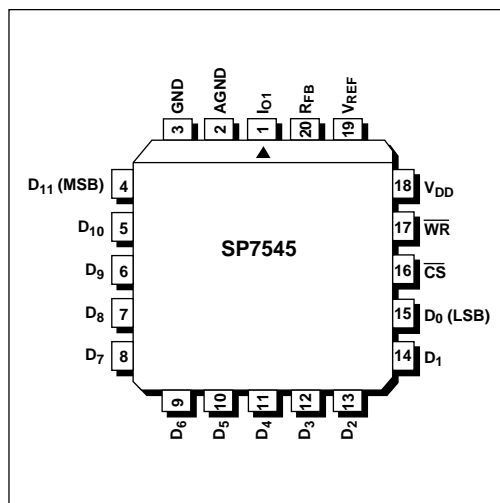
### Notes and Cautions:

- Do not apply voltages higher than  $V_{DD}$  or less than GND potential on any terminal other than  $V_{REF}$  or  $V_{RFB}$ .
- The digital inputs are diode-clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Use proper anti-static handling procedures.
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above these specifications is not implied. Exposure to the above maximum rated conditions for extended periods may affect device reliability.
- From  $T_{MIN}$  to  $T_{MAX}$ .
- End-point linearity
- Differential Non-linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
- Guaranteed by design, but not production tested.
- Logic inputs are MOS gates.  $I_{IN}$  typically is less than 1nA @  $25^\circ\text{C}$ .
- AC performance characteristics are included for design guidance only and are subject to sample testing only.
- $R_L = 100\Omega$ ,  $C_{EXT} = 13\text{pF}$ ; all data inputs 0V to  $V_{DD}$  or  $V_{DD}$  to 0V; from 50% digital input change to 90% of final analog output.
- Settling to  $\pm 0.01\%$  FSR (strobed); all data inputs 0V to  $V_{DD}$  or  $V_{DD}$  to 0V.
- $V_{REF} = 0\text{V}$ , DAC register alternatively loaded with all 0's and all 1's.
- $V_{REF} = 20V_{P-P}$ ;  $F = 10\text{kHz}$  sinewave.
- $V_{REF} = 20V_{P-P}$ ;  $F = 1\text{kHz}$  sinewave.
- Measured using internal feedback resistor with DAC loaded with all 1's.
- All digital inputs = 0V.
- All digital inputs 0V or  $V_{DD}$ .

## PINOUT – PLASTIC DIP



## PINOUT – PLASTIC LCC



## FEATURES...

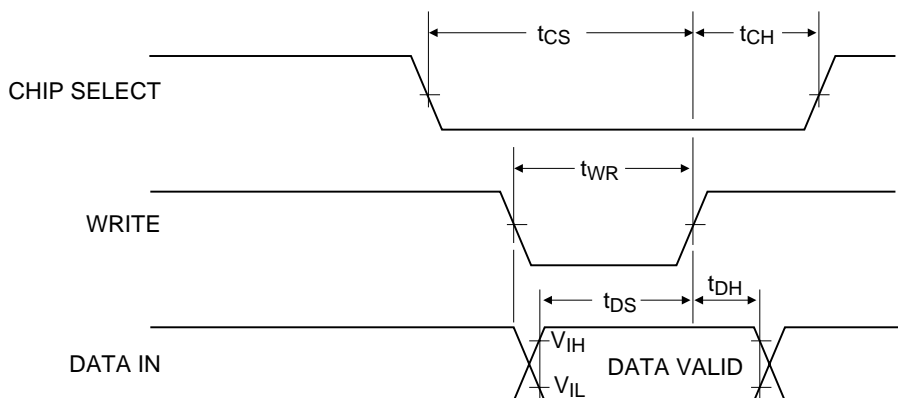
The **SP7545** is a low-cost, high stability 12-bit CMOS multiplying DAC with on-board data latches. The level-triggered latch accepts a single 12-bit wide data word under control of both CHIP SELECT ( $\overline{CS}$ ) and WRITE ( $\overline{WR}$ ) control line inputs. Tying both of these control lines low makes the input latch transparent, allowing direct, unbuffered operation of the DACs. The **SP7545** is ideally suited for applications requiring stability over time and temperature, such as digital gain blocks, attenuation control, robotics, modems, medical and process instrumentation. Because of its low power dissipation, it is also suited for battery-powered equipment.

The **SP7545** is constructed using a proprietary low-TCR thin-film process that requires no

laser-trimming to achieve 12-bit performance. With no laser-trimming, inherent high stability, and a segmented (decoded) DAC architecture, the **SP7545** retains its performance over time and temperature. To further improve reliability, the DAC features 2KV ESD protection on all digital inputs. Each DAC is fully characterized by all-codes testing to eliminate any hidden errors.

The **SP7545** is available for use in commercial and industrial temperature ranges. It operates with power supply voltages from +5V to +15V. It is available in 20-pin plastic DIP and PLCC packages.

## TIMING



### WRITE MODE:

$\overline{CS}$  and  $\overline{WR}$  low, DAC responds to DATA INPUTS ( $D_0$ – $D_{11}$ ).

### HOLD MODE:

Either  $\overline{CS}$  or  $\overline{WR}$  high, DATA INPUTS are locked out; DAC holds last data present when either  $\overline{CS}$  or  $\overline{WR}$  was asserted high.

## AC DYNAMICS

( $T_A=25^\circ\text{C}$ ;  $V_{DD}=+5\text{V}$  or  $+15\text{V}$  as noted,  $V_{REF}=+10\text{V}$ ;  $I_{O1}=AGND=GND=0\text{V}$ ; unipolar unless otherwise noted.)

| PARAMETER                                  | MIN. | TYP. | MAX. | UNIT | CONDITIONS  |
|--|------|------|------|------|---|
|  |      |      |      |      | Refer to Timing Diagram<br>$t_{CS} \geq t_{WR}$ ; $t_{CH} \geq 0$ |
| $t_{CS}$ — Chip Select to Write Setup Time | 280  | 200  | 380  | ns   | $V_{DD}=+5\text{V}$   |
|  |      |      |      | ns   | $V_{DD}=+5\text{V}$ ; from $T_{MIN}$ to $T_{MAX}$                 |
|  |      |      |      | ns   | $V_{DD}=+15\text{V}$  |
|  |      |      |      | ns   | $V_{DD}=+15\text{V}$ ; from $T_{MIN}$ to $T_{MAX}$                |
| $t_{CH}$ — Chip Select to Write Hold Time  | 0    |      |      | ns   | From $T_{MIN}$ to $T_{MAX}$                                       |
| $t_{WR}$ — Write Pulse Width               | 250  | 175  | 400  | ns   | $V_{DD}=+5\text{V}$   |
|  |      |      |      | ns   | $V_{DD}=+5\text{V}$ ; from $T_{MIN}$ to $T_{MAX}$                 |
|  |      |      |      | ns   | $V_{DD}=+15\text{V}$  |
|  |      |      |      | ns   | $V_{DD}=+15\text{V}$ ; from $T_{MIN}$ to $T_{MAX}$                |
| $t_{DS}$ — Data Setup Time                 | 140  | 100  | 210  | ns   | $V_{DD}=+5\text{V}$   |
|  |      |      |      | ns   | $V_{DD}=+5\text{V}$ ; from $T_{MIN}$ to $T_{MAX}$                 |
|  |      |      |      | ns   | $V_{DD}=+15\text{V}$  |
|  |      |      |      | ns   | $V_{DD}=+15\text{V}$ ; from $T_{MIN}$ to $T_{MAX}$                |
| $t_{DH}$ — Data Hold Time                  |      | 10   |      | ns   |   |

## ORDERING INFORMATION

| Model                                | Integral Linearity | Package                  |
|--------------------------------------|--------------------|--------------------------|
| 0°C to +70°C Operating Temperature   |                    |                          |
| SP7545JCN .....                      | ±2LSB .....        | 20-pin, 0.3" Plastic DIP |
| SP7545JCL .....                      | ±2LSB .....        | 20-pin PLCC              |
| SP7545KCN .....                      | ±1LSB .....        | 20-pin, 0.3" Plastic DIP |
| SP7545KCL .....                      | ±1LSB .....        | 20-pin PLCC              |
| -40°C to +85°C Operating Temperature |                    |                          |
| SP7545JIN .....                      | ±2LSB .....        | 20-pin, 0.3" Plastic DIP |
| SP7545JIL .....                      | ±2LSB .....        | 20-pin PLCC              |
| SP7545KIN .....                      | ±1LSB .....        | 20-pin, 0.3" Plastic DIP |
| SP7545KIL .....                      | ±1LSB .....        | 20-pin PLCC              |



SIGNAL PROCESSING EXCELLENCE

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