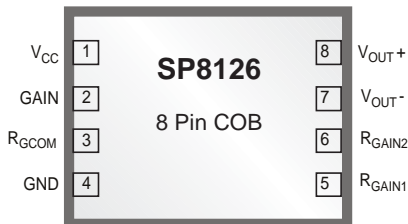


## High Speed Differential APC Amplifier

### FEATURES

- Dual Wavelength
- Slew Rate of 250V/ $\mu$ s
- Fast Settling Time - 7ns
- Gain Control
- 2V Output Swing
- Low Offset Voltage: < 10mV
- Low Offset Drift: < 20 $\mu$ V/ $^{\circ}$ C
- 12dB External Gain Adjust Range



### APPLICATIONS

- DVDRW
- DVDROM
- CDRW

### DESCRIPTION

The SP8126 is a high-speed, differential output APC amplifier that integrates the photodiode and adjustable gain block on one chip. Independent gain control allows individual adjustment for 780nm and 650nm wavelength operation, as found in CD/DVD optical storage drives. This allows the user to control the laser power of the system in high-speed DVDRW, DVDROM and CDRW systems. The wide 2V output swing also allows better system performance, through improved dynamic range.

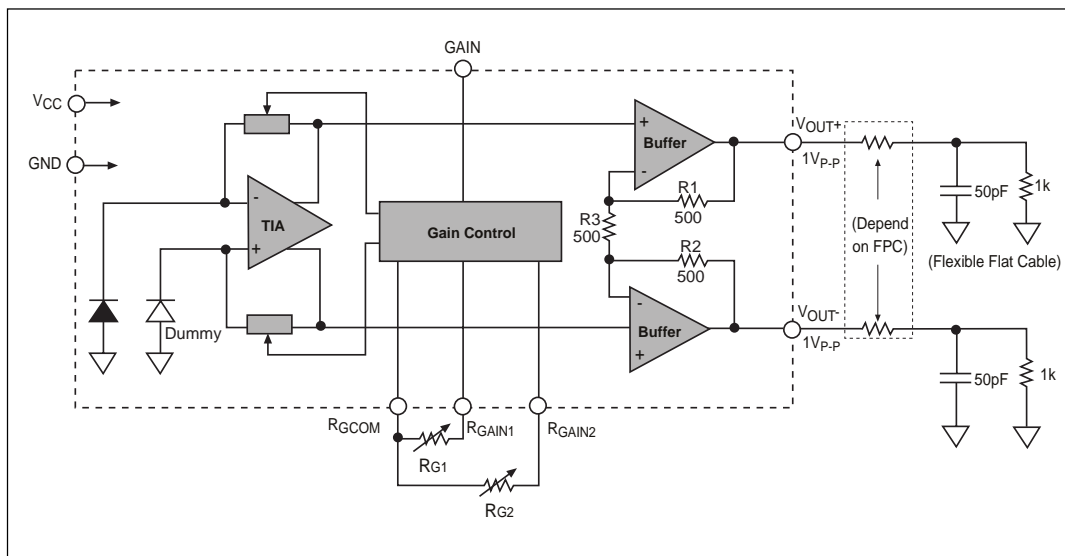


Figure 1. Functional Diagram and Typical Application

## ABSOLUTE MAXIMUM RATINGS

$T_{J(MAX)}$  ..... 120°C  
 $V_{S(MAX)}$  ..... 6V  
 $V_{IN(MAX)}$  ..... 6V

### Power Supply Voltage

Continuous Power Dissipation ( $T_{AMB} = 70^{\circ}C$ )

COB (derate 13.3mW/°C above +70°C) ..... 90mW

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## ELECTRICAL SPECIFICATIONS

Unless otherwise noted:  $V_{CC} = 5.0V$ ,  $C_{LOAD} = 50pF$  to GND,  $R_{LOADP} = R_{LOADN} = 1k\Omega$  to GND,  $R_{GAIN} = 510\Omega$  (Nominal Gain),  $-20^{\circ}C \leq T_A \leq +85^{\circ}C$ , Output measured differentially.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.5	5	5.5	V
Output Sensitivity	Laser Beam Diameter = 0.70mm, uniform density	2400	3000	3600	V/W
Input Optical Power Required to Produce 2V Output Swing		533	666	800	$\mu W$
Full Scale Linear Output Voltage Swing		2	2.8		V
Output Common Mode Voltage		2.3	2.5	2.7	V
	$4.5V < V_{CC} < 5.5V$	$V_{CC}/2.2$	$V_{CC}/2$	$V_{CC}/1.8$	V
Output Offset Voltage		-10	0.5	10	mV
	$R_{GAIN} = 1230\Omega$ (High Gain)	-20	1.0	20	mV
Output Offset Voltage Drift		-25	-11	25	$\mu V/C$
	$R_{GAIN} = 1230\Omega$ (High Gain)	-50	-13	50	$\mu V/C$
Output Noise	BW = 100MHz		1.6	2	mVrms
	BW = 100MHz, $R_{GAIN} = 1230\Omega$ (High Gain)		2.4	5	mVrms
Bandwidth	-3dB	70	100		MHz
	-3dB, $R_{GAIN} = 1230\Omega$ (High Gain)	50	68		MHz
PSRR	$4.5V < V_{CC} < 5.5V$	55	76		dB
	$4.5V < V_{CC} < 5.5V$ , $R_{GAIN} = 1230\Omega$ (High Gain)	50	73		dB
Output Settling Time (1% of Final Value)	$2V_{PP}$ Step		7	10	ns
	$2V_{PP}$ Step, $R_{GAIN} = 1230\Omega$ (High Gain)		12	15	ns
Output Slew Rate		200	300		V/ $\mu s$
Output Overshoot	$2V_{PP}$ Step			5	%

## ELECTRICAL SPECIFICATIONS: Continued

Unless otherwise noted:  $V_{CC} = 5.0V$ ,  $C_{LOAD} = 50pF$  to GND,  $R_{LOADP} = R_{LOADN} = 1k\Omega$  to GND,  $R_{GAIN} = 510\Omega$  (Nominal Gain),  $-20^{\circ}C \leq T_A \leq +85^{\circ}C$ , Output measured differentially.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current			15		mA
	$-20^{\circ}C < T_A < +85^{\circ}C$			20	mA
Gain Adjust Range	$215\Omega < R_{GAIN} < 1230\Omega$	-6		6	dB
Gain Select Input Voltage VIL (TTL Level)				0.8	V
Gain Select Input Voltage VIH (TTL Level)		2.0			V

## PIN DESCRIPTION

PIN NUMBER	NAME	FUNCTION
1	$V_{CC}$	Supply Voltage
2	GAIN	Gain Select
3	$R_{GCOM}$	Common connection point for $R_{GAIN1}$ and $R_{GAIN2}$
4	GND	Power Ground
5	$R_{GAIN1}$	Gain Adjust 1 (Gain Select = LOW) or OPEN
6	$R_{GAIN2}$	Gain Adjust 2 (Gain Select = HIGH)
7	$V_{OUT-}$	Output Voltage -
8	$V_{OUT+}$	Output Voltage +

## THEORY OF OPERATION

### Internal Operation

The SP8126 APC circuit has an integrated photo detector and is designed with nominal sensitivities of  $3mV/\mu W$  for both 650nm and 780nm wavelength laser light. The part's sensitivity can also be adjusted continuously and independently for two different gain modes via two external resistors over a range of  $\pm 6dB$ . The two gain modes are controlled by a TTL compatible logic input, called GAIN SELECT. This logic pin selects between the two external gain setting resistors to allow independent control and settings for the two gain functions.

The system is a two stage design, consisting of a Trans-Impedance Amplifier (TIA) and an output buffer stage. In dark condition the outputs  $V_{OUT-}$  and  $V_{OUT+}$  are set to a reference voltage

that is defined internally as  $V_{CC}/2$ . With 650nm or 780nm wavelength laser light falling on the photodetector, the output will swing differentially around  $V_{CC}/2$  proportional with the light power according to the chosen gain.

### TIA and Gain control

The first stage is a differential TIA used to convert the photodetector current to a balanced differential voltage. The traditional fixed feedback resistors have been replaced with an active resistor circuit that sets the trans-impedance value.

A Resistor Control Block that senses the value of the external gain setting resistor controls the value of the equivalent feedback resistor.

The  $\pm 6\text{dB}$  Gain adjustment is therefore done directly in the TIA, by adjusting the active feedback blocks proportional with the gain setting resistor. The external resistor is not directly in the signal path, and therefore any parasitic from the off-chip connections does not affect the signal quality. The value of the active feedback is controlled tightly over supply and temperature changes through a Control Block with active feedback circuitry.

Gain control is proportional with the external resistor, so the lowest value of  $R_{\text{GAIN}}$  will produce the  $-6\text{dB}$  gain adjustment and the highest value will produce the  $+6\text{dB}$  gain adjustment. Please consult the specification table for the required  $R_{\text{GAIN}}$  values.

### Buffer

This stage buffers the differential signal from the TIA to the  $V_{\text{OUT}}$  pins and refers the signal to the internal reference voltage. A balanced current feedback amplifier is used for this purpose to achieve high slew rate and fast settling.

The buffer is designed to drive high capacitive loads. The maximum load is  $50\text{pF}$  bulk. The actual load is typically a flexible printed circuit (FPC) that acts like a transmission line. This presents a distributed capacitive load plus inductance and resistance. In this case care should be taken to match the characteristic impedance of the line at the far end to avoid standing waves and ringing. The buffer is designed to drive  $1\text{k}\Omega$  to ground. However, this resistor can be adjusted in value to accommodate the characteristic impedance of the signal trace. The output buffer amplifier is designed to be stable without load and with loads up to  $50\text{pF}$  lumped capacitance.

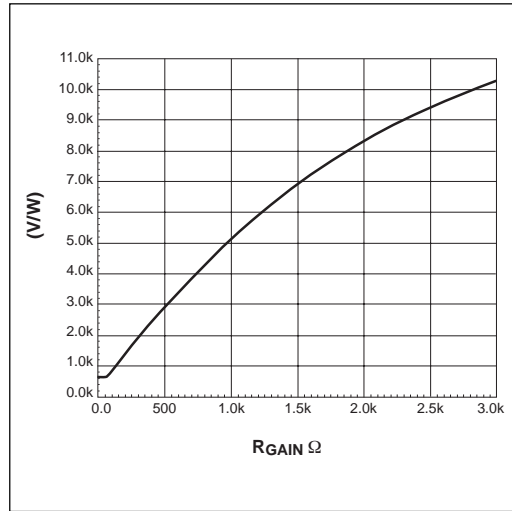


Figure 2. Sensitivity

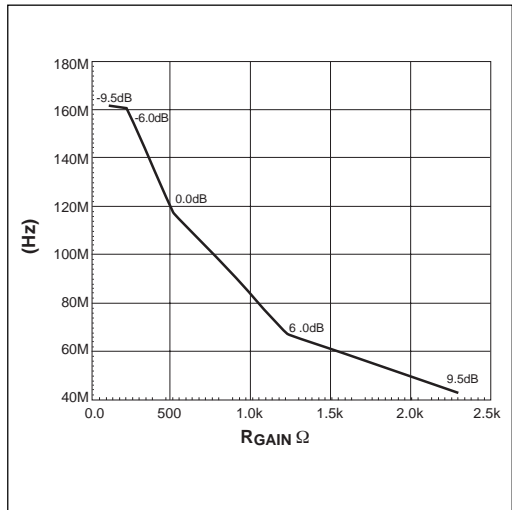


Figure 3. SP8126 Bandwidth versus  $R_{\text{GAIN}}$

**TABLE 1: APC SYSTEM GUARANTEED AND TARGET GAIN SET POINTS.**

$V_{\text{OUTP}} - V_{\text{OUTN}} = 2V_{\text{P-P}}$ ,  $V_{\text{CC}} = 5\text{V}$ ,  $T = 27^\circ\text{C}$

Gain (dB)	Sensitivity (V/W)	$R_{\text{GAIN}} \ (\Omega)$	$T_s \ 1\% \ (\text{nS})$	BW (MHz)	Pin ( $\mu\text{W}$ )	Specification
+9.5	9000	2300	14	45	223	Target
+6	6000	1230	10	68	335	Guaranteed
0	3000	510	7	119	666	Guaranteed
-6	1500	215	5.5	160	1331	Guaranteed
-9.5	1000	125	5	162	1988	Target

## LAYOUT AND ROUTING CONSIDERATIONS

A major consideration in developing the optical pick-up head system is the extremely small form factor, which is additionally aggravated by the physical locations required by the light path.

Special care must be taken when designing the Flex or PCB for this part. The output peak current requirement is in the order of 12.5mA when driving 50pF of capacitive load with a slew rate of 250V/ $\mu$ s. Therefore care must be taken to provide low inductance, low resistance paths for power and ground and output traces.

Supply coupling is also very important. Good supply decoupling is important to ensure the high frequency performance of the system by eliminating supply lead inductance effects. The decoupling capacitor C1, as shown in Figure 5, should be as close to the part as possible. This

capacitor should be 0.1 $\mu$ F ceramic. C2 is optional to improve decoupling and is recommended to be 1 $\mu$ F tantalum. The layout of the PCB is pictured here. Note the wide and short traces on the supply lines.

The traces for the gain resistors  $R_{GAIN1}$  and  $R_{GAIN2}$  are kept as short as possible to avoid excessive parasitics. Any parasitics on these nodes will limit the performance of the system.  $R_{GAIN1}$  and  $R_{GAIN2}$  are subminiature potentiometers in the application. This is a single layer board using FR4 material.

In order to minimize coupling capacitance into the gain setting resistor nodes, it is also critical that  $V_{OUT+}$  and  $V_{OUT-}$  are routed away from the traces associated with the gain-setting resistors.

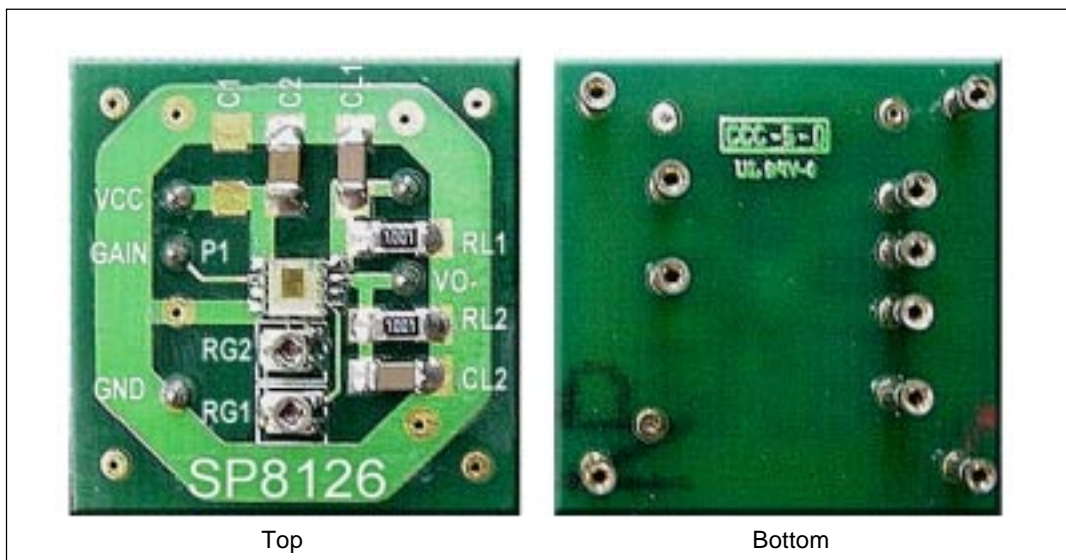
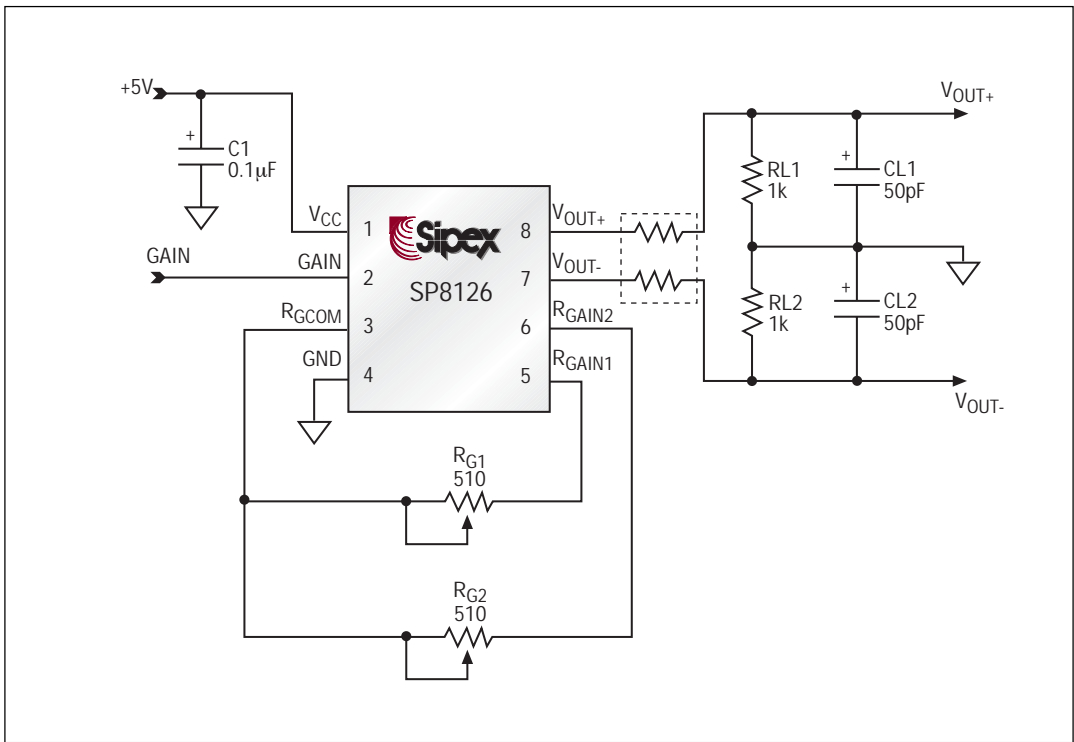
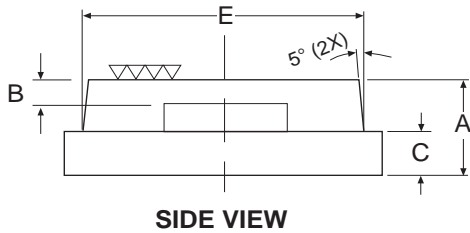
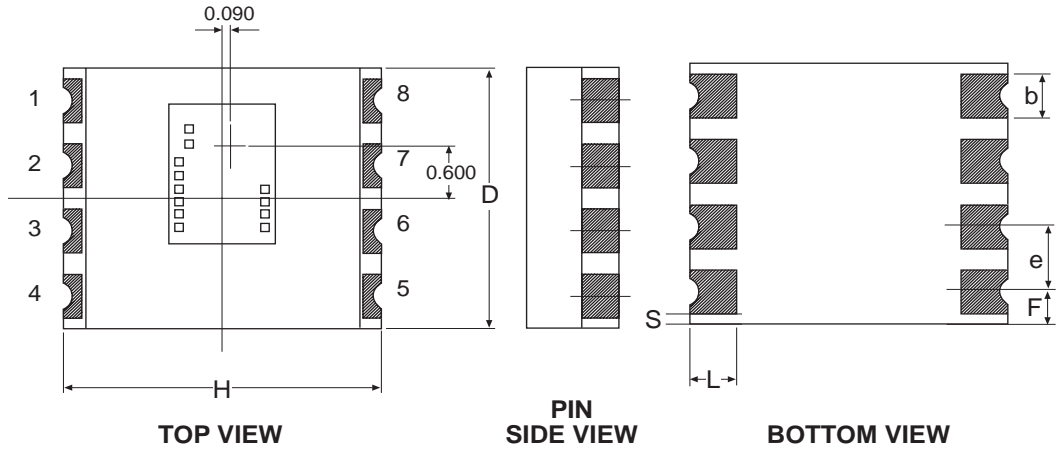


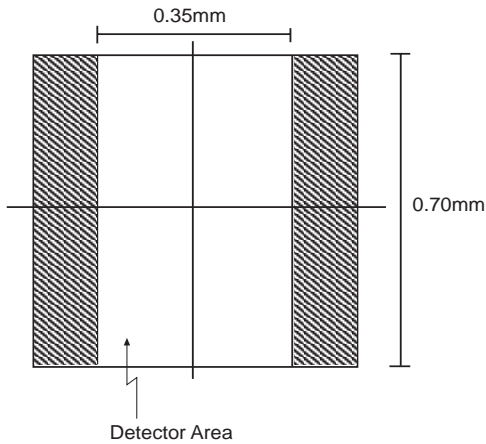
Figure 4. Test and Evaluation PCB Layout for COB 8 Lead Package



**Figure 5. Test and Evaluation Schematic**



#### DETECTOR SIZE



DIMENSIONS in mm Minimum/Maximum	8-PIN COB
A	0.90/1.10
B	.127/.33
b	0.30/0.50
c	0.50 nom
D	2.90/3.10
E	3.00/3.20
e	0.75 nom
H	3.40/3.60
L	0.40/0.60
F	0.28/0.48
S	0.075/0.275

**8 PIN COB**  
**(3.5mm x 3.0mm)**

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## ORDERING INFORMATION

Part Number	Temperature Range	Package Type
SP8126 .....	-20°C to +85°C .....	8 lead COB (3.0mm x 3.5mm)
SP8126EB .....	-20°C to +85°C .....	8 lead COB (3.0mm x 3.5mm)



ANALOG EXCELLENCE

**Sipex Corporation**

**Headquarters and  
Sales Office**  
233 South Hillview Drive  
Milpitas, CA 95035  
TEL: (408) 934-7500  
FAX: (408) 935-7600

**Sales Office**  
22 Linnell Circle  
Billerica, MA 01821  
TEL: (978) 667-8700  
FAX: (978) 670-9001  
e-mail: sales@sipex.com

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