

1. DESCRIPTION

The ST8024 is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The ST8024 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

2. FEATURES

- Number of LCD drive outputs: 240
- Supply voltage for LCD drive: +15.0 to +42.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

Package: 269-pin TCP (Tape Carrier Package)

(Segment mode)

- Shift clock frequency
 - 20 MHz (MAX.): $V_{DD} = +5.0 \pm 0.5$ V
 - 15 MHz (MAX.): $V_{DD} = +3.0$ to $+4.5$ V
 - 12 MHz (MAX.): $V_{DD} = +2.5$ to $+3.0$ V
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data

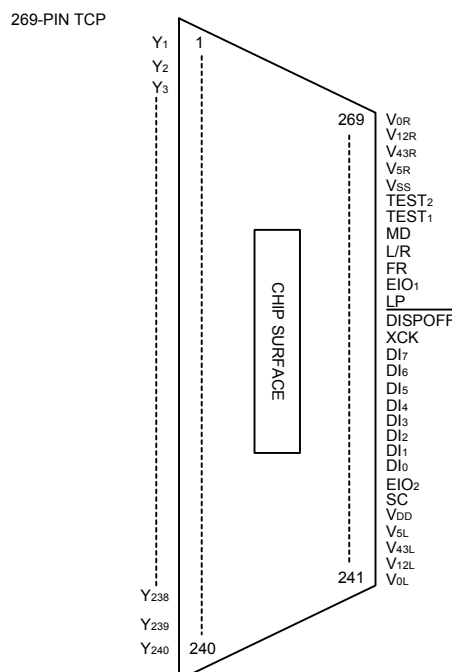
- Line latch circuits are reset when $\overline{\text{DISPOFF}}$ active (Common mode)
- Shift clock frequency: 4 MHz (MAX.)
- Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
- Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)

- Y1->Y240 Single mode
- Y240->Y1 Single mode
- Y1->Y120, Y121->Y240 Dual mode
- Y240->Y121, Y120->Y1 Dual mode

The above 4 shift directions are pin-selectable

- Shift register circuits are reset when $\overline{\text{DISPOFF}}$ active

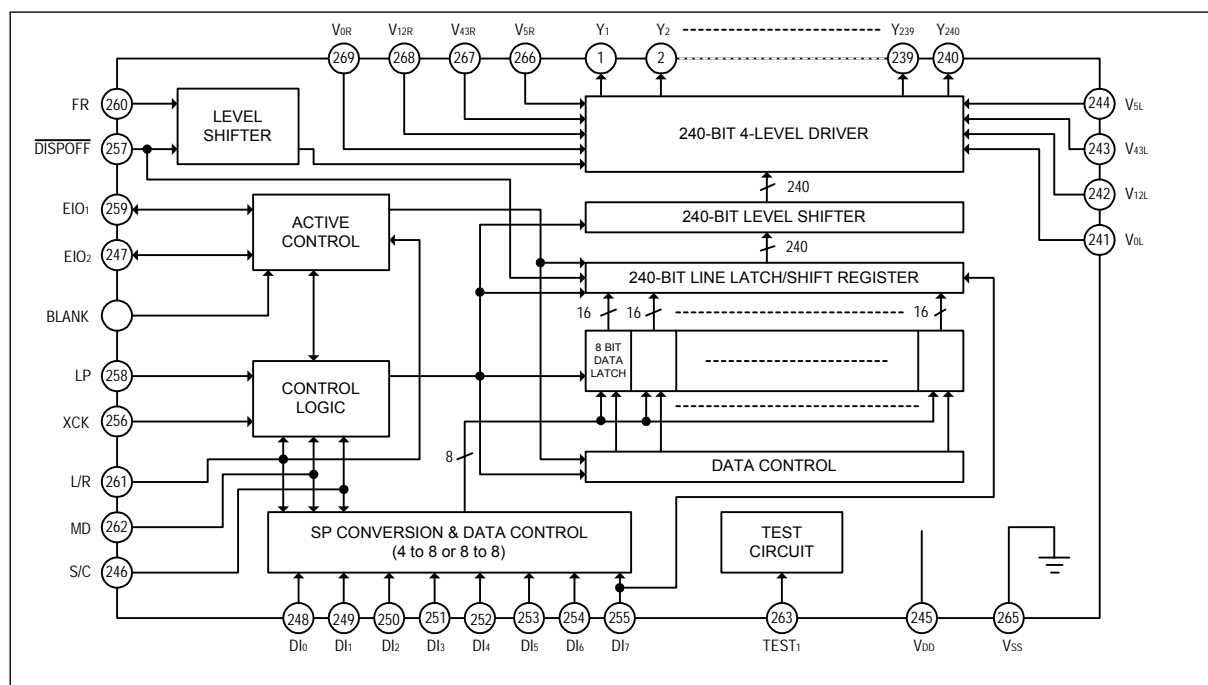
3. PIN CONNECTIONS



4. PIN DESCRIPTION (TCP)

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 ~ 240	Y ₁ -Y ₂₄₀	0	LCD drive output
241, 269	V _{OL} , V _{OR}	-	Power supply for LCD drive
242, 268	V _{12L} , V _{12R}	-	Power supply for LCD drive
243, 267	V _{43L} , V _{43R}	-	Power supply for LCD drive
244, 266	V _{5L} , V _{5R}	-	Power supply for LCD drive
245	V _{DD}	-	Power supply for logic system (+2.5 to +5.5 V)
246	S/C	I	Segment mode/common mode selection
247, 259	EIO ₂ , EIO ₁	I/O	Input/output for chip selection at segment mode Shift data input/output for shift register at common mode
248 ~ 254	DI ₀ -DI ₆	I	Display data input at segment mode
255	DI ₇	I	Display data input at segment mode/Dual mode data input at common mode
256	XCK	I	Clock input for taking display data at segment mode
257	/DISPOFF	I	Control input for output of non-select level
258	LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
260	FR	I	AC-converting signal input for LCD drive waveform
261	L/R	I	Input for selecting the reading direction of display data at segment mode/ Input for selecting the shift direction of shift register at common mode
262	MD	I	Mode selection input
263	TEST ₁	I	Test mode selection pins During normal operation, fix to V _{SS} level "L".
265	V _{SS}	-	Ground (0 V)

5. BLOCK DIAGRAM



6. FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 30 sets of 8 bits.
Line Latch/Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V ₀ , V ₁₂ , V ₄₃ or V ₅) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.
Test Circuit	The circuit for testing. During normal operation, it isn't activated.

INPUT/OUTPUT CIRCUITS

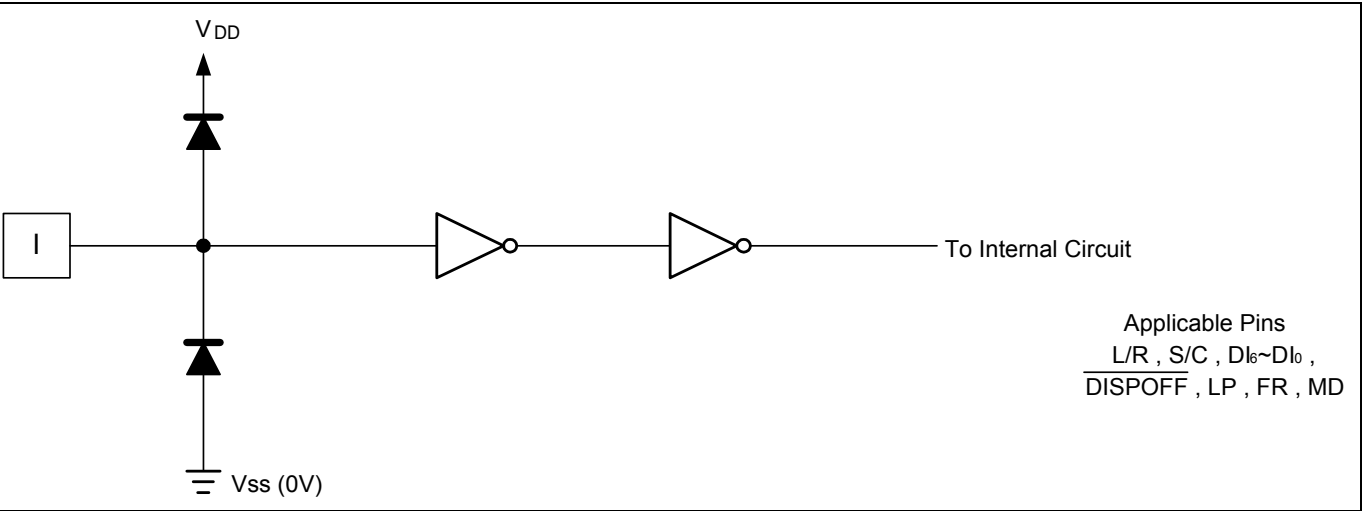


Fig. 1 Input Circuit (1)

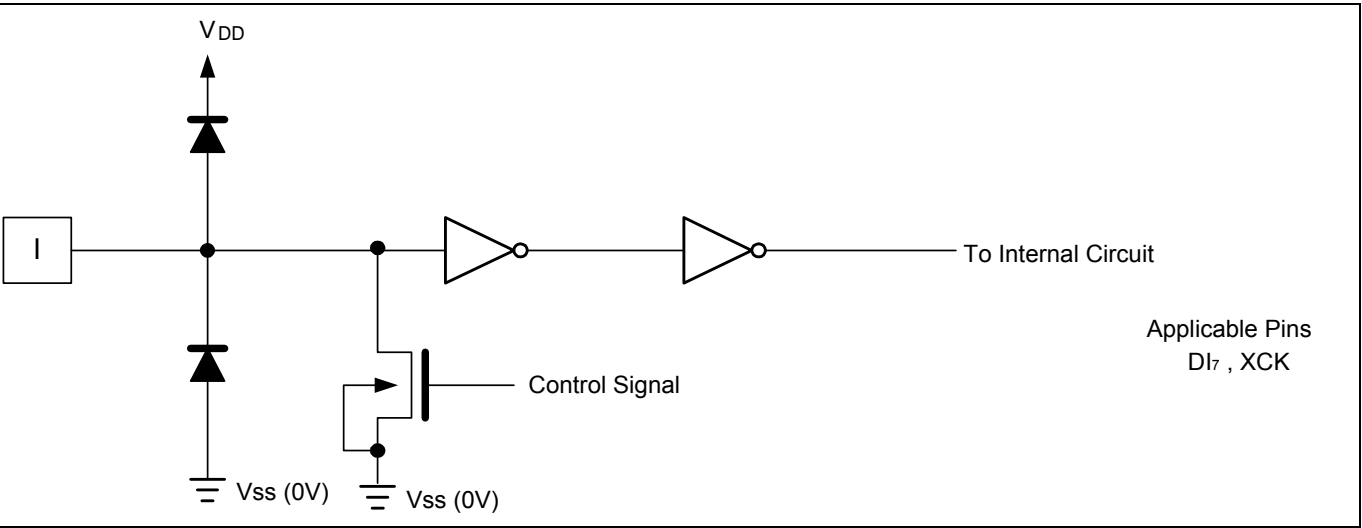


Fig. 2 Input Circuit (2)

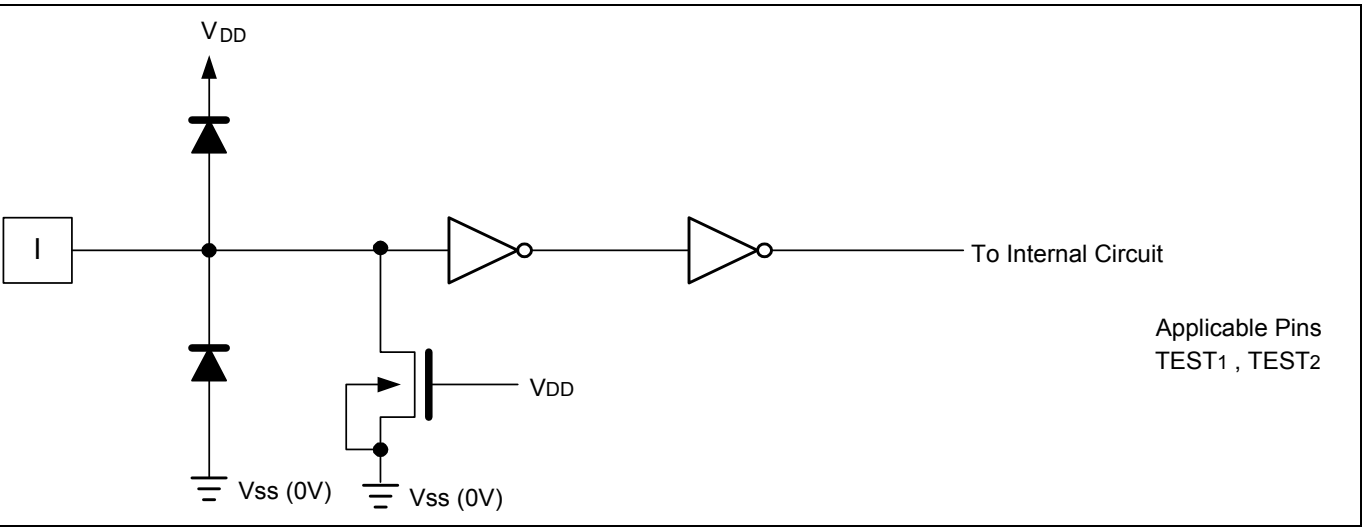


Fig. 3 Input Circuit (3)



7. FUNCTIONAL DESCRIPTION

7.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V _{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V _{SS}	Ground pin, connected to 0 V.
V _{OL} , V _{OR} V _{12L} , V _{12R} V _{43L} , V _{43R} V _{5L} , V _{5R}	Bias power supply pins for LCD drive voltage <ul style="list-style-type: none"> • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0, 12, 43, 5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI ₇ -DI ₀	Input pins for display data <ul style="list-style-type: none"> • In 4-bit parallel input mode, input data into the 4 pins, DI₃-DI₀. Connect DI₇-DI₄ to V_{SS} or V_{DD}. • In 8-bit parallel input mode, input data into the 8 pins, DI₇-DI₀. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data <ul style="list-style-type: none"> * Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data <ul style="list-style-type: none"> • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data <ul style="list-style-type: none"> • When set to V_{SS} level "L", data is read sequentially from Y₂₄₀ to Y₁. • When set to V_{DD} level "H", data is read sequentially from Y₁ to Y₂₄₀. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y₁-Y₂₄₀) are set to level V_{SS}. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of DISPOFF. When the DISPOFF function is canceled, the driver outputs non-select level (V₁₂ or V₄₃), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin <ul style="list-style-type: none"> • When set to V_{SS} level "L", 8-bit parallel input mode is set. • When set to V_{DD} level "H", 4-bit parallel input mode is set. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
S/C	Segment mode/common mode selection pin <ul style="list-style-type: none"> • When set to V_{DD} level "H", segment mode is set.
EIO ₁ , EIO ₂	Input/output pins for chip selection <ul style="list-style-type: none"> • When L/R input is at V_{SS} level "L", EIO₁ is set for output, and EIO₂ is set for input. • When L/R input is at V_{DD} level "H", EIO₁ is set for input, and EIO₂ is set for output. • During output, set to "H" while LP • XCK is "H" and after 240 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read.
TEST ₁	Test mode selection pins <ul style="list-style-type: none"> • During normal operation, fix to V_{SS} level "L". •

Y ₁ -Y ₂₄₀	LCD drive output pins <ul style="list-style-type: none"> Corresponding directly to each bit of the data latch, one level (V₀, V₁₂, V₄₃, or V₅) is selected and output. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
DBLKB	Use as contrast control, use PWM signal as input. Connect to V _{DD} for no contrast control

(Common mode)

SYMBOL	FUNCTION
V _{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V _{SS}	Ground pin, connected to 0 V.
V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R} V _{5L} , V _{5R}	Bias power supply pins for LCD drive voltage <ul style="list-style-type: none"> Normally use the bias voltages set by a resistor divider. Ensure that voltages are set such that V_{SS} ≤ V₅ < V₄₃ < V₁₂ < V₀. V_{iL} and V_{iR} (i = 0, 12, 43, 5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
EIO ₁	Shift data input/output pin for bi-directional shift register <ul style="list-style-type: none"> Output pin when L/R is at V_{SS} level "L", input pin when L/R is at V_{DD} level "H". When L/R = H, EIO₁ is used as input pin, it will be pulled down. When L/R = L, EIO₁ is used as output pin, it won't be pulled down. Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
EIO ₂	Shift data input/output pin for bi-directional shift register <ul style="list-style-type: none"> Input pin when L/R is at V_{SS} level "L", output pin when L/R is at V_{DD} level "H". When L/R = L, EIO₂ is used as input pin, it will be pulled down. When L/R = H, EIO₂ is used as output pin, it won't be pulled down. Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
LP	Shift clock pulse input pin for bi-directional shift register <ul style="list-style-type: none"> * Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register <ul style="list-style-type: none"> Data is shifted from Y₂₄₀ to Y₁ when set to V_{SS} level "L", and data is shifted from Y₁ to Y₂₄₀ when set to V_{DD} level "H". Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level <ul style="list-style-type: none"> The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to V_{SS} level "L", the LCD drive output pins (Y₁-Y₂₄₀) are set to level V_{SS}. When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V₁₂ or V₄₃), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform <ul style="list-style-type: none"> The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin <ul style="list-style-type: none"> When set to V_{SS} level "L", single mode operation is selected; when set to V_{DD} level "H" dual mode operation is selected. Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
DI ₇	Dual mode data input pin <ul style="list-style-type: none"> According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI₇ will be pulled down. When the chip is used in single mode, DI₇ won't be pulled down. Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.

S/C	Segment mode/common mode selection pin • When set to V_{SS} level "L", common mode is set.
DI ₆ -DI ₀	Not used • Connect DI ₆ -DI ₀ to V_{SS} or V_{DD} , avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} or open.
TEST ₁	Test mode selection pins • During normal operation, fix to V_{SS} level "L".
Y ₁ -Y ₂₄₀	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0 , V_{12} , V_{43} , or V_5) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
DBLKB	Use as contrast control, use PWM signal as input. Connect to V_{DD} for no contrast control

7.2 Functional Operations

7.2.1 TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

NOTES:

- $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$: V_{SS} (0 V), H V_{DD} (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

Supply regular voltage which is assigned by specification for each power pin.

7.2.2 RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					60 CLOCK	59 CLOCK	58 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI ₀	Y ₁	Y ₅	Y ₉	...	Y ₂₂₉	Y ₂₃₃	Y ₂₃₇
				DI ₁	Y ₂	Y ₆	Y ₁₀	...	Y ₂₃₀	Y ₂₃₄	Y ₂₃₈
				DI ₂	Y ₃	Y ₇	Y ₁₁	...	Y ₂₃₁	Y ₂₃₅	Y ₂₃₉
				DI ₃	Y ₄	Y ₈	Y ₁₂	...	Y ₂₃₂	Y ₂₃₆	Y ₂₄₀
H	H	Input	Output	DI ₀	Y ₂₄₀	Y ₂₃₆	Y ₂₃₂	...	Y ₁₂	Y ₈	Y ₄
				DI ₁	Y ₂₃₉	Y ₂₃₅	Y ₂₃₁	...	Y ₁₁	Y ₇	Y ₃
				DI ₂	Y ₂₃₈	Y ₂₃₄	Y ₂₃₀	...	Y ₁₀	Y ₆	Y ₂
				DI ₃	Y ₂₃₇	Y ₂₃₃	Y ₂₂₉	...	Y ₉	Y ₅	Y ₁

(b) 8-bit Parallel Input Mode

MD	L/R	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI ₀	Y ₁	Y ₉	Y ₁₇	...	Y ₂₁₇	Y ₂₂₅	Y ₂₃₃
				DI ₁	Y ₂	Y ₁₀	Y ₁₈	...	Y ₂₁₈	Y ₂₂₆	Y ₂₃₄
				DI ₂	Y ₃	Y ₁₁	Y ₁₉	...	Y ₂₁₉	Y ₂₂₇	Y ₂₃₅
				DI ₃	Y ₄	Y ₁₂	Y ₂₀	...	Y ₂₂₀	Y ₂₂₈	Y ₂₃₆
				DI ₄	Y ₅	Y ₁₃	Y ₂₁	...	Y ₂₂₁	Y ₂₂₉	Y ₂₃₇
				DI ₅	Y ₆	Y ₁₄	Y ₂₂	...	Y ₂₂₂	Y ₂₃₀	Y ₂₃₈
				DI ₆	Y ₇	Y ₁₅	Y ₂₃	...	Y ₂₂₃	Y ₂₃₁	Y ₂₃₉
				DI ₇	Y ₈	Y ₁₆	Y ₂₄	...	Y ₂₂₄	Y ₂₃₂	Y ₂₄₀
L	H	Input	Output	DI ₀	Y ₂₄₀	Y ₂₃₂	Y ₂₂₄	...	Y ₂₄	Y ₁₆	Y ₈
				DI ₁	Y ₂₃₉	Y ₂₃₁	Y ₂₂₃	...	Y ₂₃	Y ₁₅	Y ₇
				DI ₂	Y ₂₃₈	Y ₂₃₀	Y ₂₂₂	...	Y ₂₂	Y ₁₄	Y ₆
				DI ₃	Y ₂₃₇	Y ₂₂₉	Y ₂₂₁	...	Y ₂₁	Y ₁₃	Y ₅
				DI ₀	Y ₂₃₆	Y ₂₂₈	Y ₂₂₀	...	Y ₂₀	Y ₁₂	Y ₄
				DI ₁	Y ₂₃₅	Y ₂₂₇	Y ₂₁₉	...	Y ₁₉	Y ₁₁	Y ₃
				DI ₂	Y ₂₃₄	Y ₂₂₆	Y ₂₁₈	...	Y ₁₈	Y ₁₀	Y ₂
				DI ₃	Y ₂₃₃	Y ₂₂₅	Y ₂₁₇	...	Y ₁₇	Y ₉	Y ₁

(Common Mode)

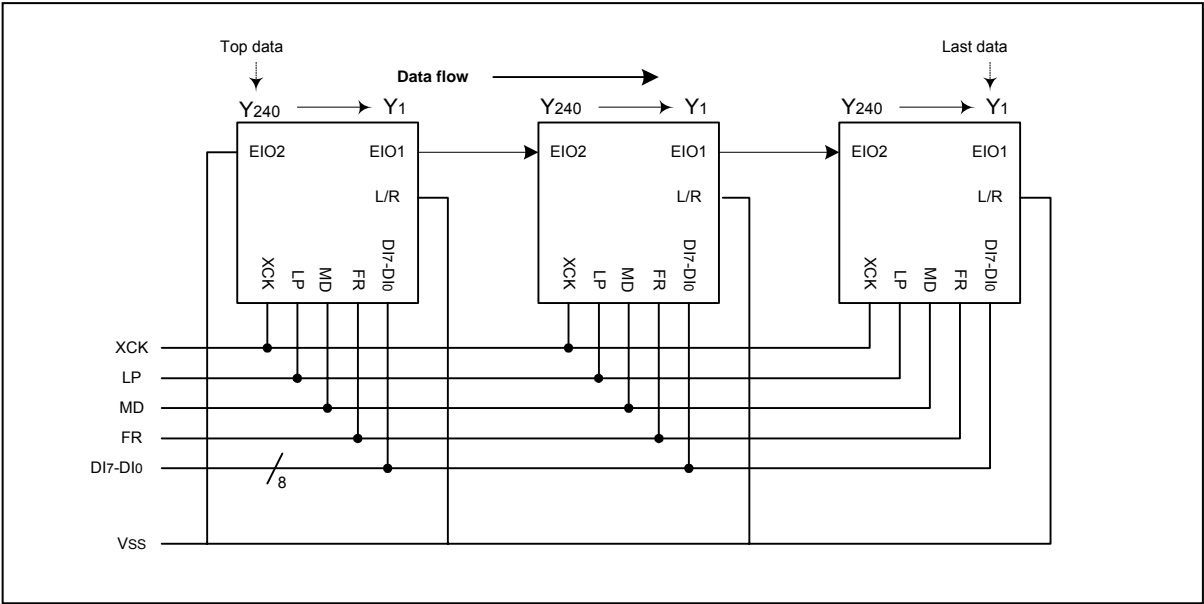
MD	L/R	DATA TRANSFER DIRECTION	EIO ₁	EIO ₂	DI ₇
L (Single)	L	Y ₂₄₀ → Y ₁	Output	Input	X
	H	Y ₁ → Y ₂₄₀	Input	Output	X
H (Dual)	L	Y ₂₄₀ → Y ₁₂₁	Output	Input	Input
		Y ₁₂₀ → Y ₁			
	H	Y ₁ → Y ₁₂₀	Input	Output	Input
		Y ₁₂₁ → Y ₂₄₀			

NOTES:

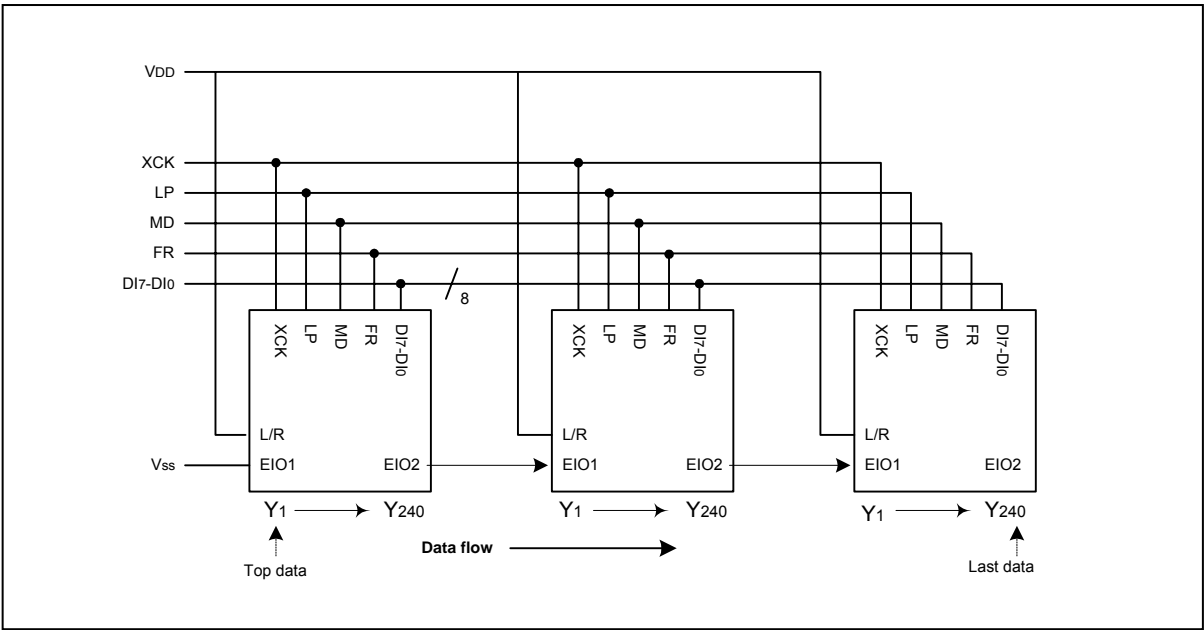
- L: V_{SS} (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

7.2.3 Connection examples of plural segment drivers

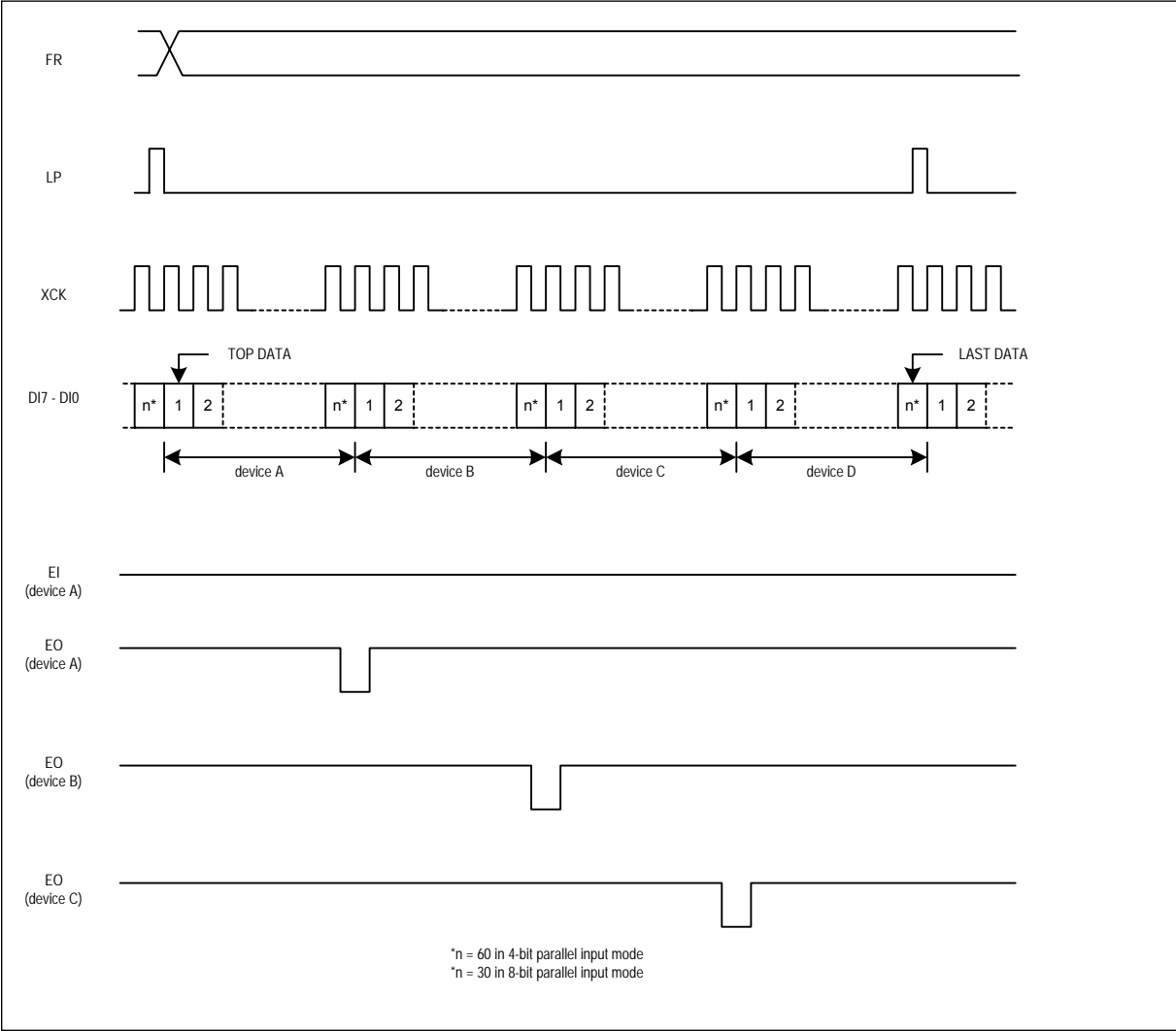
(c) When L/R = “L”



(d) When L/R = “H”

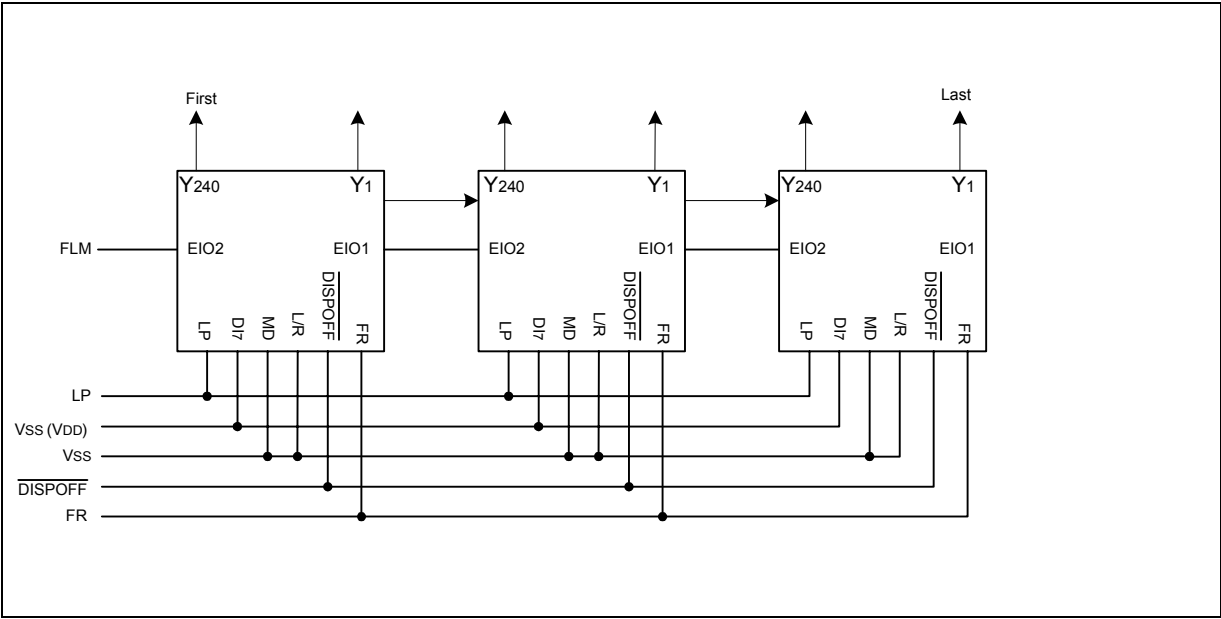


7.2.4 Timing chart of 4-device cascade connection of segment drivers

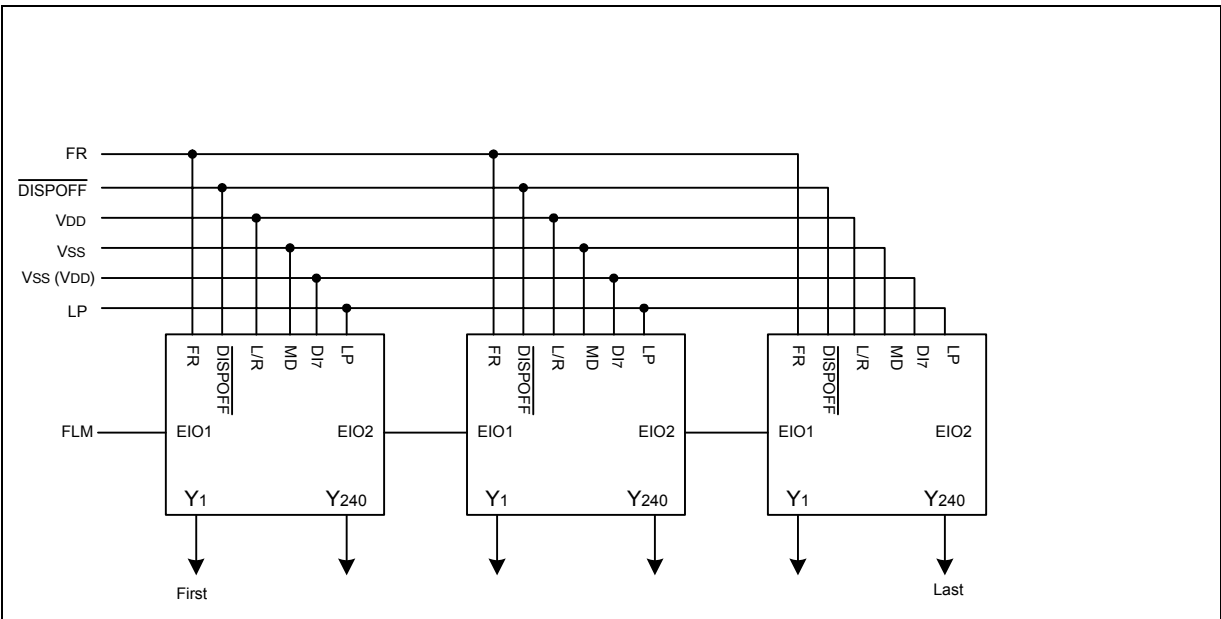


7.2.5 Connection examples for plural common drivers

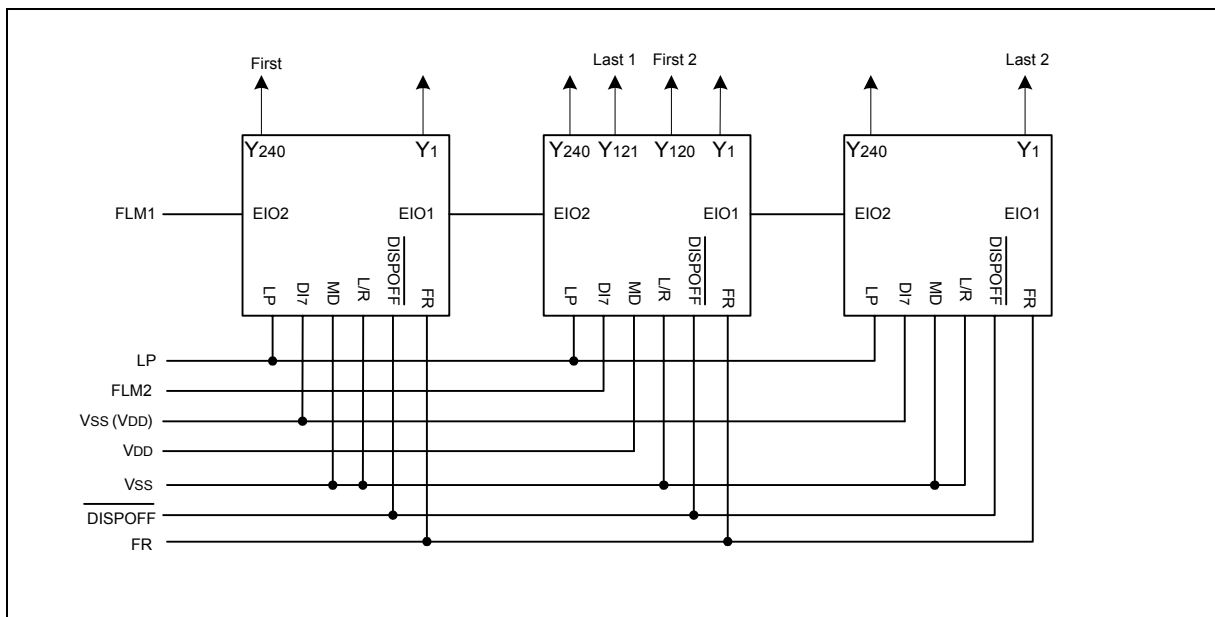
(e) Single Mode (L/R = "L")



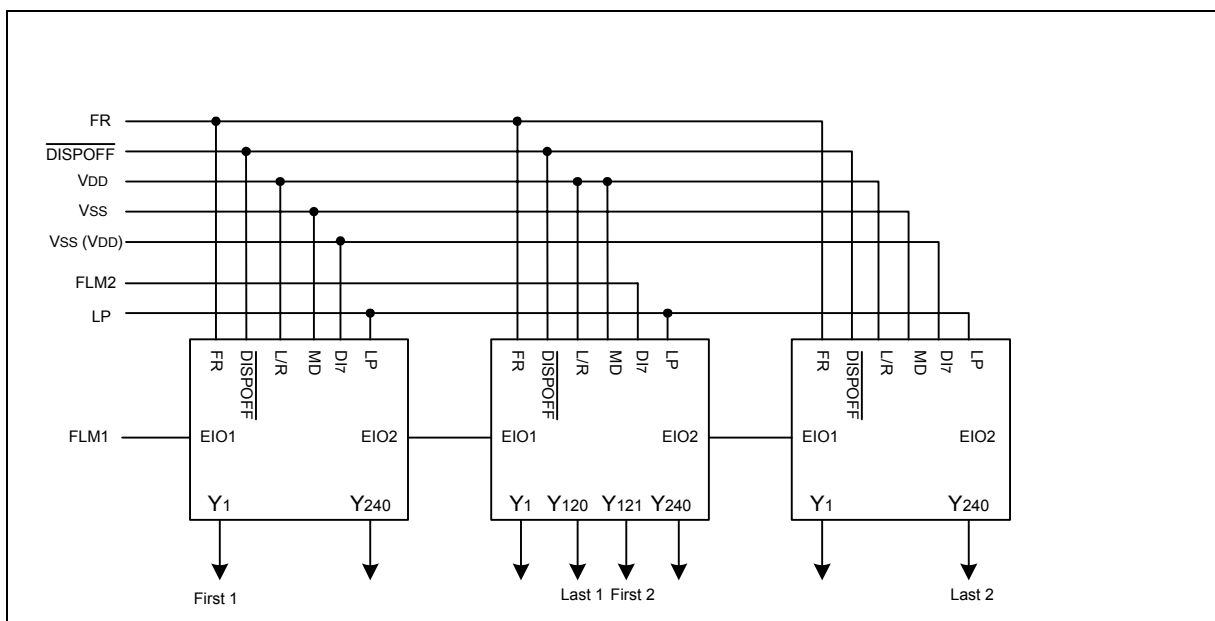
(f) Single Mode (L/R = "H")



(g) Dual Mode (L/R = "L")



(h) Dual mode (L/R = "H")



8. PRECAUTIONS

Precautions when connecting or disconnecting the power supply

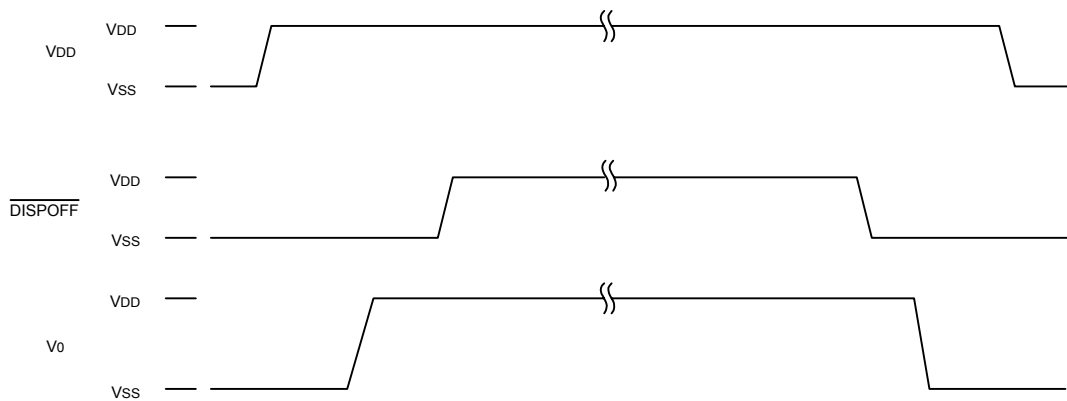
This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the

system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_s on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



9. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_0	V_{OL}, V_{OR}	-0.3 to +45.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to $V_0 + 0.3$	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to $V_0 + 0.3$	V	
	V_5	V_{SL}, V_{SR}	-0.3 to $V_0 + 0.3$	V	
Input voltage	V_I	D17-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF, TEST1	-0.3 to $V_{DD} + 0.3$	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. $T_A = +25\text{ °C}$
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

10. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{OL}, V_{OR}	+15.0		+42.0	V	
Operating temperature	T_{OPR}		-25		+85	°C	

NOTES:

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.

11. ELECTRICAL CHARACTERISTICS

11.1 DC Characteristics

(Segment Mode) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+5.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, LP, L/R FR,			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}		MD, S/C, EIO1, EIO2, DISPOFF	$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	$I_{OL} = +0.4\text{ mA}$	EIO1, EIO2			+0.4	V	
Output "High" voltage	V_{OH}	$I_{OH} = -0.4\text{ mA}$		$V_{DD}-0.4$			V	
Input leakage current	I_{LIL}	$V_i = V_{SS}$	DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO1, EIO2, DISPOFF			-10.0	μA	
	I_{LIH}	$V_i = V_{DD}$				+10.0	μA	
Output resistance	R_{ON}	$ \Delta V_{ON} = 0.5\text{ V}$	Y1-Y240		1.0	1.5	k Ω	
					1.5	2.0		
					2.0	2.5		
Standby current	I_{STB}		V_{SS}			75.0	μA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			12.0	mA	3
Supply current (3)	I_0		V_{OL}, V_{OR}			1.5	mA	4

NOTES:

- $V_{DD} = +5.0\text{ V}$, $V_0 = +42.0\text{ V}$, $V_i = V_{SS}$.
- $V_{DD} = +5.0\text{ V}$, $V_0 = +42.0\text{ V}$, $f_{XCK} = 20\text{ MHz}$, no-load, $EI = V_{DD}$. The input data is turned over by data taking clock (4-bit parallel input mode).
- $V_{DD} = +5.0\text{ V}$, $V_0 = +42.0\text{ V}$, $f_{XCK} = 20\text{ MHz}$, no-load, $EI = V_{SS}$. The input data is turned over by data taking clock (4-bit parallel input mode).
- $V_{DD} = +5.0\text{ V}$, $V_0 = +42.0\text{ V}$, $f_{XCK} = 20\text{ MHz}$, $f_{LP} = 41.6\text{ kHz}$, $f_{FR} = 80\text{ Hz}$, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+5.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, LP, L/R			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}		FR, MD, S/C, EIO1, EIO2, DISPOFF	$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	$I_{OL} = +0.4\text{ mA}$	EIO1, EIO2			+0.4	V	
Output "High" voltage	V_{OH}	$I_{OH} = -0.4\text{ mA}$		$V_{DD}-0.4$			V	
Input leakage current	I_{LIL}	$V_i = V_{SS}$	DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO1, EIO2, DISPOFF			-10.0	μA	
	I_{LIH}	$V_i = V_{DD}$	DI6-DI0, LP, L/R, FR, MD, S/C, DISPOFF			+10.0	μA	
Input pull-down current	I_{PD}	$V_i = V_{DD}$	DI7, XCK, EIO1, EIO2			100.0	μA	
Output resistance	R_{ON}	$ \Delta V_{ON} = 0.5\text{ V}$	Y1-Y240		1.0	1.5	k Ω	
					1.5	2.0		
					2.0	2.5		
Standby current	I_{SPD}		V_{SS}			75.0	μA	1
Supply current (1)	I_{DD}		V_{DD}			120.0	μA	2
Supply current (2)	I_0		V_{OL}, V_{OR}			240.0	μA	2

NOTES:

- $V_{DD} = +5.0\text{ V}$, $V_0 = +42.0\text{ V}$, $V_i = V_{SS}$
- $V_{DD} = +5.0\text{ V}$, $V_0 = +42.0\text{ V}$, $f_{LP} = 41.6\text{ kHz}$, $f_{FR} = 80\text{ Hz}$, 1/480 duty operation, no-load.

11.2 AC Characteristics

(Segment Mode 1) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +5.0 \pm 0.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10\text{ ns}$	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 2) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +3.0\text{ to }+4.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10\text{ ns}$	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

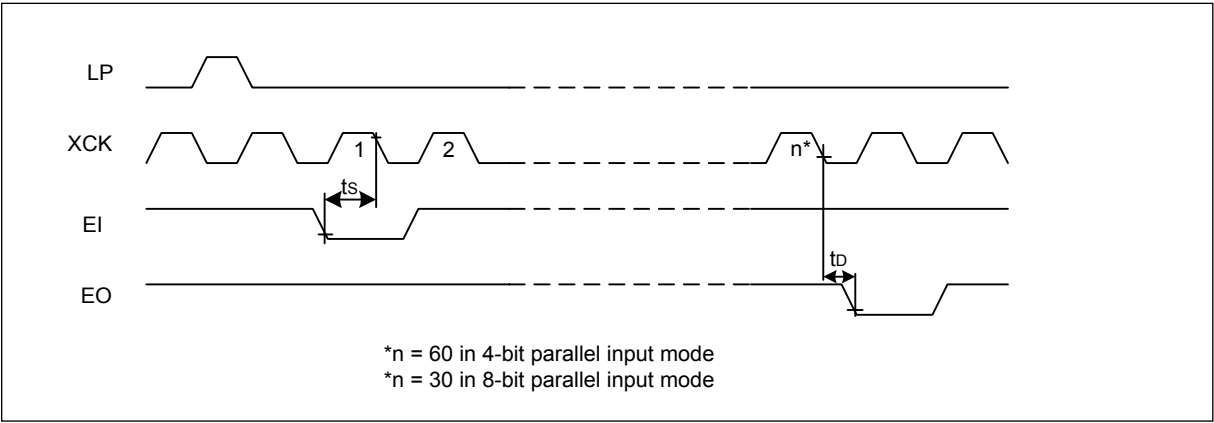
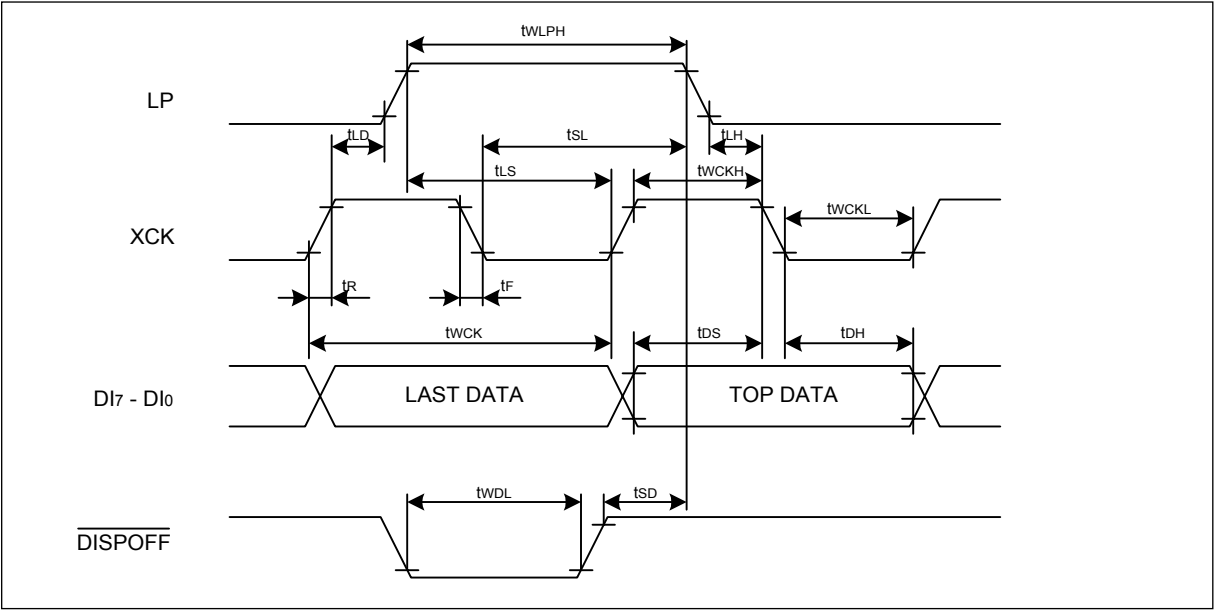
(Segment Mode 3) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+3.0\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10\text{ ns}$	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

11.3 Timing Chart of Segment Mode



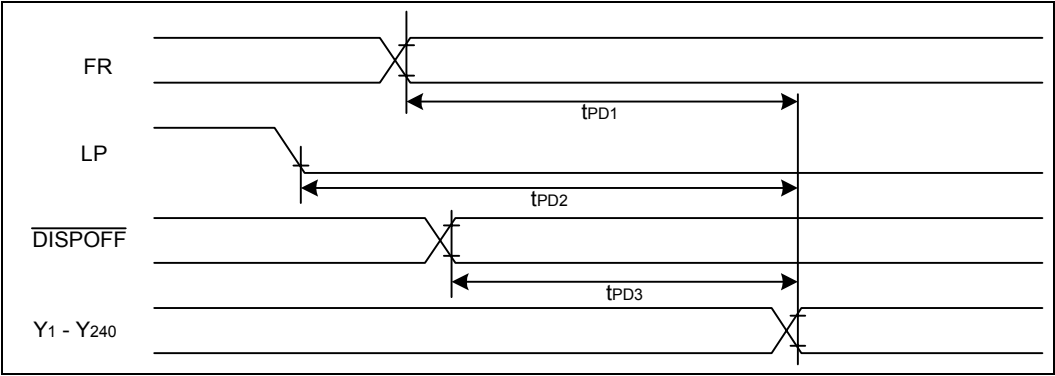
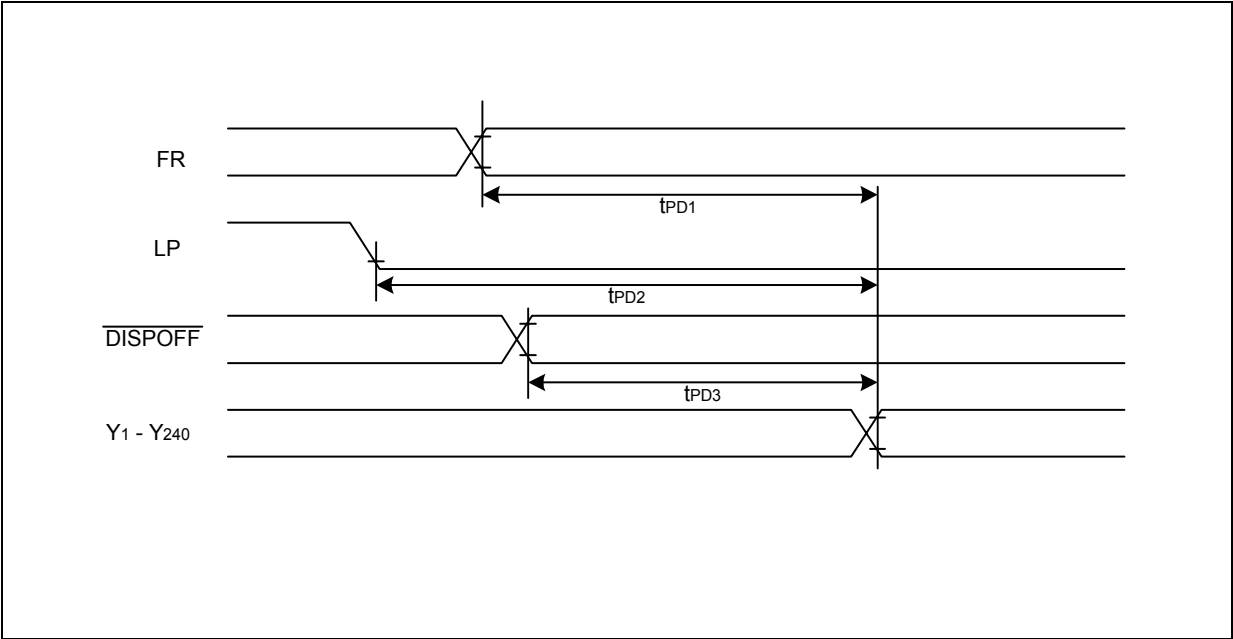
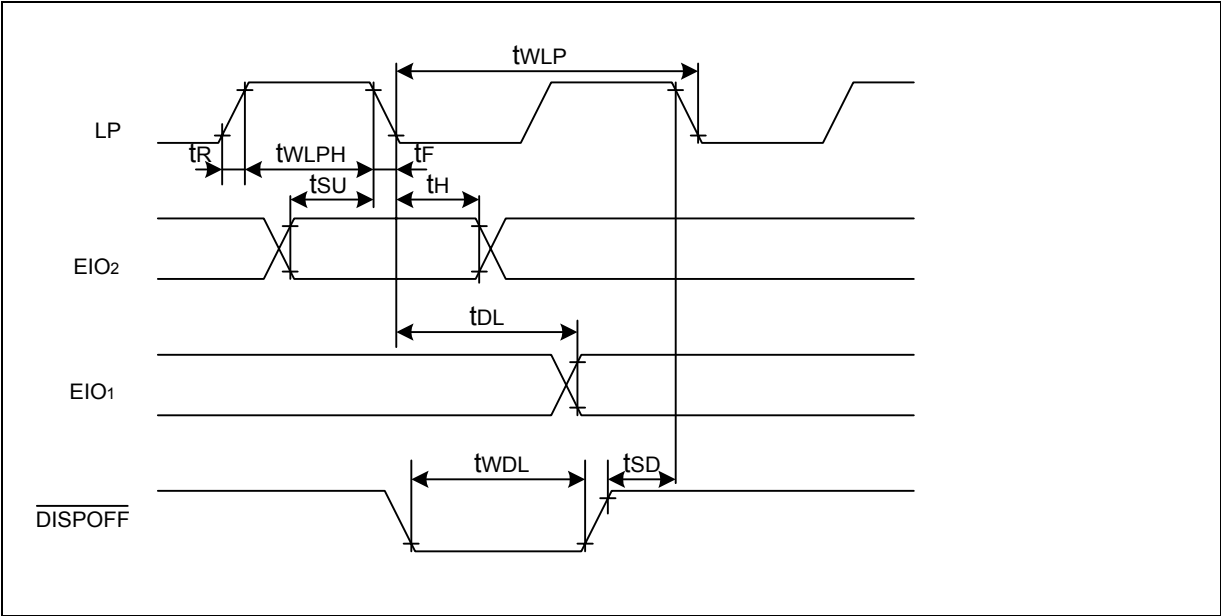


Fig. 8 Timing Characteristics (3)

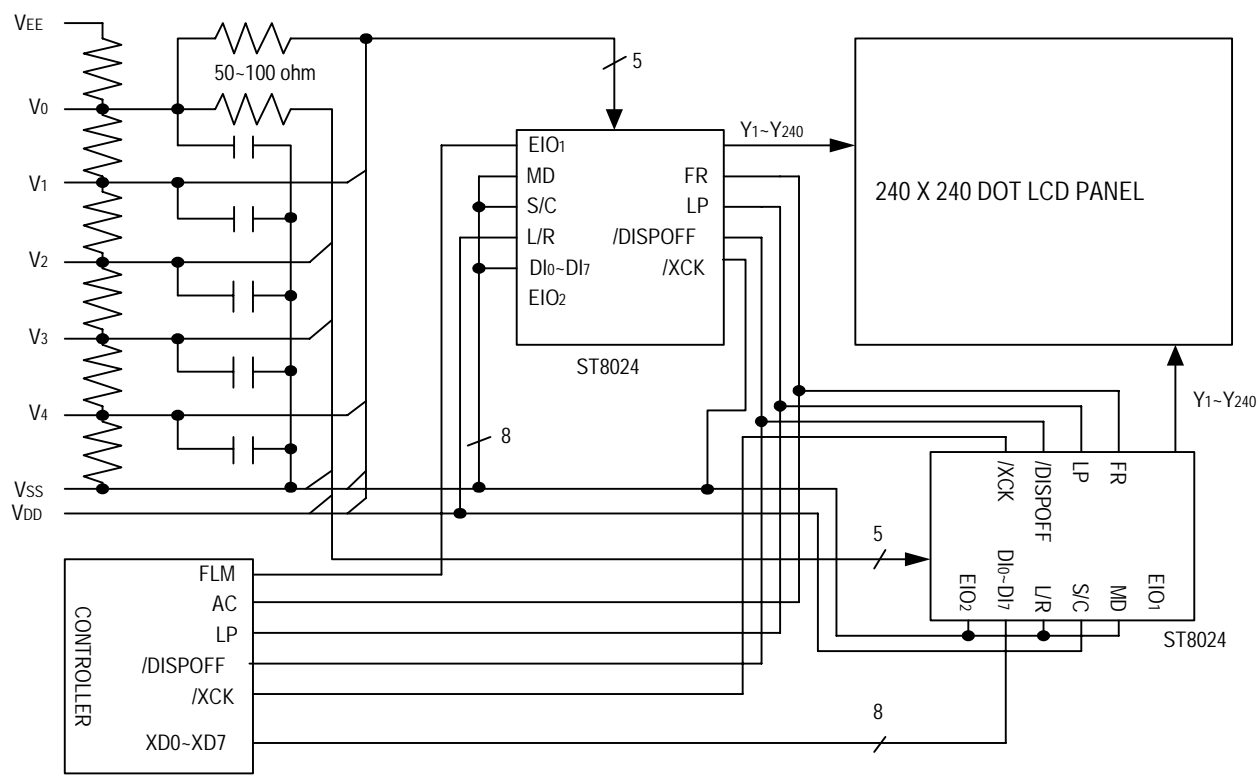
(Common Mode) ($V_{SS} = V_5 = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+5.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85^\circ\text{ C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	$t_R, t_F \leq 20\text{ ns}$	250			ns
Shift clock "H" pulse width	t_{WLPH}	$V_{DD} = +5.0 \pm 0.5\text{ V}$	15			ns
		$V_{DD} = +2.5 + 4.5\text{ V}$	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			μs
Output delay time (1)	t_{DL}	$CL = 15\text{ pF}$			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs

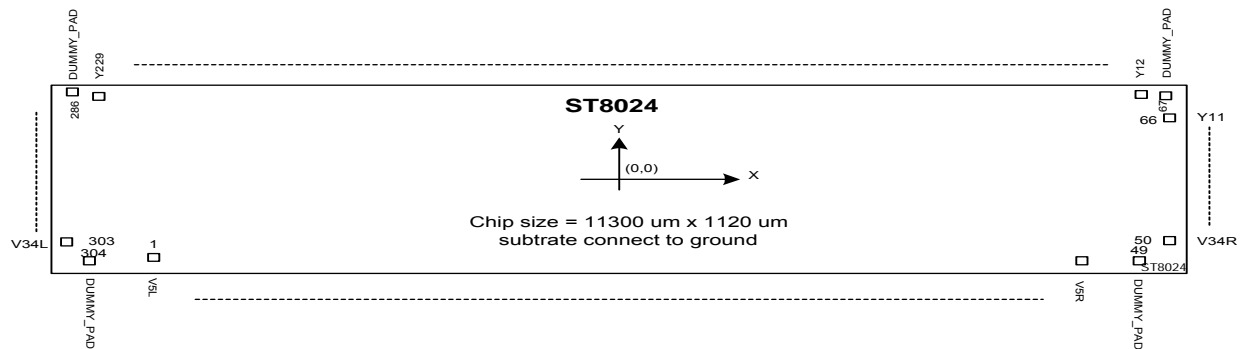
11.4 Timing Chart of Common Mode



12.APPLICATION CIRCUIT



13. PAD DIAGRAM



Unit : um

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	V5L	-5464.7	-471	38	FR_PAD	3346.9	-471	75	Y19	5075	467
2	V5L	-5384.7	-471	39	DUMMY_PAD	3616.3	-471	76	Y20	5025	467
3	GND	-5232.7	-471	40	LR_PAD	3885.7	-471	77	Y21	4975	467
4	GND	-5308.7	-471	41	DUMMY_PAD	4155.1	-471	78	Y22	4925	467
5	VCC	-5080.7	-471	42	MD_PAD	4424.5	-471	79	Y23	4875	467
6	VCC	-5156.7	-471	43	DUMMY_PAD	4693.9	-471	80	Y24	4825	467
7	DUMMY_PAD	-5004.5	-471	44	TEST1	4963.3	-471	81	Y25	4775	467
8	DBLKB_PAD	-4735.1	-471	45	GND	5232.7	-471	82	Y26	4725	467
9	DUMMY_PAD	-4465.7	-471	46	GND	5308.7	-471	83	Y27	4675	467
10	SC_PAD	-4196.3	-471	47	V5R	5384.7	-471	84	Y28	4625	467
11	DUMMY_PAD	-3926.9	-471	48	V5R	5464.7	-471	85	Y29	4575	467
12	EIO2	-3657.5	-471	49	DUMMY_PAD	5551.5	-471	86	Y30	4525	467
13	DUMMY_PAD	-3388.1	-471	50	V34R	5557	-394.8	87	Y31	4475	467
14	DI[0]	-3118.7	-471	51	V34R	5557	-344.8	88	Y32	4425	467
15	DUMMY_PAD	-2849.3	-471	52	V12R	5557	-294.8	89	Y33	4375	467
16	DI[1]	-2579.9	-471	53	V12R	5557	-244.8	90	Y34	4325	467
17	DUMMY_PAD	-2310.5	-471	54	V0R	5557	-194.8	91	Y35	4275	467
18	DI[2]	-2041.1	-471	55	V0R	5557	-144.8	92	Y36	4225	467
19	DUMMY_PAD	-1771.7	-471	56	Y1	5557	-94.8	93	Y37	4175	467
20	DI[3]	-1502.3	-471	57	Y2	5557	-44.8	94	Y38	4125	467
21	DUMMY_PAD	-1232.9	-471	58	Y3	5557	5.2	95	Y39	4075	467
22	DI[4]	-963.5	-471	59	Y4	5557	55.2	96	Y40	4025	467
23	DUMMY_PAD	-694.1	-471	60	Y5	5557	105.2	97	Y41	3975	467
24	DI[5]	-424.7	-471	61	Y6	5557	155.2	98	Y42	3925	467
25	DUMMY_PAD	-155.3	-471	62	Y7	5557	205.2	99	Y43	3875	467
26	DI[6]	114.1	-471	63	Y8	5557	255.2	100	Y44	3825	467
27	DUMMY_PAD	383.5	-471	64	Y9	5557	305.2	101	Y45	3775	467
28	DI[7]	652.9	-471	65	Y10	5557	355.2	102	Y46	3725	467
29	DUMMY_PAD	922.3	-471	66	Y11	5557	405.2	103	Y47	3675	467
30	XCK_PAD	1191.7	-471	67	DUMMY_PAD	5551.5	474	104	Y48	3625	467
31	DUMMY_PAD	1461.1	-471	68	Y12	5425	467	105	Y49	3575	467
32	DOFFB_PAD	1730.5	-471	69	Y13	5375	467	106	Y50	3525	467
33	DUMMY_PAD	1999.9	-471	70	Y14	5325	467	107	Y51	3475	467
34	LP_PAD	2269.3	-471	71	Y15	5275	467	108	Y52	3425	467
35	DUMMY_PAD	2538.7	-471	72	Y16	5225	467	109	Y53	3375	467
36	EIO1	2808.1	-471	73	Y17	5175	467	110	Y54	3325	467
37	DUMMY_PAD	3077.5	-471	74	Y18	5125	467	111	Y55	3275	467

112	Y56	3225	467	166	Y110	525	467	220	Y164	-2175	467
113	Y57	3175	467	167	Y111	475	467	221	Y165	-2225	467
114	Y58	3125	467	168	Y112	425	467	222	Y166	-2275	467
115	Y59	3075	467	169	Y113	375	467	223	Y167	-2325	467
116	Y60	3025	467	170	Y114	325	467	224	Y168	-2375	467
117	Y61	2975	467	171	Y115	275	467	225	Y169	-2425	467
118	Y62	2925	467	172	Y116	225	467	226	Y170	-2475	467
119	Y63	2875	467	173	Y117	175	467	227	Y171	-2525	467
120	Y64	2825	467	174	Y118	125	467	228	Y172	-2575	467
121	Y65	2775	467	175	Y119	75	467	229	Y173	-2625	467
122	Y66	2725	467	176	Y120	25	467	230	Y174	-2675	467
123	Y67	2675	467	177	Y121	-25	467	231	Y175	-2725	467
124	Y68	2625	467	178	Y122	-75	467	232	Y176	-2775	467
125	Y69	2575	467	179	Y123	-125	467	233	Y177	-2825	467
126	Y70	2525	467	180	Y124	-175	467	234	Y178	-2875	467
127	Y71	2475	467	181	Y125	-225	467	235	Y179	-2925	467
128	Y72	2425	467	182	Y126	-275	467	236	Y180	-2975	467
129	Y73	2375	467	183	Y127	-325	467	237	Y181	-3025	467
130	Y74	2325	467	184	Y128	-375	467	238	Y182	-3075	467
131	Y75	2275	467	185	Y129	-425	467	239	Y183	-3125	467
132	Y76	2225	467	186	Y130	-475	467	240	Y184	-3175	467
133	Y77	2175	467	187	Y131	-525	467	241	Y185	-3225	467
134	Y78	2125	467	188	Y132	-575	467	242	Y186	-3275	467
135	Y79	2075	467	189	Y133	-625	467	243	Y187	-3325	467
136	Y80	2025	467	190	Y134	-675	467	244	Y188	-3375	467
137	Y81	1975	467	191	Y135	-725	467	245	Y189	-3425	467
138	Y82	1925	467	192	Y136	-775	467	246	Y190	-3475	467
139	Y83	1875	467	193	Y137	-825	467	247	Y191	-3525	467
140	Y84	1825	467	194	Y138	-875	467	248	Y192	-3575	467
141	Y85	1775	467	195	Y139	-925	467	249	Y193	-3625	467
142	Y86	1725	467	196	Y140	-975	467	250	Y194	-3675	467
143	Y87	1675	467	197	Y141	-1025	467	251	Y195	-3725	467
144	Y88	1625	467	198	Y142	-1075	467	252	Y196	-3775	467
145	Y89	1575	467	199	Y143	-1125	467	253	Y197	-3825	467
146	Y90	1525	467	200	Y144	-1175	467	254	Y198	-3875	467
147	Y91	1475	467	201	Y145	-1225	467	255	Y199	-3925	467
148	Y92	1425	467	202	Y146	-1275	467	256	Y200	-3975	467
149	Y93	1375	467	203	Y147	-1325	467	257	Y201	-4025	467
150	Y94	1325	467	204	Y148	-1375	467	258	Y202	-4075	467
151	Y95	1275	467	205	Y149	-1425	467	259	Y203	-4125	467
152	Y96	1225	467	206	Y150	-1475	467	260	Y204	-4175	467
153	Y97	1175	467	207	Y151	-1525	467	261	Y205	-4225	467
154	Y98	1125	467	208	Y152	-1575	467	262	Y206	-4275	467
155	Y99	1075	467	209	Y153	-1625	467	263	Y207	-4325	467
156	Y100	1025	467	210	Y154	-1675	467	264	Y208	-4375	467
157	Y101	975	467	211	Y155	-1725	467	265	Y209	-4425	467
158	Y102	925	467	212	Y156	-1775	467	266	Y210	-4475	467
159	Y103	875	467	213	Y157	-1825	467	267	Y211	-4525	467
160	Y104	825	467	214	Y158	-1875	467	268	Y212	-4575	467
161	Y105	775	467	215	Y159	-1925	467	269	Y213	-4625	467
162	Y106	725	467	216	Y160	-1975	467	270	Y214	-4675	467
163	Y107	675	467	217	Y161	-2025	467	271	Y215	-4725	467
164	Y108	625	467	218	Y162	-2075	467	272	Y216	-4775	467
165	Y109	575	467	219	Y163	-2125	467	273	Y217	-4825	467

274	Y218	-4875	467	285	Y229	-5425	467	295	Y238	-5557	5.2
275	Y219	-4925	467	286	DUMMY_PAD	-5551.5	474	296	Y239	-5557	-44.8
276	Y220	-4975	467	287	Y230	-5557	405.2	297	Y240	-5557	-94.8
277	Y221	-5025	467	288	Y231	-5557	355.2	298	V0L	-5557	-144.8
278	Y222	-5075	467	289	Y232	-5557	305.2	299	V0L	-5557	-194.8
279	Y223	-5125	467	290	Y233	-5557	255.2	300	V12L	-5557	-244.8
280	Y224	-5175	467	291	Y234	-5557	205.2	301	V12L	-5557	-294.8
281	Y225	-5225	467	292	Y235	-5557	155.2	302	V34L	-5557	-344.8
282	Y226	-5275	467	293	Y236	-5557	105.2	303	V34L	-5557	-394.8
283	Y227	-5325	467	294	Y237	-5557	55.2	304	DUMMY_PAD	-5551.5	-471
284	Y228	-5375	467								

13.1 Gold bump size

Pad No.	X	Y	Area (um ²)
1~48(not DUMMY_PAD)	58	60	3480
50~66,287~303	74	35	2590
7~43(DUMMY_PAD only)	58	60	3480
68~285	35	74	2590
49,67,286,304	85	60	5100

Bump pad height = 18um, strength=30g V5L(pin1),V5R(pin48) has no gold bump

Appendix

Version 0.2.....add pad location and gold bump data ,2000/oct/23
Version 0.21.....add BLANK contrast control information, 2000/oct/25
Version 0.24.....add TCP (F4) information, 2000/Dec/4
Version 0.25.....remove TCP information to another PDF file ST8024TCP(F4).PDF
Version 0.26.....gold bump strength=30g, update IC diagram
Version 0.27.....Correct wrong word mistake
Version 0.28.....Correct parameter name (page 17) , 2001/Sep/28
Version 0.29.....Correct DI to FLM (page 12) , 2001/10/04
Version 0.30.....Change operating temperature from -20°C~85°C to -25°C~85°C
Version 0.31.....Change description of TEST1 pin in PIN DESCRIPTION(TCP) in page 2 , 2002/Jul/22
Version 1.0.....Add 1 and 48 Gold bump size