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SSD0858

Advance Information

LCD Segment / Common Driver with Controller CMOS

1 General Description

SSD0858 is a single-chip CMOS 4 gray scale LCD driver with controller for liquid crystal dot-matrix graphic display system. SSD0858 consists of 169 high voltage driving output pins for driving maximum 104 Segments, 64 Commons and 1 icon driving Commons. SSD0858 supports two display modes 96x65 or 104x65 by pin select.

SSD0858 displays data directly from its internal 104x65x2 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through I²C Interface.

SSD0858 embeds a DC-DC Converter, a LCD Voltage Regulator, an On-Chip Bias Divider, Integrated Bias Capacitors, Integrated Booster Capacitors and an On-Chip Oscillator, which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD0858 is suitable for any portable battery-driven applications requiring a long operation period and a compact size.

This document contains information on a new product under definition stage. Solomon Systech Limited reserves the right to change or discontinue this product without notice.

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SSD0858

Rev 1.1

P 1/41

Mar 2003

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2 FEATURES

104x64 with 4 gray scale levels Graphic Display with an Icon Line
Single Supply Operation, 1.8 V - 3.3V
Low Current Sleep Mode
Maximum +12.0V LCD Driving Output Voltage
Maximum 400KHz I²C Interface
On-Chip 104 x 65 x 2 Graphic Display Data RAM
On-Chip Voltage Generator / External Power Supply
On-Chip Oscillator
Software selectable 2X / 3X / 4X / 5X On-Chip DC-DC Converter, with Integrated Capacitors
Software Selectable On-Chip Bias Dividers, with Integrated Capacitors
Programmable Multiplex ratio (partial display) [16Mux - 65Mux]
Programmable 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 bias ratio
Selectable LCD Driving Voltage Temperature Coefficients (5 settings) [-0.14%/°C (POR)]
Programmable Frame Frequency
Selectable Gray level by FRC & PWM
64 Levels Internal Contrast Control
External Contrast Control
Re-mapping of Row and Column Drivers
Vertical Scrolling
Display Offset Control
One time programmable (OTP) capability for Vout adjustment

3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	Seg	Com	Package Form
SSD0858Z	104 /96	64 + 1	Gold Bump Die

4 BLOCK DIAGRAM

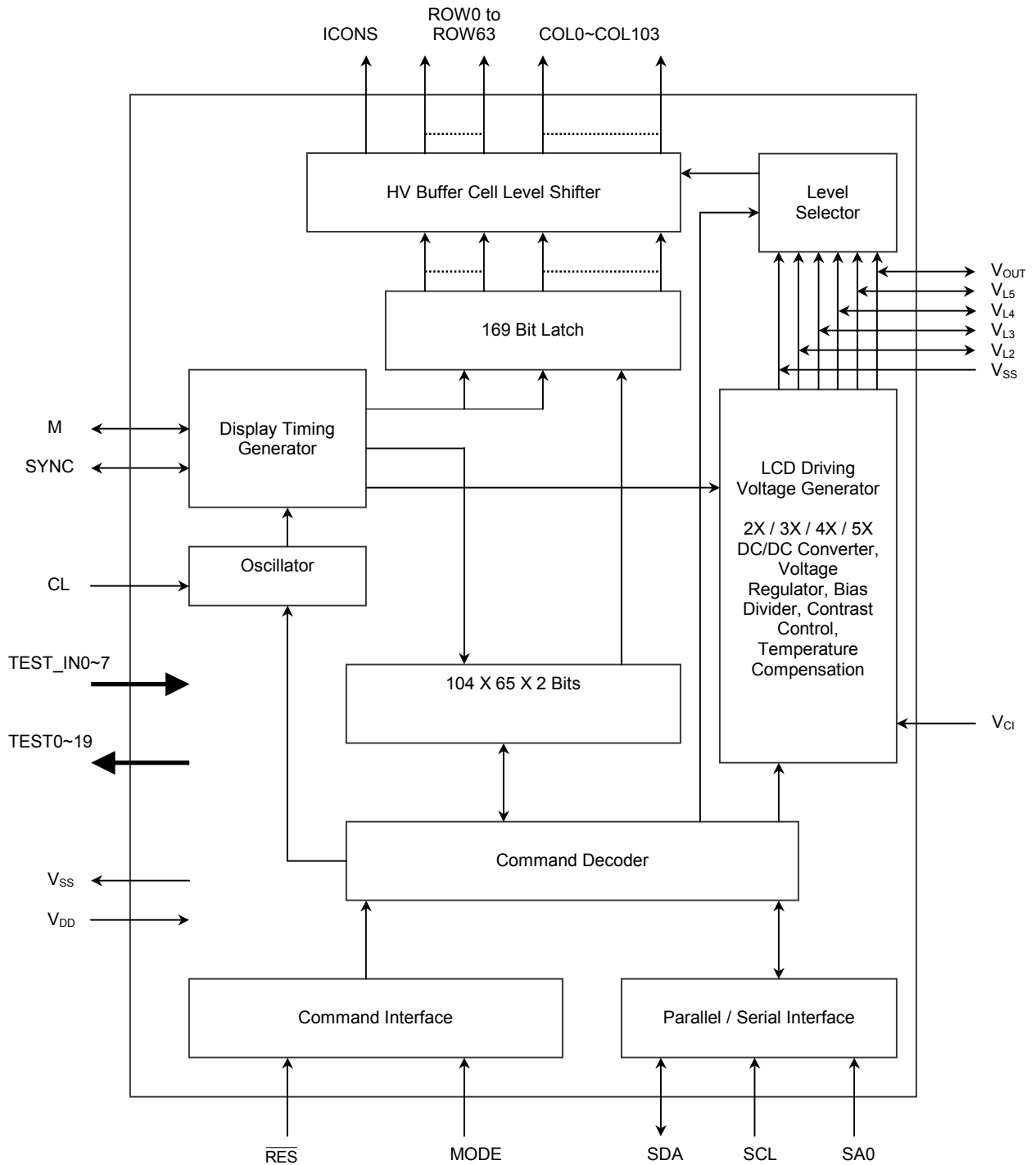
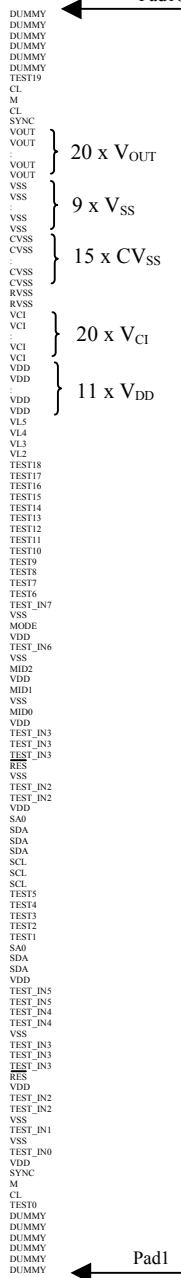


Figure 1 - Block Diagram

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1. Diagram showing the die face up.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in μm .
4. All alignment keys do not contain gold bump.

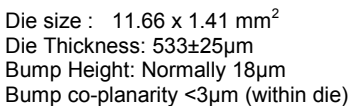


Figure 2 – SSD0858 Pin Assignment

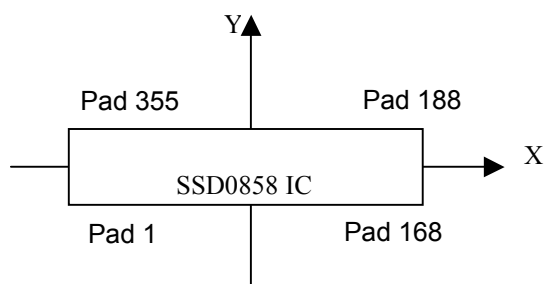
Table 2 - SSD0858 Series Die Pad Coordinates

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1	DUMMY	-5601.45	-619.05	51	TEST_IN3	-2256.45	-619.05	101	V _{CI}	1103.85	-619.05
2	DUMMY	-5534.55	-619.05	52	V _{DD}	-2189.55	-619.05	102	V _{CI}	1170.75	-619.05
3	DUMMY	-5467.65	-619.05	53	MID0	-2122.65	-619.05	103	V _{CI}	1237.65	-619.05
4	DUMMY	-5400.75	-619.05	54	V _{SS}	-2055.75	-619.05	104	V _{CI}	1304.55	-619.05
5	DUMMY	-5333.85	-619.05	55	MID1	-1988.85	-619.05	105	V _{CI}	1371.45	-619.05
6	DUMMY	-5266.95	-619.05	56	V _{DD}	-1921.95	-619.05	106	V _{CI}	1438.35	-619.05
7	TEST0	-5200.05	-619.05	57	MID2	-1855.05	-619.05	107	V _{CI}	1505.25	-619.05
8	CL	-5133.15	-619.05	58	V _{SS}	-1788.15	-619.05	108	V _{CI}	1572.15	-619.05
9	M	-5066.25	-619.05	59	TEST_IN6	-1721.25	-619.05	109	V _{CI}	1639.05	-619.05
10	SYNC	-4999.35	-619.05	60	V _{DD}	-1654.35	-619.05	110	V _{CI}	1705.95	-619.05
11	V _{DD}	-4932.45	-619.05	61	MODE	-1587.45	-619.05	111	V _{CI}	1772.85	-619.05
12	TEST_IN0	-4865.55	-619.05	62	V _{SS}	-1520.55	-619.05	112	RV _{SS}	1839.75	-619.05
13	V _{SS}	-4798.65	-619.05	63	TEST_IN7	-1453.65	-619.05	113	RV _{SS}	1906.65	-619.05
14	TEST_IN1	-4731.75	-619.05	64	TEST6	-1386.75	-619.05	114	CV _{SS}	1973.55	-619.05
15	VSS	-4664.85	-619.05	65	TEST7	-1319.85	-619.05	115	CV _{SS}	2040.45	-619.05
16	TEST_IN2	-4597.95	-619.05	66	TEST8	-1252.95	-619.05	116	CV _{SS}	2107.35	-619.05
17	TEST_IN2	-4531.05	-619.05	67	TEST9	-1186.05	-619.05	117	CV _{SS}	2174.25	-619.05
18	V _{DD}	-4464.15	-619.05	68	TEST10	-1119.15	-619.05	118	CV _{SS}	2241.15	-619.05
19	RES	-4397.25	-619.05	69	TEST11	-1052.25	-619.05	119	CV _{SS}	2308.05	-619.05
20	TEST_IN3	-4330.35	-619.05	70	TEST12	-985.35	-619.05	120	CV _{SS}	2374.95	-619.05
21	TEST_IN3	-4263.45	-619.05	71	TEST13	-918.45	-619.05	121	CV _{SS}	2441.85	-619.05
22	TEST_IN3	-4196.55	-619.05	72	TEST14	-851.55	-619.05	122	CV _{SS}	2508.75	-619.05
23	V _{SS}	-4129.65	-619.05	73	TEST15	-784.65	-619.05	123	CV _{SS}	2575.65	-619.05
24	TEST_IN4	-4062.75	-619.05	74	TEST16	-717.75	-619.05	124	CV _{SS}	2642.55	-619.05
25	TEST_IN4	-3995.85	-619.05	75	TEST17	-650.85	-619.05	125	CV _{SS}	2709.45	-619.05
26	TEST_IN5	-3928.95	-619.05	76	TEST18	-576.30	-619.05	126	CV _{SS}	2776.35	-619.05
27	TEST_IN5	-3862.05	-619.05	77	V _{L2}	-509.40	-619.05	127	CV _{SS}	2843.25	-619.05
28	VDD	-3795.15	-619.05	78	V _{L3}	-442.50	-619.05	128	CV _{SS}	2910.15	-619.05
29	SDA	-3728.25	-619.05	79	V _{L4}	-375.60	-619.05	129	V _{SS}	2977.05	-619.05
30	SDA	-3661.35	-619.05	80	V _{L5}	-308.70	-619.05	130	V _{SS}	3043.95	-619.05
31	SA0	-3594.45	-619.05	81	V _{DD}	-234.15	-619.05	131	V _{SS}	3110.85	-619.05
32	TEST1	-3527.55	-619.05	82	V _{DD}	-167.25	-619.05	132	V _{SS}	3177.75	-619.05
33	TEST2	-3460.65	-619.05	83	V _{DD}	-100.35	-619.05	133	V _{SS}	3244.65	-619.05
34	TEST3	-3393.75	-619.05	84	V _{DD}	-33.45	-619.05	134	V _{SS}	3311.55	-619.05
35	TEST4	-3326.85	-619.05	85	V _{DD}	33.45	-619.05	135	V _{SS}	3378.45	-619.05
36	TEST5	-3259.95	-619.05	86	V _{DD}	100.35	-619.05	136	V _{SS}	3445.35	-619.05
37	SCL	-3193.05	-619.05	87	V _{DD}	167.25	-619.05	137	V _{SS}	3512.25	-619.05
38	SCL	-3126.15	-619.05	88	V _{DD}	234.15	-619.05	138	V _{OUT}	3586.80	-619.05
39	SCL	-3059.25	-619.05	89	V _{DD}	301.05	-619.05	139	V _{OUT}	3653.70	-619.05
40	SDA	-2992.35	-619.05	90	V _{DD}	367.95	-619.05	140	V _{OUT}	3720.60	-619.05
41	SDA	-2925.45	-619.05	91	V _{DD}	434.85	-619.05	141	V _{OUT}	3787.50	-619.05
42	SDA	-2858.55	-619.05	92	V _{CI}	501.75	-619.05	142	V _{OUT}	3854.40	-619.05
43	SA0	-2791.65	-619.05	93	V _{CI}	568.65	-619.05	143	V _{OUT}	3921.30	-619.05
44	V _{DD}	-2724.75	-619.05	94	V _{CI}	635.55	-619.05	144	V _{OUT}	3988.20	-619.05
45	TEST_IN2	-2657.85	-619.05	95	V _{CI}	702.45	-619.05	145	V _{OUT}	4055.10	-619.05
46	TEST_IN2	-2590.95	-619.05	96	V _{CI}	769.35	-619.05	146	V _{OUT}	4122.00	-619.05
47	V _{SS}	-2524.05	-619.05	97	V _{CI}	836.25	-619.05	147	V _{OUT}	4188.90	-619.05
48	RES	-2457.15	-619.05	98	V _{CI}	903.15	-619.05	148	V _{OUT}	4255.80	-619.05
49	TEST_IN3	-2390.25	-619.05	99	V _{CI}	970.05	-619.05	149	V _{OUT}	4322.70	-619.05
50	TEST_IN3	-2323.35	-619.05	100	V _{CI}	1036.95	-619.05	150	V _{OUT}	4389.60	-619.05

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	SIGNAL MODE=H	SIGNAL MODE=L	X-pos	Y-pos
151	V _{OUT}	4456.50	-619.05	201	ROW6	ROW6	ROW6	4716.45	619.05
152	V _{OUT}	4523.40	-619.05	202	ROW5	ROW5	ROW5	4649.55	619.05
153	V _{OUT}	4590.30	-619.05	203	ROW4	ROW4	ROW4	4582.65	619.05
154	V _{OUT}	4657.20	-619.05	204	ROW3	ROW3	ROW3	4515.75	619.05
155	V _{OUT}	4724.10	-619.05	205	ROW2	ROW2	ROW2	4448.85	619.05
156	V _{OUT}	4791.00	-619.05	206	ROW1	ROW1	ROW1	4381.95	619.05
157	V _{OUT}	4857.90	-619.05	207	ROW0	ROW0	ROW0	4315.05	619.05
158	SYNC	4932.45	-619.05	208	ICONS	ICONS	ICONS	4248.15	619.05
159	CL	4999.35	-619.05	209	DUMMY	DUMMY	DUMMY	4181.25	619.05
160	M	5066.25	-619.05	210	DUMMY	DUMMY	DUMMY	4114.35	619.05
161	CL	5133.15	-619.05	211	DUMMY	DUMMY	DUMMY	4047.45	619.05
162	TEST19	5200.05	-619.05	212	DUMMY	DUMMY	DUMMY	3980.55	619.05
163	DUMMY	5266.95	-619.05	213	DUMMY	DUMMY	DUMMY	3913.65	619.05
164	DUMMY	5333.85	-619.05	214	DUMMY	DUMMY	DUMMY	3846.75	619.05
165	DUMMY	5400.75	-619.05	215	DUMMY	DUMMY	DUMMY	3779.85	619.05
166	DUMMY	5467.65	-619.05	216	DUMMY	DUMMY	DUMMY	3712.95	619.05
167	DUMMY	5534.55	-619.05	217	DUMMY	DUMMY	DUMMY	3646.05	619.05
168	DUMMY	5601.45	-619.05	218	DUMMY	DUMMY	DUMMY	3579.15	619.05
169	DUMMY	5741.55	-615.90	219	DUMMY	DUMMY	DUMMY	3512.25	619.05
170	DUMMY	5741.55	-549.00	220	COL0	N/C	SEG0	3445.35	619.05
171	ROW31	5741.55	-482.10	221	COL1	N/C	SEG1	3378.45	619.05
172	ROW30	5741.55	-415.20	222	COL2	N/C	SEG2	3311.55	619.05
173	ROW29	5741.55	-348.30	223	COL3	N/C	SEG3	3244.65	619.05
174	ROW28	5741.55	-281.40	224	COL4	SEG0	SEG4	3177.75	619.05
175	ROW27	5741.55	-214.50	225	COL5	SEG1	SEG5	3110.85	619.05
176	ROW26	5741.55	-147.60	226	COL6	SEG2	SEG6	3043.95	619.05
177	ROW25	5741.55	-80.70	227	COL7	SEG3	SEG7	2977.05	619.05
178	ROW24	5741.55	-13.80	228	COL8	SEG4	SEG8	2910.15	619.05
179	ROW23	5741.55	53.10	229	COL9	SEG5	SEG9	2843.25	619.05
180	ROW22	5741.55	120.00	230	COL10	SEG6	SEG10	2776.35	619.05
181	ROW21	5741.55	186.90	231	COL11	SEG7	SEG11	2709.45	619.05
182	ROW20	5741.55	253.80	232	COL12	SEG8	SEG12	2642.55	619.05
183	ROW19	5741.55	320.70	233	COL13	SEG9	SEG13	2575.65	619.05
184	ROW18	5741.55	387.60	234	COL14	SEG10	SEG14	2508.75	619.05
185	ROW17	5741.55	454.50	235	COL15	SEG11	SEG15	2441.85	619.05
186	DUMMY	5741.55	521.40	236	COL16	SEG12	SEG16	2374.95	619.05
187	DUMMY	5741.55	588.30	237	COL17	SEG13	SEG17	2308.05	619.05
188	DUMMY	5586.15	619.05	238	COL18	SEG14	SEG18	2241.15	619.05
189	DUMMY	5519.25	619.05	239	COL19	SEG15	SEG19	2174.25	619.05
190	DUMMY	5452.35	619.05	240	COL20	SEG16	SEG20	2107.35	619.05
191	ROW16	5385.45	619.05	241	COL21	SEG17	SEG21	2040.45	619.05
192	ROW15	5318.55	619.05	242	COL22	SEG18	SEG22	1973.55	619.05
193	ROW14	5251.65	619.05	243	COL23	SEG19	SEG23	1906.65	619.05
194	ROW13	5184.75	619.05	244	COL24	SEG20	SEG24	1839.75	619.05
195	ROW12	5117.85	619.05	245	COL25	SEG21	SEG25	1772.85	619.05
196	ROW11	5050.95	619.05	246	COL26	SEG22	SEG26	1705.95	619.05
197	ROW10	4984.05	619.05	247	COL27	SEG23	SEG27	1639.05	619.05
198	ROW9	4917.15	619.05	248	COL28	SEG24	SEG28	1572.15	619.05
199	ROW8	4850.25	619.05	249	COL29	SEG25	SEG29	1505.25	619.05
200	ROW7	4783.35	619.05	250	COL30	SEG26	SEG30	1438.35	619.05

Pad #	Pad Name	SIGNAL MODE=H	SIGNAL MODE=L	X-pos	Y-pos	Pad #	Pad Name	SIGNAL MODE=H	SIGNAL MODE=L	X-pos	Y-pos
251	COL31	SEG27	SEG31	1371.45	619.05	301	COL81	SEG77	SEG81	-1973.55	619.05
252	COL32	SEG28	SEG32	1304.55	619.05	302	COL82	SEG78	SEG82	-2040.45	619.05
253	COL33	SEG29	SEG33	1237.65	619.05	303	COL83	SEG79	SEG83	-2107.35	619.05
254	COL34	SEG30	SEG34	1170.75	619.05	304	COL84	SEG80	SEG84	-2174.25	619.05
255	COL35	SEG31	SEG35	1103.85	619.05	305	COL85	SEG81	SEG85	-2241.15	619.05
256	COL36	SEG32	SEG36	1036.95	619.05	306	COL86	SEG82	SEG86	-2308.05	619.05
257	COL37	SEG33	SEG37	970.05	619.05	307	COL87	SEG83	SEG87	-2374.95	619.05
258	COL38	SEG34	SEG38	903.15	619.05	308	COL88	SEG84	SEG88	-2441.85	619.05
259	COL39	SEG35	SEG39	836.25	619.05	309	COL89	SEG85	SEG89	-2508.75	619.05
260	COL40	SEG36	SEG40	769.35	619.05	310	COL90	SEG86	SEG90	-2575.65	619.05
261	COL41	SEG37	SEG41	702.45	619.05	311	COL91	SEG87	SEG91	-2642.55	619.05
262	COL42	SEG38	SEG42	635.55	619.05	312	COL92	SEG88	SEG92	-2709.45	619.05
263	COL43	SEG39	SEG43	568.65	619.05	313	COL93	SEG89	SEG93	-2776.35	619.05
264	COL44	SEG40	SEG44	501.75	619.05	314	COL94	SEG90	SEG94	-2843.25	619.05
265	COL45	SEG41	SEG45	434.85	619.05	315	COL95	SEG91	SEG95	-2910.15	619.05
266	COL46	SEG42	SEG46	367.95	619.05	316	COL96	SEG92	SEG96	-2977.05	619.05
267	COL47	SEG43	SEG47	301.05	619.05	317	COL97	SEG93	SEG97	-3043.95	619.05
268	COL48	SEG44	SEG48	234.15	619.05	318	COL98	SEG94	SEG98	-3110.85	619.05
269	COL49	SEG45	SEG49	167.25	619.05	319	COL99	SEG95	SEG99	-3177.75	619.05
270	COL50	SEG46	SEG50	100.35	619.05	320	COL100	N/C	SEG100	-3244.65	619.05
271	COL51	SEG47	SEG51	33.45	619.05	321	COL101	N/C	SEG101	-3311.55	619.05
272	COL52	SEG48	SEG52	-33.45	619.05	322	COL102	N/C	SEG102	-3378.45	619.05
273	COL53	SEG49	SEG53	-100.35	619.05	323	COL103	N/C	SEG103	-3445.35	619.05
274	COL54	SEG50	SEG54	-167.25	619.05	324	DUMMY	DUMMY	DUMMY	-3512.25	619.05
275	COL55	SEG51	SEG55	-234.15	619.05	325	DUMMY	DUMMY	DUMMY	-3579.15	619.05
276	COL56	SEG52	SEG56	-301.05	619.05	326	DUMMY	DUMMY	DUMMY	-3646.05	619.05
277	COL57	SEG53	SEG57	-367.95	619.05	327	DUMMY	DUMMY	DUMMY	-3712.95	619.05
278	COL58	SEG54	SEG58	-434.85	619.05	328	DUMMY	DUMMY	DUMMY	-3779.85	619.05
279	COL59	SEG55	SEG59	-501.75	619.05	329	DUMMY	DUMMY	DUMMY	-3846.75	619.05
280	COL60	SEG56	SEG60	-568.65	619.05	330	DUMMY	DUMMY	DUMMY	-3913.65	619.05
281	COL61	SEG57	SEG61	-635.55	619.05	331	DUMMY	DUMMY	DUMMY	-3980.55	619.05
282	COL62	SEG58	SEG62	-702.45	619.05	332	DUMMY	DUMMY	DUMMY	-4047.45	619.05
283	COL63	SEG59	SEG63	-769.35	619.05	333	DUMMY	DUMMY	DUMMY	-4114.35	619.05
284	COL64	SEG60	SEG64	-836.25	619.05	334	DUMMY	DUMMY	DUMMY	-4181.25	619.05
285	COL65	SEG61	SEG65	-903.15	619.05	335	ROW32	ROW32	ROW32	-4248.15	619.05
286	COL66	SEG62	SEG66	-970.05	619.05	336	ROW33	ROW33	ROW33	-4315.05	619.05
287	COL67	SEG63	SEG67	-1036.95	619.05	337	ROW34	ROW34	ROW34	-4381.95	619.05
288	COL68	SEG64	SEG68	-1103.85	619.05	338	ROW35	ROW35	ROW35	-4448.85	619.05
289	COL69	SEG65	SEG69	-1170.75	619.05	339	ROW36	ROW36	ROW36	-4515.75	619.05
290	COL70	SEG66	SEG70	-1237.65	619.05	340	ROW37	ROW37	ROW37	-4582.65	619.05
291	COL71	SEG67	SEG71	-1304.55	619.05	341	ROW38	ROW38	ROW38	-4649.55	619.05
292	COL72	SEG68	SEG72	-1371.45	619.05	342	ROW39	ROW39	ROW39	-4716.45	619.05
293	COL73	SEG69	SEG73	-1438.35	619.05	343	ROW40	ROW40	ROW40	-4783.35	619.05
294	COL74	SEG70	SEG74	-1505.25	619.05	344	ROW41	ROW41	ROW41	-4850.25	619.05
295	COL75	SEG71	SEG75	-1572.15	619.05	345	ROW42	ROW42	ROW42	-4917.15	619.05
296	COL76	SEG72	SEG76	-1639.05	619.05	346	ROW43	ROW43	ROW43	-4984.05	619.05
297	COL77	SEG73	SEG77	-1705.95	619.05	347	ROW44	ROW44	ROW44	-5050.95	619.05
298	COL78	SEG74	SEG78	-1772.85	619.05	348	ROW45	ROW45	ROW45	-5117.85	619.05
299	COL79	SEG75	SEG79	-1839.75	619.05	349	ROW46	ROW46	ROW46	-5184.75	619.05
300	COL80	SEG76	SEG80	-1906.65	619.05	350	ROW47	ROW47	ROW47	-5251.65	619.05

Pad #	Signal	X-pos	Y-pos
351	ROW48	-5318.55	619.05
352	ROW49	-5385.45	619.05
353	DUMMY	-5452.35	619.05
354	DUMMY	-5519.25	619.05
355	DUMMY	-5586.15	619.05
356	DUMMY	-5741.55	588.30
357	DUMMY	-5741.55	521.40
358	ROW50	-5741.55	454.50
359	ROW51	-5741.55	387.60
360	ROW52	-5741.55	320.70
361	ROW53	-5741.55	253.80
362	ROW54	-5741.55	186.90
363	ROW55	-5741.55	120.00
364	ROW56	-5741.55	53.10
365	ROW57	-5741.55	-13.80
366	ROW58	-5741.55	-80.70
367	ROW59	-5741.55	-147.60
368	ROW60	-5741.55	-214.50
369	ROW61	-5741.55	-281.40
370	ROW62	-5741.55	-348.30
371	ROW63	-5741.55	-415.20
372	ICONS	-5741.55	-482.10
373	DUMMY	-5741.55	-549.00
374	DUMMY	-5741.55	-615.90



	X	Y	Unit	Remark
Pad Pitch	66.9	66.9	um	Min.
Pad Space	24.9	24.9	um	Min.

	Pad #	X	Y	Unit
Pad Size	1 - 168	42	60	um
	169 - 187	60	42	um
	188 - 355	42	60	um
	356 - 374	60	42	um

6 PIN DESCRIPTION

6.1 $\overline{\text{RES}}$

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

6.2 SDA, SCL & SA0

These pins are bi-directional data bus to be connected to the MCU in I²C-bus interface. Please refer to the section: I²C Communication interface on page 22 for detail pin descriptions.

6.3 V_{DD}

Power supply pin.

6.4 RV_{SS}

Ground reference of Vref.

6.5 CV_{SS}

Ground reference of analog circuitry.

6.6 V_{SS}

Ground reference of logic circuitry.

6.7 V_{CI}

Reference voltage input for internal DC-DC converter. The voltage of generated V_{CC} equals to the multiple factor (2X, 3X, 4X or 5X) times V_{CI} with respect to V_{SS} .

Note: Voltage at this input pin must be larger than or equal to V_{DD} .

6.8 V_{OUT}

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal regulator.

6.9 V_{L5} , V_{L4} , V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$$V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$$

Table 3 - $V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$ Relationship

	1 : a bias
V_{L5}	$(a-1)/a * V_{OUT}$
V_{L4}	$(a-2)/a * V_{OUT}$
V_{L3}	$2/a * V_{OUT}$
V_{L2}	$1/a * V_{OUT}$

a is equals to 9 at POR.

6.10 ROW0 – ROW63

These pins provide the row driving signal ROW0 - ROW63 to the LCD panel. See Figure 5 or Figure 7 about the COM signal mapping in different multiplex ratio N.

6.11 ICONS

This pin is the special icon line ROW signal output.

6.12 COL0 – COL103

These pins provide the LCD column driving signal. Their voltage level is V_{SS} during sleep mode.

6.13 CL

This pin is the external clock input for the device, which is enabled by using an extended command. Under normal operation, this pin should be left opened and internal oscillator will be used after power on reset.

6.14 M

This pin is used for cascade purpose only. Under normal operation, it should be left open.

6.15 MID0~MID2

These pins are used for setting the ID code of LCD panel manufacturer. These pins should be connected to V_{SS} or V_{DD} when NOT IN USE.

6.16 SYNC

This pin is used for cascade purpose only. Under normal operation, it should be left open.

6.17 MODE

This pin is used for setting the display size.

Table 4 – Mode setting

MODE	Remarks:
H	SSD0858 96x65 display mode
L	SSD0858 104x65 display mode

6.18 TEST_IN0~7

These pins are used for internal only. TEST_IN0~5 & 7 should be connected to V_{SS} and TEST_IN6 should be connected to V_{DD} .

6.19 TEST0~19

These pins are used for internal only and should be left open, any connection is not allowed.

6.20 Dummy

There are the floating dummy pads without any internal circuitry connection.

6.21 N/C

These No Connection pins should NOT be connected to signal pins nor shorted together. They should be left open.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 I²C communication Interface

The IIC communication interface consists of slave address bit (SA0), I²C-bus data signal (SDA) and I²C-bus clock signal (SCL). Both the SDA and the SCL must be connected to pull-up resistors. There is also an input signal \overline{RES} which is used for the initialization of device.

a) Slave address bit (SA0)

SSD0858 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will responds to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W" bit) with the following byte format,

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀
0 1 1 1 1 0 SA0 R/W

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101" can be selected as the slave address of SSD0858.

"R/W" bit determines the I²C-bus interface is operating at either write mode or read status mode.

b) I²C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

c) I²C-bus clock signal (SCL)

The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.2 Command Decoder

Input is directed to the command decoder based on the input of control byte which consists of a D/C bit and a R/W bit. For further information about the control byte, please refer to the section "I²C-bus write data and read register status" on page 22. If both the D/C bit and the R/W bit are low, the input signal is interpreted as a Command. It will be decoded and written to the corresponding command register. If the D/C bit is high and the R/W bit is low, input signal is written to Graphic Display Data RAM (GDDRAM).

7.3 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 104 x 65 x 2 = 12,480bits. Figure 4 is a description of the GDDRAM address map.

For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data mapped to the display. Figure 4 shows the case in which the display start line register is set at 30H.

For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

7.4 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 3). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

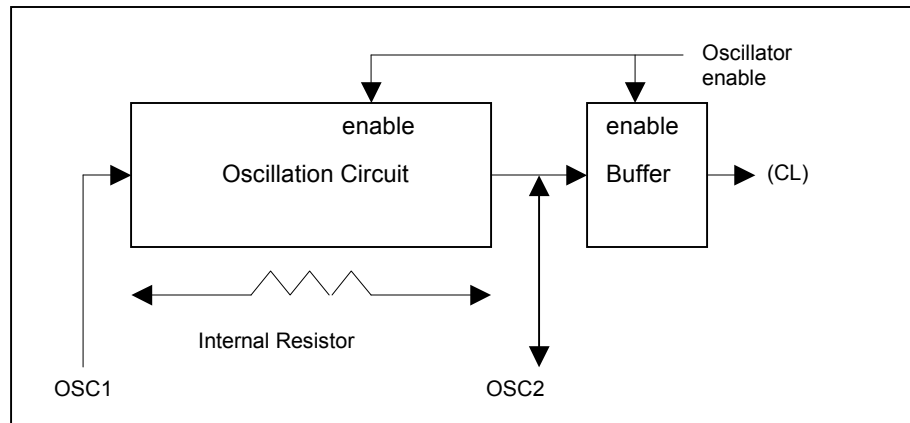


Figure 3 - Oscillator Circuitry

7.5 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages.

It consists of:

1. 2X, 3X, 4X and 5X DC-DC voltage converter
2. Bias Divider
If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{OUT}) to give the LCD driving levels ($V_{L2} - V_{L5}$). The divider does not require external capacitors that reduce the external hardware and pin counts.
3. Contrast Control
Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry
Software control of 1/4 to 1/9 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry
Provide 5 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is $-0.14\%/^{\circ}\text{C}$.

7.6 169 Bits Latch

A register carries the display signal information. In 104 X 65 display-mode, data will be fed to the HV-buffer Cell and level-shifted to the required level.

7.7 Level selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

7.8 HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter, which translated the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

7.9 Default Setting after Reset

When $\overline{\text{RES}}$ input is low, the chip is initialized to the following:

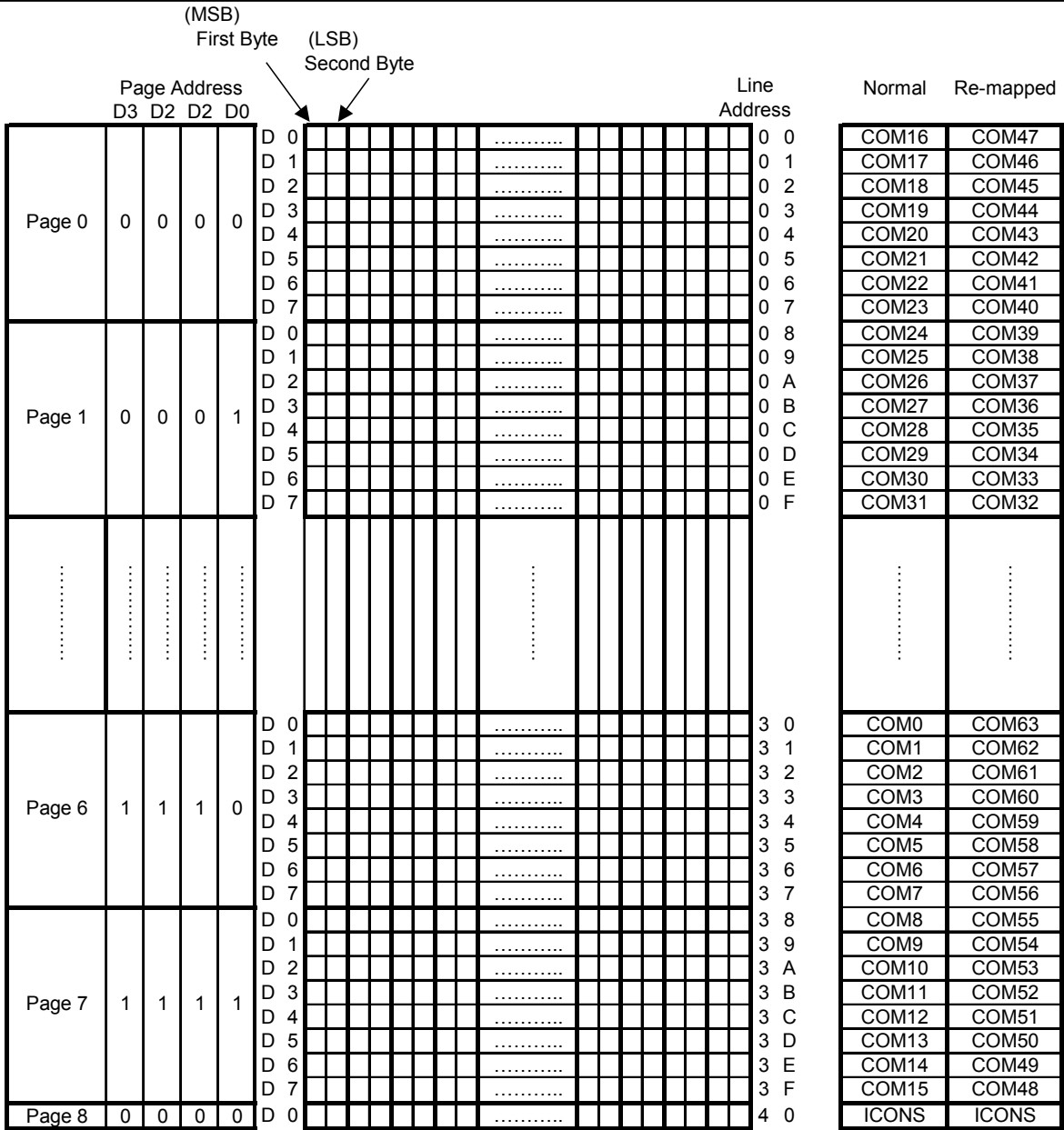
Register	Default Value	Descriptions
Page address	0	
Column address	0	
Display ON/OFF	0	Display OFF
Display Start Line	0	GDDRAM page 0,D0
Display Offset	0	COM0 is mapped to ROW0
Mux Ratio	40H	64 Mux
Normal/Reverse Display	0	Normal Display
N-line Inversion	0	No N-line Inversion
Entire Display	0	Entire Display is OFF
DC-DC booster	0	3X booster is selected
Internal Resistor Ratio	0	Gain = 2.84 (IR0)
Contrast	20H	
LCD Bias Ratio	5	1/9 Bias Ratio
Scan direction of COM	0	Normal Scan direction
Segment Re-map	0	Segment re-map is disabled
Internal oscillator	0	Internal oscillator is OFF
Power save mode	0	Power save mode is OFF
Data display length	0	
FRC, PWM Mode	0	4FRC, 9PWM
White Palette	(0, 0, 0, 0)	
Light Gray Palette	(9, 0, 0, 0)	
Dark Gray Palette	(9, 9, 9, 0)	
Black Palette	(9, 9, 9, 9)	
Test mode	0	Test mode is OFF
Temperature coefficient	4	PTC4 (-0.14%/°C)
Icon display	0	Icon display line is OFF
Frame frequency	8	Frame frequency = 157.5Hz
Power control	0,0,0	Booster, regulator & divider are both disabled

When RESET command is issued, the following parameters are initialized only:

Register	Default Value	Descriptions
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 2.84 (IR0)
Contrast	20H	
Data display length	0	
FRC, PWM Mode	0	4FRC, 9PWM
White Palette	(0, 0, 0, 0)	
Light Gray Palette	(9, 0, 0, 0)	
Dark Gray Palette	(9, 9, 9, 0)	
Black Palette	(9, 9, 9, 9)	

7.10 LCD Panel Driving Waveform

Figure 4 and Figure 5 are examples of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 6 and Figure 7 illustrate the desired multiplex scheme with N-line inversion feature is disabled (default).



Internal Column Address	00	01	02	03	04	05	06	07	B8	B9	BA	BB	BC	BD	BE	BF
SEG Re-map = 0	00	01	02	03	5C	5D	5E	5F								
SEG Re-map = 1	5F	5E	5D	5C	03	02	01	00								
SEG Outputs	SEG0	SEG1	SEG2	SEG3	SEG92	SEG93	SEG94	SEG95								

MODE=HIGH(V_{DD})

Figure 4 - SSD0858 Graphic Display Data RAM (GDDRAM) Address Map (with vertical scroll value 30H & MODE=H)

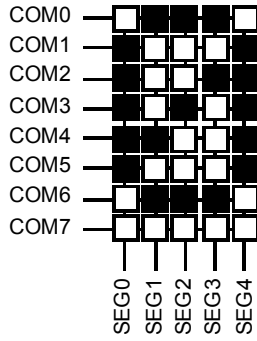
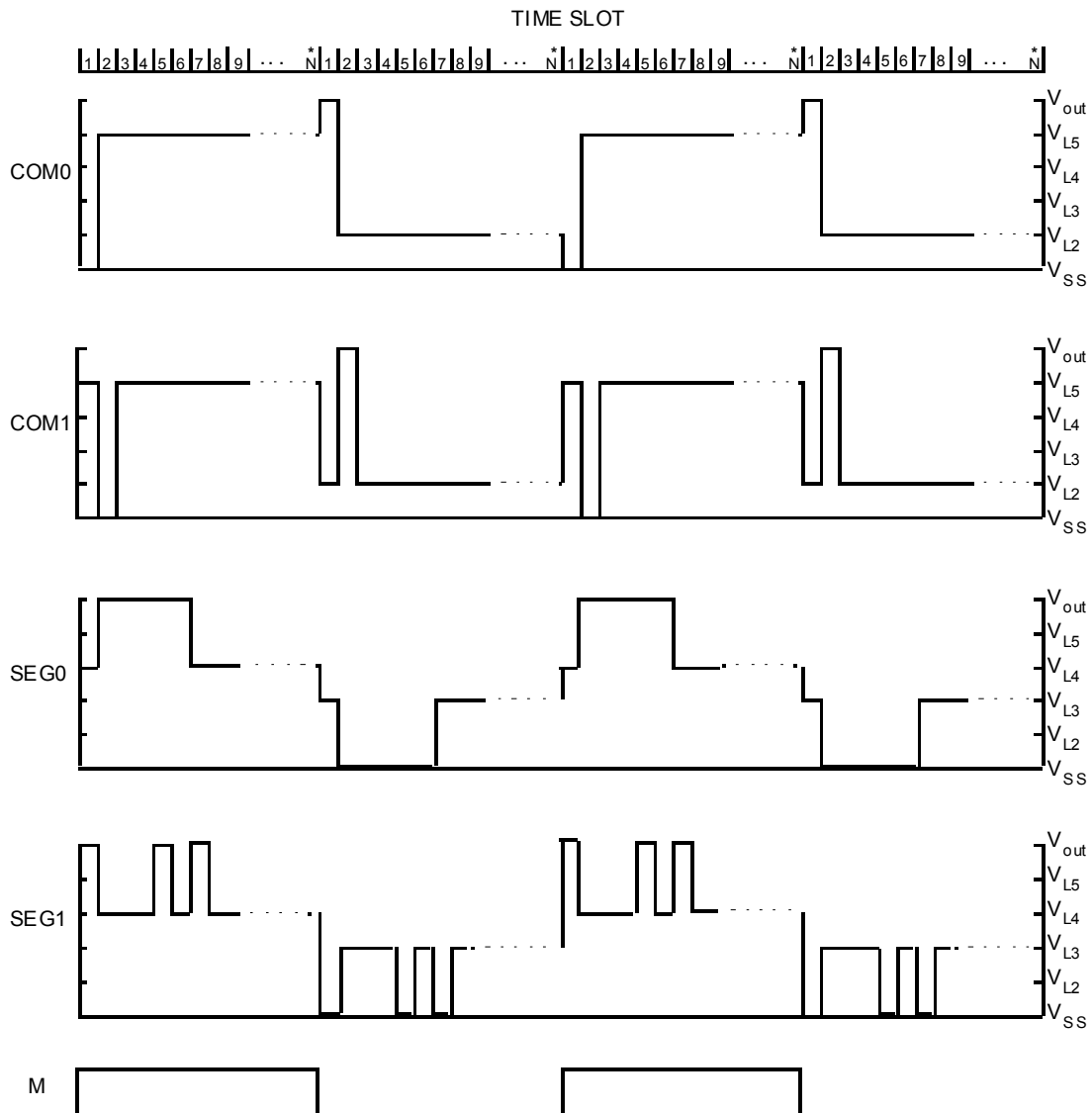


Figure 6 - LCD Display Example "0"



* Note : N is the number of multiplex ratio including loon line if it is enabled, N is equal to 64 on POR.

Figure 7 - LCD Driving Signal from SSD0858

8 COMMAND TABLE

Table 5 - COMMAND TABLE

Bit Pattern	Command	Description
0000 C ₃ C ₂ C ₁ C ₀	Set Lower Column Address	Set the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0001 0C ₆ C ₅ C ₄	Set Upper Column Address	Set the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0010 0R ₂ R ₁ R ₀	Set Internal Regulator Resistor Ratio	The internal regulator gain (1+R ₂ /R ₁) Vout increases as R ₂ R ₁ R ₀ is increased from 000b to 111b. The factor, 1+R ₂ /R ₁ , is given by: R ₂ R ₁ R ₀ = 000: 2.84 (POR) R ₂ R ₁ R ₀ = 001: 3.71 R ₂ R ₁ R ₀ = 010: 4.57 R ₂ R ₁ R ₀ = 011: 5.44 R ₂ R ₁ R ₀ = 100: 6.30 R ₂ R ₁ R ₀ = 101: 7.16 R ₂ R ₁ R ₀ = 110: 8.03 R ₂ R ₁ R ₀ = 111: 8.89
0010 1VC VR VF	Set Power Control Register	VC=0: turn OFF the internal voltage booster (POR) VC=1: turn ON the internal voltage booster & regulator VR=0: turn OFF the internal regulator (POR) VR=1: turn ON the internal regulator & voltage booster VF=0: turn OFF the output op-amp buffer (POR) VF=1: turn ON the output op-amp buffer
0011 1T ₂ T ₁ T ₀	Set TC value	This command set the Temperature Coefficient T ₂ T ₁ T ₀ : 000: -0.01%/°C 001: -0.035%/°C 010: -0.05%/°C 011: -0.083%/°C 100: -0.14%/°C(POR) 101: Reserved 110: Reserved 111: Reserved
0100 00XX XL ₆ L ₅ L ₄ L ₃ L ₂ L ₁ L ₀	Set Display Start Line	The second command specifies the row address pointer (0-63) of the RAM data to be displayed in COM0. This command has no effect on ICONS. The pointer is set to 0 after reset.
0100 01XX XXC ₅ C ₄ C ₃ C ₂ C ₁ C ₀	Set Display Offset	The second command specifies the mapping of first display line (COM0) to one of ROW0~63. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

Bit Pattern	Command	Description																																				
0100 10XX XD ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Set Multiplex Ratio (Duty Ratio)	<p>The second command specifies the number of lines, excluding ICONS, to be displayed. With Icon is disabled (POR), 16~64 mux could be selected. With Icon enabled, the available multiplex ratios are 17~ 65mux.</p> <table><thead><tr><th><u>D₆ – D₀</u></th><th><u>Mux(icon disable)</u></th><th><u>Mux(icon enable)</u></th></tr></thead><tbody><tr><td>000000</td><td>invalid</td><td>invalid</td></tr><tr><td>...</td><td></td><td></td></tr><tr><td>0001111</td><td>invalid</td><td>invalid</td></tr><tr><td>0010000</td><td>16</td><td>17</td></tr><tr><td>0010001</td><td>17</td><td>18</td></tr><tr><td>...</td><td></td><td></td></tr><tr><td>1000000</td><td>64</td><td>65</td></tr><tr><td>1000001</td><td>invalid</td><td>invalid</td></tr><tr><td>1000010</td><td>invalid</td><td>invalid</td></tr><tr><td>...</td><td></td><td></td></tr><tr><td>1111111</td><td>invalid</td><td>invalid</td></tr></tbody></table>	<u>D₆ – D₀</u>	<u>Mux(icon disable)</u>	<u>Mux(icon enable)</u>	000000	invalid	invalid	...			0001111	invalid	invalid	0010000	16	17	0010001	17	18	...			1000000	64	65	1000001	invalid	invalid	1000010	invalid	invalid	...			1111111	invalid	invalid
<u>D₆ – D₀</u>	<u>Mux(icon disable)</u>	<u>Mux(icon enable)</u>																																				
000000	invalid	invalid																																				
...																																						
0001111	invalid	invalid																																				
0010000	16	17																																				
0010001	17	18																																				
...																																						
1000000	64	65																																				
1000001	invalid	invalid																																				
1000010	invalid	invalid																																				
...																																						
1111111	invalid	invalid																																				
0100 11XX XXXN ₄ N ₃ N ₂ N ₁ N ₀	Set N-line Inversion	<p>The second command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value.</p> <p>To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n).</p> <table><thead><tr><th><u>N₄ – N₀</u></th><th><u>n-line inversion</u></th></tr></thead><tbody><tr><td>00000</td><td>Exit n-line inversion</td></tr><tr><td>00001</td><td>3 lines</td></tr><tr><td>00010</td><td>4 lines</td></tr><tr><td>...</td><td></td></tr><tr><td>11101</td><td>31 lines</td></tr><tr><td>11110</td><td>32 lines</td></tr><tr><td>11111</td><td>33 lines</td></tr></tbody></table>	<u>N₄ – N₀</u>	<u>n-line inversion</u>	00000	Exit n-line inversion	00001	3 lines	00010	4 lines	...		11101	31 lines	11110	32 lines	11111	33 lines																				
<u>N₄ – N₀</u>	<u>n-line inversion</u>																																					
00000	Exit n-line inversion																																					
00001	3 lines																																					
00010	4 lines																																					
...																																						
11101	31 lines																																					
11110	32 lines																																					
11111	33 lines																																					
0101 0B ₂ B ₁ B ₀	Set LCD Bias	<p>Sets the LCD bias from 1/4 ~ 1/9 according to B₂B₁B₀:</p> <p>000: 1/4 bias 001: 1/5 bias 010: 1/6 bias 011: 1/7 bias 100: 1/8 bias 101: 1/9 bias (POR) 110: 1/9 bias 111: 1/9 bias</p>																																				
0110 01B ₁ B ₀	Set DC-DC Converter Factor	<p>Set the DC-DC multiplying factor from 2X to 5X</p> <p>B₁B₀: 00: 3X (POR) 01: 4X 10: 5X 11: invalid</p>																																				
1000 0001 XXC ₅ C ₄ C ₃ C ₂ C ₁ C ₀	Set Contrast Control Register	<p>The second command sets one of the 64 contrast levels. The darkness increase as the contrast level increase.</p>																																				

Bit Pattern	Command	Description
1000 1000 WB ₃ WB ₂ WB ₁ WB ₀ WA ₃ WA ₂ WA ₁ WA ₀	Set White Mode, Frame 2 nd & 1 st	Set gray scale mode and register. These are two-byte commands used to specify the contrast levels for the gray scale, 4 levels available. After power on reset: WA0~3 = WB0~3 = WC0~3 = WD0~3 = 0000 LA0~3 = 1001 LB0~3 = LC0~3 = LD0~3 = 0000 DA0~3 = DB0~3 = DC0~3 = 1001 DD0~3 = 0000 BA0~3 = BB0~3 = BC0~3 = BD0~3 = 1001
1000 1001 WD ₃ WD ₂ WD ₁ WD ₀ WC ₃ WC ₂ WC ₁ WC ₀	Set White Mode, Frame 4 th & 3 rd	
1000 1010 LB ₃ LB ₂ LB ₁ LB ₀ LA ₃ LA ₂ LA ₁ LA ₀	Set Light Gray Mode, Frame 2 nd & 1 st	
1000 1011 LD ₃ LD ₂ LD ₁ LD ₀ LC ₃ LC ₂ LC ₁ LC ₀	Set Light Gray Mode, Frame 4 th & 3 rd	
1000 1100 DB ₃ DB ₂ DB ₁ DB ₀ DA ₃ DA ₂ DA ₁ DA ₀	Set Dark Gray Mode, Frame 2 nd & 1 st	
1000 1101 DD ₃ DD ₂ DD ₁ DD ₀ DC ₃ DC ₂ DC ₁ DC ₀	Set Dark Gray Mode, Frame 4 th & 3 rd	
1000 1110 BB ₃ BB ₂ BB ₁ BB ₀ BA ₃ BA ₂ BA ₁ BA ₀	Set Black Mode, Frame 2 nd & 1 st	
1000 1111 BD ₃ BD ₂ BD ₁ BD ₀ BC ₃ BC ₂ BC ₁ BC ₀	Set Black Mode, Frame 4 th & 3 rd	
1001 0 FRC PWM1 PWM0	Set PWM and FRC	Set PWM and FRC for gray-scale operation. FRC = 0 : 4-frame (POR) FRC = 1 : 3-frame PWM = 00 & 01 : 9-levels (POR) PWM = 10 : 12-levels PWM = 11 : 15-levels
1010 000S ₀	Set Segment Re-map	MODE=L S ₀ =0: column address 00H is mapped to SEG0 (POR) S ₀ =1: column address 67H is mapped to SEG0 MODE=H S ₀ =0: column address 00H is mapped to SEG0 (POR) S ₀ =1: column address 5FH is mapped to SEG0
1010 001C ₀	Set Icon Enable	C ₀ =0: Disable icon row (Mux = 16 to 64, POR) C ₀ =1: Enable icon row (Mux = 17 to 65)
1010 010E ₀	Set Entire Display On/Off	E ₀ =0: Normal display (display according to RAM contents, POR) E ₀ =1: All pixels are ON regardless of the RAM contents *Note: This command will override the effect of "Set Normal/Invert Display"
1010 011R ₀	Set Normal/Inverse Display	R ₀ =0: Normal display (display according to RAM contents, POR) R ₀ =1: Invert display (ON and OFF pixels are inverted) *Note: This command will not affect the display of the icon lines
1010 1001	Set Power Save Mode	Sleep Mode: Oscillator: OFF LCD Power Supply: OFF COM/SEG Outputs: V _{SS}
1010 1011	Start Internal Oscillator	This command starts the internal oscillator. Note that the oscillator is OFF after reset, so this instruction must be executed for initialization
1010 111D ₀	Set Display On/Off	Turn the display on and off without modifying the content of the RAM. (0: off, 1: on) This command has priority over Entire Display On/Off and Inverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

Memory Content		Gray Mode
1 st Byte	2 nd Byte	
0	0	White
0	1	Light Gray
1	0	Dark Gray
1	1	Black

Bit Pattern	Command	Description
1011 P ₃ P ₂ P ₁ P ₀	Set Page Address	Select the page of display RAM to be addressed. Pages 0-8 are valid.
1100 S ₀ XXX	Set COM Output Scan Direction	Set the COM (row) scanning direction. (0: COM0 →COM63, 1: COM63 →COM0)
1110 0001	Exit Power-save Mode	Return the driver/controller from the sleep mode.
1110 0010	Software Reset	Reset some functions of the driver/controller. See Reset Section below for more details.
1110 0100	Exit N-line Inversion	Release the driver/controller from N-line inversion mode.
1101 1F ₂ F ₁ F ₀	Set Frame Frequency	This command is used to set the frame frequency. F ₂ F ₁ F ₀ Frame Frequency 000 70 001 78.5 010 88.5 011 100 100 115 101 130 110 140 111 157.5(POR)

Table 6 – Extended Command Table

Bit Pattern	Command	Comment
1000 0010 0001 X ₃ X ₂ X ₁ X ₀	OTP setting	This command set the offset value of contrast X ₃ X ₂ X ₁ X ₀ 0000 : original contrast 0001 : original contrast + 1 step 0010 : original contrast + 2 steps 0011 : original contrast + 3 steps 0100 : original contrast + 4 steps 0101 : original contrast + 5 steps 0110 : original contrast + 6 steps 0111 : original contrast + 7 steps 1000 : original contrast - 8 steps 1001 : original contrast - 7 steps 1010 : original contrast - 6 steps 1011 : original contrast - 5 steps 1100 : original contrast - 4 steps 1101 : original contrast - 3 steps 1110 : original contrast - 2 steps 1111 : original contrast - 1 step
1000 0011	OTP programming	This command start program LCD driver with OTP offset value. This command only execute once. No effect on the second run.
1111 0010 00X ₀ 0 0000	Select Oscillator Source	Select external oscillator input form CL pin. X ₀ = 0 : (POR) internal RC oscillator X ₀ = 1 : external square wave
1111 1101 xxxx 0X ₀ 10	Lock/Unlock Interface	X ₂ = 0 : Unlock the IC. The driver accepts any command and data written. X ₂ = 1 : Lock the IC. The driver ignores all command and data written, except the unlock command or pin reset.
Other than above	Reserved	

8.1 I²C-bus write data and read register status

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8 for the write mode of I²C-bus in chronological order.

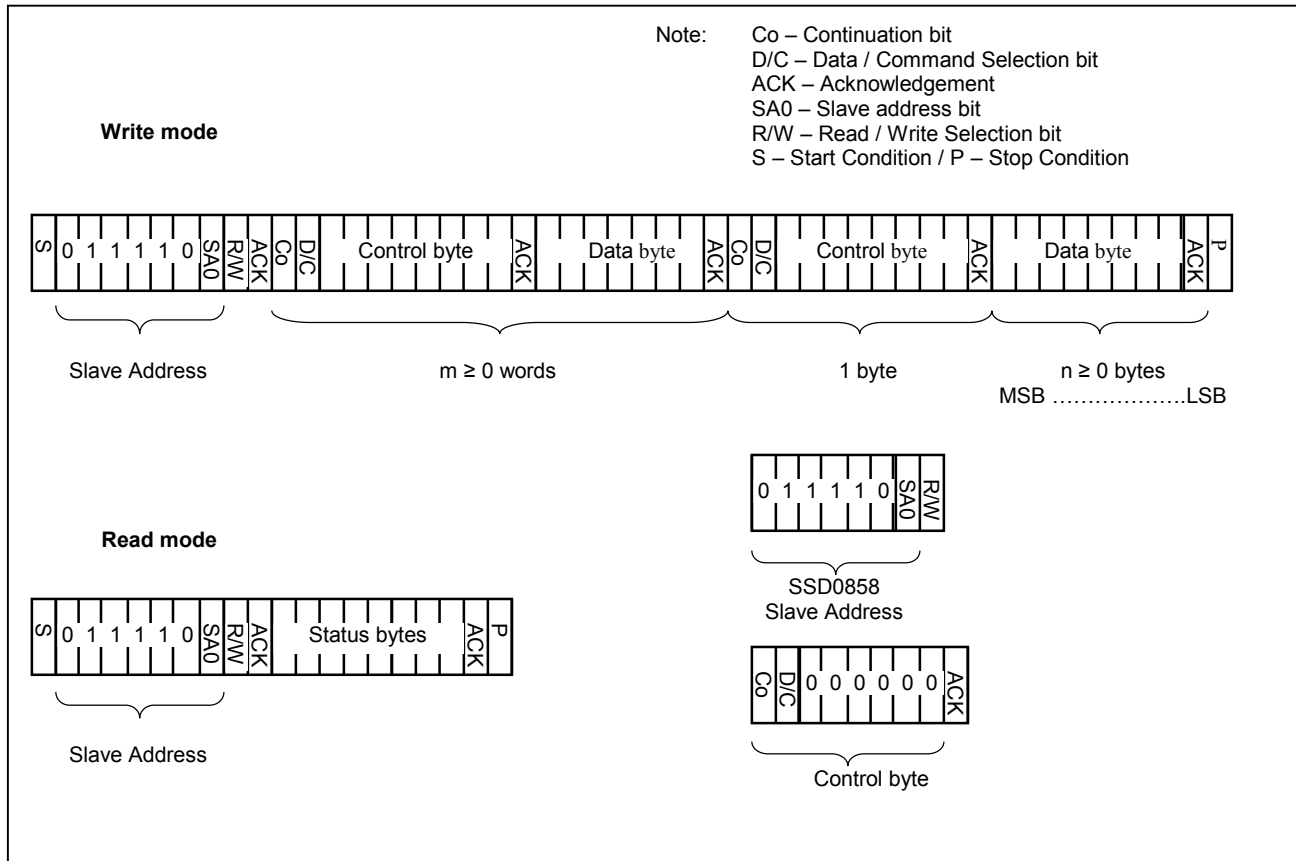


Figure 8 - I²C-bus data format

Write mode

- 1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 9. The start condition is established by pulling the SDA from high to low while the SCL stays high.
- 2) The slave address is following the start condition for recognition use. For the SSD0858, the slave address is either "b0111100" or "b0111101" by changing the SA0 to high or low.
- 3) The write mode is established by setting the R/W bit to logic "0".
- 4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W bit. Please refer to the Figure 10 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as that the SDA line is pulled down during the high period of the acknowledgement related clock pulse.
- 5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C bits following by six "0"s.
 - a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.

- b. The D/C bit determines the next data byte is acted as a command or a data. If the D/C bit is set to logic "0", it defines the following data byte as a command. If the D/C bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
- 6) Acknowledge bit will be generated after receiving each control byte or data byte.
- 7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 9. The stop condition is established by pulling the "SDA in" from low to high while the "SCL" stays high.

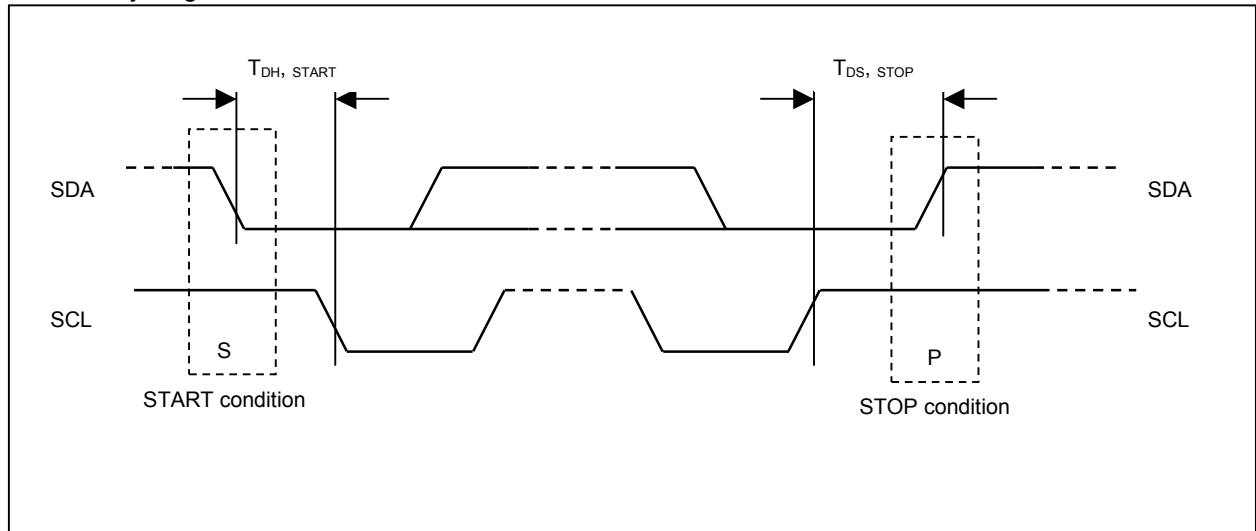


Figure 9 - Definition of the start and stop condition

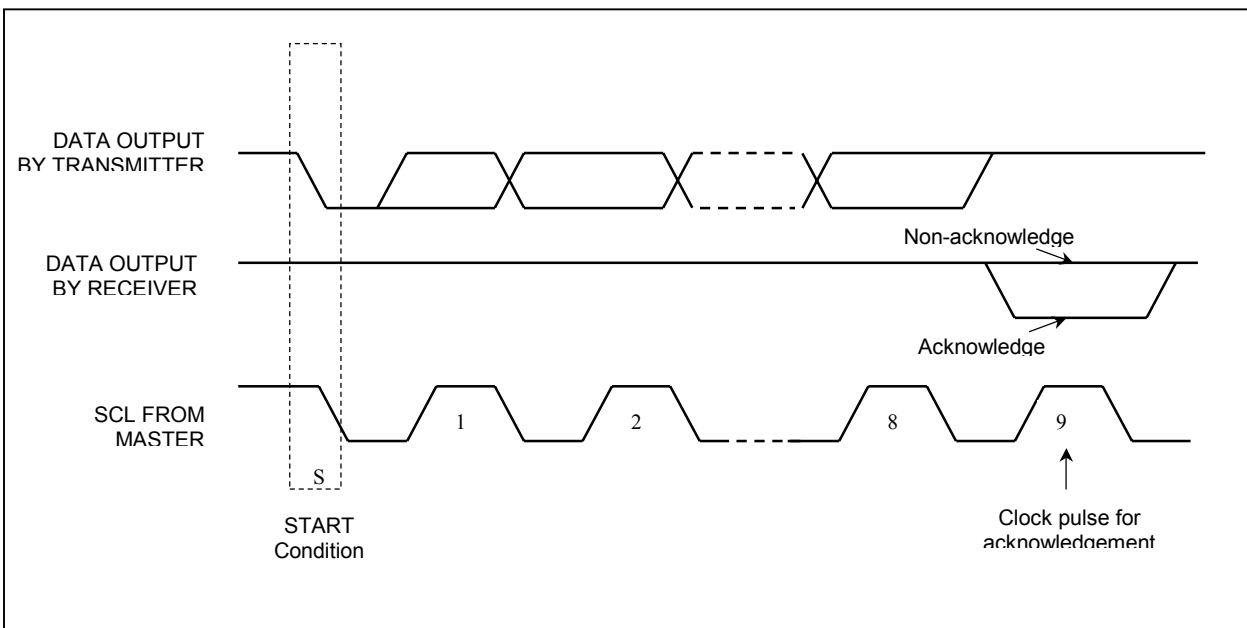


Figure 10 - Definition of the acknowledgement condition

Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must be kept at a stable state within the "high" period of the clock pulse. Please refer to the Figure 11 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is low.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

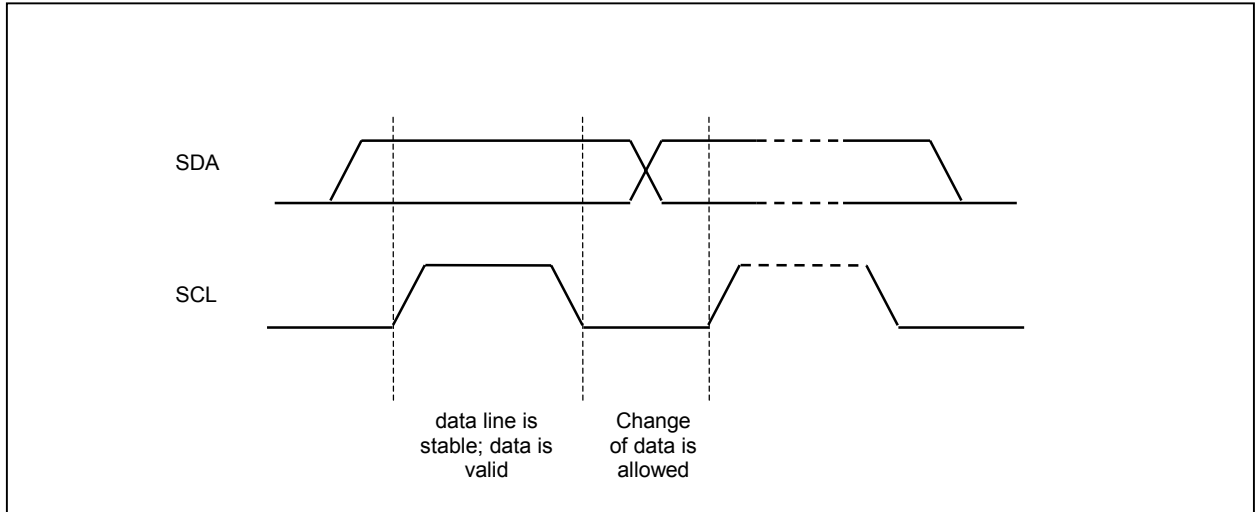


Figure 11 - Definition of the data transfer condition

Read mode (Read status register)

Not support in SSD0858

9 COMMAND DESCRIPTIONS

9.1 Set Lower Column Address

This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>95 when MODE=H OR >103 when MODE=L).

9.2 Set Upper Column Address

This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>95 when MODE=H OR >103 when MODE=L).

9.3 Set Internal Regulator Resistor Ratio

This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref} \quad , \text{where } V_{ref} = 1.7V$$

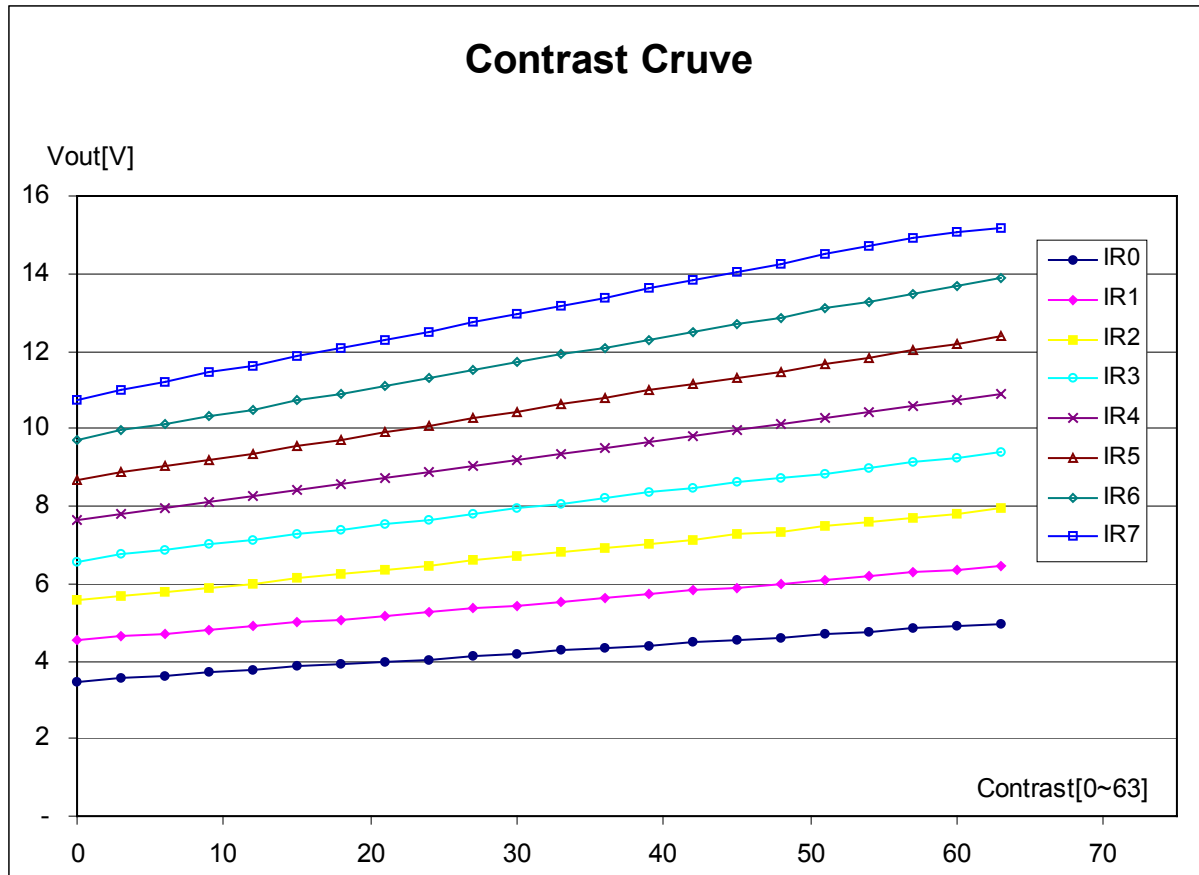


Figure 12 - Contrast Control Voltage Range Curve (TC=-0.14%/°C; $V_{DD}=2.775V$; $V_{CI}=3.5V$)

9.4 Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three power relating sub-circuits could be turned on/off by this command.

Internal voltage booster is used to generate the highest positive voltage supply internally from the voltage input ($V_{CI} - V_{SS}$).

Internal regulator is used to generate the LCD driving voltage.

Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2} , V_{L3} , V_{L4} , V_{L5}) from the internal regulator output, V_{out} . External voltage sources should be fed into this driver if this circuit is turned off.

9.5 Set TC Value

This command is to set 1 out of 5 different temperature coefficients in order to match various liquid crystal temperature grades.

9.6 Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to 7.

9.7 Set Display Offset

The second command specifies the mapping of display start line (COM0 if display start line register equals to 0) to one of ROW0-63. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

9.8 Set Multiplex Ratio

This command switches default 64 multiplex mode to any multiplex from 16 to 64, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped to 17 to 65. The chip pads ROW0-ROW63 will be switched to corresponding COM signal output as specified in Table 2.

9.9 Set N-line Inversion

Number of line inversion is set by this command for reducing crosstalk noise. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled.

It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change.

9.10 Set LCD Bias

This command selects a suitable bias ratio (1/4 to 1/9) required for driving the particular LCD panel in use. The POR is set to 1/9 bias.

9.11 Set DC-DC Converter Factor

Internal DC-DC converter factor is set by this command. For SSD0858, 2X to 5X multiplying factors could be selected. 2X to 5X factors are selected using this command.

9.12 Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing V_{out} of the LCD drive voltage provided by the On-Chip power circuits. V_{OUT} is set with 64 steps (6-bit) contrast control register. It is a compound commands:

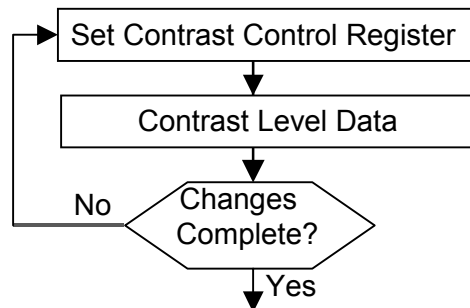


Figure 13 - Contrast Control Flow

9.13 Set Gray Scale Mode (White/Light Gray/Dark Gray/Black)

Command 88(hex) to 8F(hex) are used to specify the four gray levels' pulse width at the four possible frames. The four gray levels are called white, light gray, dark gray and black. Each level is defined by 4 registers for 4 consecutive frames. For example, WA is a 4-bit register to define the pulse width of the 1st frame in White mode. WB is a register for 2nd frame in White mode etc. Each command specifies two registers.

For 4 FRC,

Memory Content		Gray Mode	FRAME			
1 st Byte	2 nd Byte		1 st	2 nd	3 rd	4 th
0	0	White	WA	WB	WC	WD
0	1	Light Gray	LA	LB	LC	LD
1	0	Dark Gray	DA	DB	DC	DD
1	1	Black	BA	BB	BC	BD

For 3 FRC,

Memory Content		Gray Mode	FRAME			
1 st Byte	2 nd Byte		1 st	2 nd	3 rd	4 th (No use)
0	0	White	WA	WB	WC	WD (XX)
0	1	Light Gray	LA	LB	LC	LD (XX)
1	0	Dark Gray	DA	DB	DC	DC (XX)
1	1	Black	BA	BB	BC	BC (XX)

Example for pure PWM mode:

No. of level	RAM Content								Gray Scale mode and Register (3/4 FRC)			
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	Dark Mode	Dark Gray Mode	Light Gray Mode	White Mode
15-levels	1	1	1	0	0	1	0	0	F,F,F,F	A,A,A,A	5,5,5,5	0,0,0,0
12-levels	1	1	1	0	0	1	0	0	C,C,C,C	8,8,8,8	4,4,4,4	0,0,0,0
9-levels	1	1	1	0	0	1	0	0	9,9,9,9	6,6,6,6	3,3,3,3	0,0,0,0
LCD panel display												

Example for pure FRC mode:

No. of Frame	RAM Content								Gray Scale mode and Register (15PWM)			
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	Dark Mode	Dark Gray Mode	Light Gray Mode	White Mode
3-FRC	1	1	1	0	0	1	0	0	F,F,F,F	F,F,0,0	F,0,0,0	0,0,0,0
4-FRC	1	1	1	0	0	1	0	0	F,F,F,F	F,F,F,0	F,0,0,0	0,0,0,0
LCD panel display												

9.14 Set PWM and FRC

This command is used to select the number of frames used in frame rate control, and the number of levels in the pulse width modulation.

9.15 Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to Figure 4.

9.16 Set Icon Enable

This command enable/disable the Icon displays.

9.17 Set Entire Display On/Off

This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. To execute this command, Set Display On command must be sent in advance.

9.18 Set Normal/Inverse Display

This command sets the display to be either normal/inverse. In normal display, a RAM data of 1 indicates an "ON" pixel. In reverse display, a RAM data of 0 indicates an "ON" pixel. The icon line is not affected by this command.

9.19 Set Power Save Mode

To force the chip to enter Standby or Sleep Mode. LSB of the command will define which mode will be entered.

9.20 Start Internal Oscillator

After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

9.21 Set Display On/Off

This command turns the display on/off, by the value of the LSB.

9.22 Set Page Address

This command indicates the positions of the page address from 0 to 8 in GDDRAM. Refer to Figure 4.

9.23 Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

9.24 Exit Power Save Mode

This command releases the chip from Sleep Mode and return to normal operation.

9.25 Software Reset

This command causes some of the internal status of the chip to be initialized:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 2.84 (IR0)
Contrast	20H	
Data display length	0	
FRC, PWM Mode	0	4FRC, 9PWM
White Palette	(0, 0, 0, 0)	
Light Gray Palette	(9, 0, 0, 0)	
Dark Gray Palette	(9, 9, 9, 0)	
Black Palette	(9, 9, 9, 9)	

9.26 Exit N-line Inversion Mode

This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

9.27 Set frame frequency

The next command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 157.5Hz at 64 mux after POR.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features, on top of general ones, designed for the chip.

9.28 OTP setting and programming

OTP (One Time Programming) is a method to adjust V_{OUT} . In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules.

OTP setting and programming should include two major steps of (1) Find the OTP offset and (2) OTP programming as following,

Step 1. Find OTP offset

- (1) Hardware Reset (sending an active low reset pulse to \overline{RES} pin)
- (2) Send original initialization routines
- (3) Set and display any test patterns
- (4) Adjust the contrast value (0x81, 0x00~0x3F) until there is the best visual contrast
- (5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:

Contrast value of original initialization = 0x20

Contrast value of the best visual contrast = 0x24

OTP setting steps = 0x24 - 0x20 = +4

OTP setting commands should be (0x82, 0x14)

Example 2:

Contrast value of original initialization = 0x20

Contrast value of the best visual contrast = 0x1B

OTP setting steps = 0x1B - 0x20 = -5

OTP setting commands should be (0x82, 0x1B)

Step 2. OTP programming

- (6) Hardware Reset (sending an active low reset pulse to $\overline{\text{RES}}$ pin)
- (7) Enable Oscillator (0xAB)
- (8) Connect an external V_{OUT} (see diagram below)
- (9) Send OTP setting commands that we find in step 1 (0x82, 0x10~0x1F)
- (10) Send OTP programming command (0x83)
- (11) Wait at least 2 seconds
- (12) Hardware Reset

Verify the result by repeating step 1. (2) – (3)

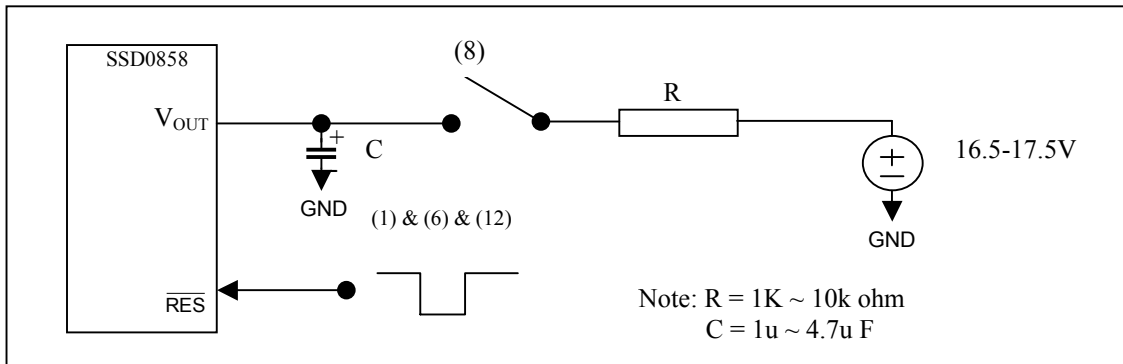


Figure 14 - OTP programming circuitry

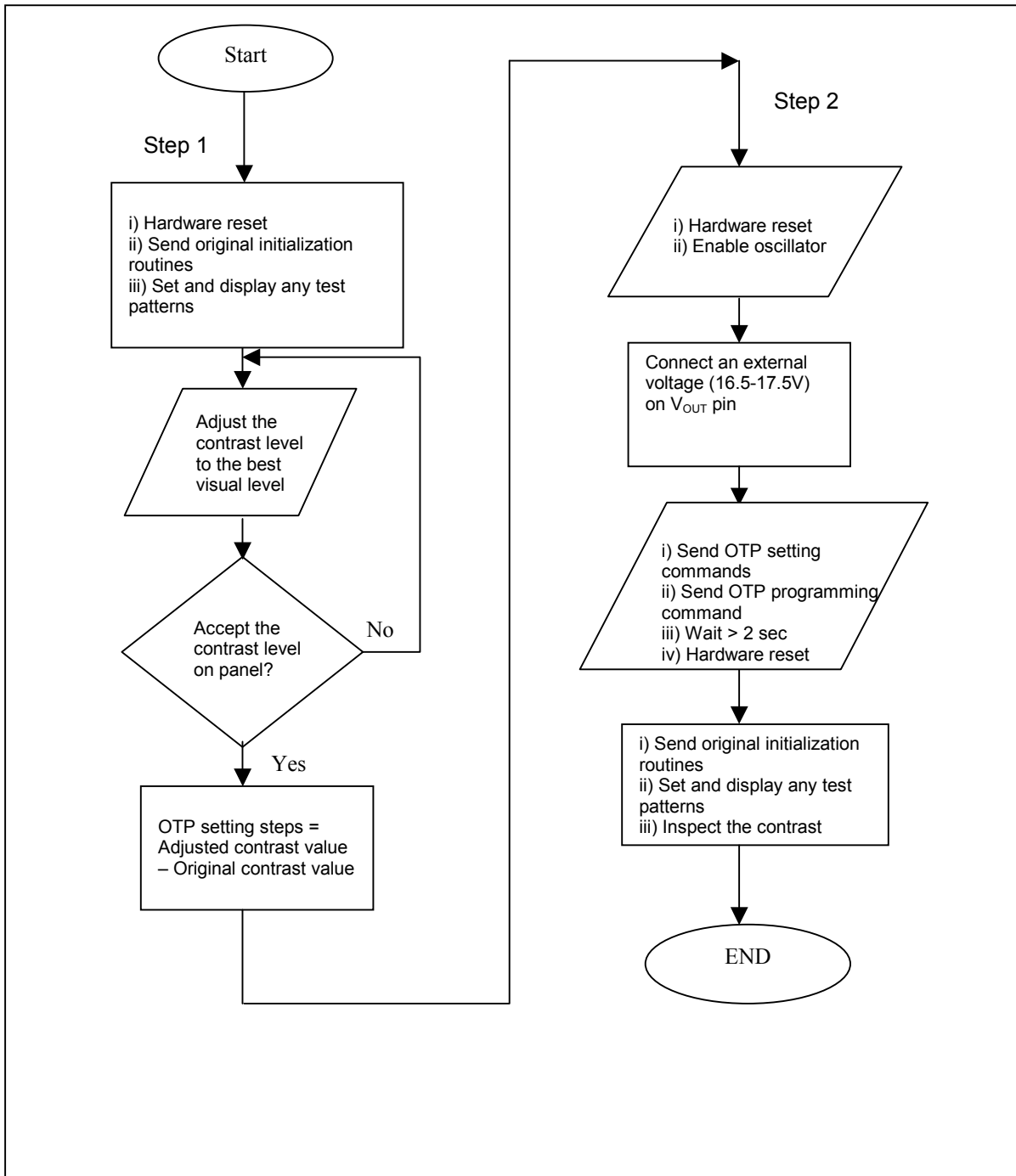


Figure 15 - Flow chart of OTP program

OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin
2. COMMAND(0XAB) \\ Enable oscillator
 COMMAND(0X2F) \\ Turn on the internal voltage booster, internal regulator and output op-amp buffer; Select booster level
3. COMMAND(0X48) \\ Set Duty ratio
 COMMAND(0X40) \\ 64Mux
 COMMAND(0X55) \\ Set Biasing ratio (1/9 BIAS)
4. COMMAND(0X81) \\ Set target gain and contrast.
 COMMAND(0X2D) \\ Contrast = 45
 COMMAND(0X24) \\ Gain = 6.3
5. \\ Set target display contents
 COMMAND(0XB0) \\ Set page address
 COMMAND(0x00) \\ Set lower nibble column address
 COMMAND(0X10) \\ Set higher nibble column address
 DATA(...) \\ Write test patterns to GDDRAM
 COMMAND(0XAF) \\ Set Display On
6. OTP offset calculation... target OTP offset value is +3

OTP programming:

7. Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin
8. COMMAND(0XAB) \\ Enable Oscillator
9. Connect an external V_{OUT} (16.5V-17.5V)
10. COMMAND(0X82) \\ Set OTP offset value to +3 (0011)
 COMMAND(0X13) \\ 0001 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value
11. COMMAND(0X83) \\ Send the OTP programming command.
12. Wait at least 2 seconds for programming wait time.
13. Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin

Verify the result:

14. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel

9.29 Select Oscillator Source

This command enables the external clock input from CL pin and expected external square wave is 726kHz.

9.30 Lock/Unlock Interface

After sending the lock command, the interface will be disabled until the unlock command is received. The lock command is suggested whenever the LCD driver will not be accessed for some period. This can minimize the incorrect data or commands written due to noisy interface.

MAXIMUM RATINGS

Table 7 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 5.5	V
V_{CC}		$V_{SS} - 0.3$ to $V_{SS} + 12.0$	V
V_{CI}	Booster Supply Voltage	V_{DD} to +5.5	V
V_{in}	Input Voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to range $V_{SS} < \text{or} = (V_{IN} \text{ or } V_{OUT}) < \text{or} = V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}). Unused outputs must be open. This device may be light sensitive. Caution should be taken to avoid exposure of this device any light source during normal operation. This device is not radiation protected.

10 DC CHARACTERISTICS

Table 8 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS} , $V_{DD} = 1.8$ to $3.3V$, $T_A = -40$ to $85^\circ C$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	1.8	2.7	3.3	V
V_{CI}	Booster Voltage Supply Pin	(Absolute value referenced to V_{SS})	V_{DD}	-	3.6	V
V_{REF}	Internal Reference Voltage ($25^\circ C$, $-0.14\%/^\circ C$)	Internal Reference Voltage Source Enabled (REF pin pulled High), V_{EXT} pin NC.	-	1.7	-	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, Voltage Generator On, 5X DC-DC Converter Enabled, Write accessing, $T_{cyc} = 3.3MHz$, Frame Freq.=157.5Hz, Display On.	-	0.9	2	mA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} & V_{CI} Pins)	$V_{DD} = V_{CI} = 2.7V$, Voltage Generator ON, internal Divider Enabled. Read/Write Halt, Frame Freq. = 157.5Hz, Display On, $V_{out} = 10.0V$.	-	220	300	μA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} & V_{CI} Pins)	$V_{DD} = V_{CI} = 1.8V$, Voltage Generator OFF, DC-DC Converter Disabled, Internal Divider Disable. Read/Write Halt, Frame Freq. = 157.5Hz, Display On, $V_{out} = 8.0V$, no panel loading.	-	75	150	μA
I_{VCI}	Operating Current (V_{CI} Pin) ($25^\circ C$, $-0.14\%/^\circ C$)	$V_{DD}=V_{CI}=2.75V$, Voltage Generator On, 4X DC-DC Converter Enabled, Internal Divider Enabled. Read/Write Halt, Frame Freq. = 157.5Hz, Display On, $V_{out} = 7.5V$, no panel loading, checker board pattern.		220	300	μA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, LCD Driving Waveform Off, Oscillator Off, Read/Write halt.	-	1.2	2.5	μA
V_{OUT}	LCD Driving Voltage Generator Output (V_{out} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Regulator Enabled, Frame Freq.=157.5Hz,	4.0	-	12.0	V
	DC-DC Converter Efficiency	80uA panel loading	-	85	-	%
V_{LCD}	LCD Driving Voltage Input (V_{out} Pin)	Voltage Generator Disabled	4.0	-	12.0	V
V_{OH1}	Output High Voltage (SCL)	$I_{OUT} = +500\mu A$	$0.8 \cdot V_{DD}$	-	V_{DD}	V
V_{OL1}	Out Low Voltage (SCL)	$I_{OUT} = -500\mu A$	0	-	$0.2 \cdot V_{DD}$	V
V_{OUT}	LCD Driving Voltage Source (V_{out} Pin)	Regulator Enabled (V_{out} voltage depends on Internal contrast Control)	V_{DD}	-	12.0	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OUT}	LCD Driving Voltage Source (V _{out} Pin)	Regulator Disable	-	Floating	-	V
V _{IH1}	Input high voltage (RES, SDA, SCL, SA0)		0.8*V _{DD}	-	V _{DD}	V
V _{IL1}	Input low voltage (RES, SDA, SCL, SA0)		0	-	0.2*V _{DD}	V
V _{OUT}	LCD Display Voltage Output	Bias Divider Enabled, 1:a bias ratio	-	V _{OUT}	-	V
V _{L5}	(V _{out} , V _{L5} , V _{L4} , V _{L3} , V _{L2} Pins)		-	(a-1)/a*V _{OUT}	-	V
V _{L4}			-	(a-2)/a*V _{OUT}	-	V
V _{L3}			-	2/a* V _{OUT}	-	V
V _{L2}			-	1/a* V _{OUT}	-	V
V _{OUT}	LCD Display Voltage Input (V _{out} , V _{L5} , V _{L4} , V _{L3} , V _{L2} Pins)	Voltage reference to V _{SS} , External Voltage Generator, Bias Diver Disabled	V _{L5}	-		V
V _{L5}			V _{L4}	-	V _{OUT}	V
V _{L4}			V _{L3}	-	V _{L5}	V
V _{L3}			V _{L2}	-	V _{L4}	V
V _{L2}			V _{SS}	-	V _{L3}	V
I _{OH}	Output High Current Source (SDA, SCL, SA0)	Output Voltage=V DD -0.4V	50	-	-	μA
I _{OL}	Output Low Current Drain (SDA, SCL, SA0)	Output Voltage = 0.4V	-	-	-50	μA
I _{OZ}	Output Tri-state Current Source (SDA, SCL)		-1	-	1	μA
I _{IL} /I _{IH}	Input Current (RES, SDA, SCL, SA0)		-1	-	1	μA
C _{IN}	Input Capacitance (all logic pins)		-	5	7.5	PF
ΔV _{OUT}	Variation of Vout Output (1.8V < V _{DD} < 3.3V)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	±2	-	%
V _{ref}	Reference Voltage (T= 25°C)		1.65	1.7	1.75	V
	Reference Voltage (T= -20°C)		1.76	1.81	1.86	V
	Reference Voltage (T= 70°C)		1.54	1.59	1.64	V
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	Voltage Regulator Enabled	0	-0.01	-0.02	%
PTC1	Temperature Coefficient 1*	Voltage Regulator Enabled	-0.025	-0.035	-0.045	%
PTC2	Temperature Coefficient 2*	Voltage Regulator Enabled	-0.04	-0.05	-0.06	%
PTC3	Temperature Coefficient 3*	Voltage Regulator Enabled	-0.07	-0.083	-0.096	%
PTC4	Temperature Coefficient 4* (POR)	Voltage Regulator Enabled	-0.126	-0.14	-0.154	%

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{OUT} 50^{\circ}C - V_{OUT} \text{ at } 0^{\circ}C}{50^{\circ}C - 0^{\circ}C} \times \frac{1}{V_{OUT} \text{ at } 25^{\circ}C} \times 100\%$$

11 AC CHARACTERISTICS

Table 9 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS} , V_{DD} , $V_{CI} = 2.7V$, $T_A = -40$ to $85^\circ C$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{FRM}	Frame Frequency	Display ON, Set 104 x 64 Graphic Display Mode, Icon Line Disabled	-	157.5	-	Hz
F_{OSC}	Oscillator frequency	Display ON, Set 104 x 64 Graphic Display Mode, Icon Line Disabled	-	726	-	kHz

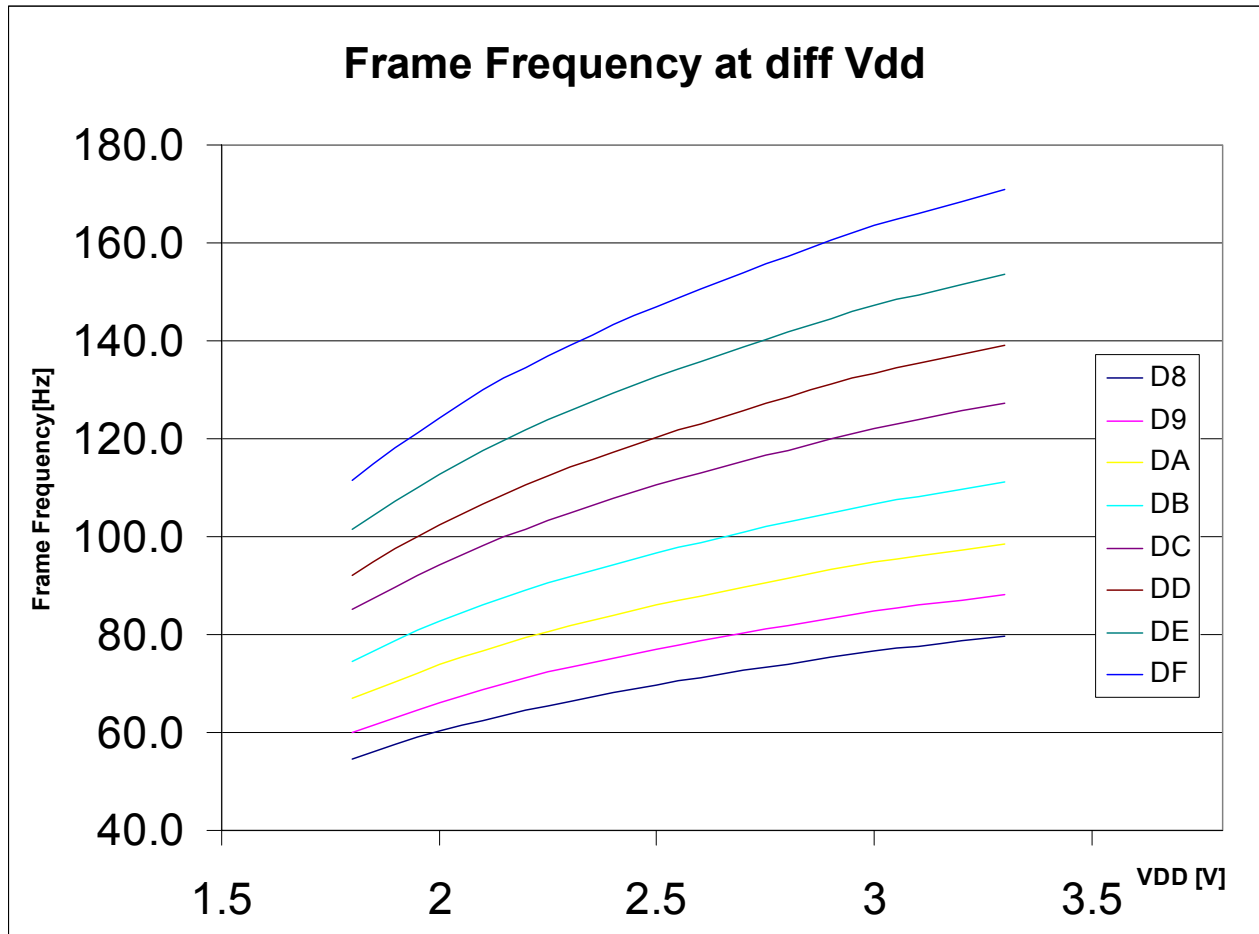


Figure 16 - Frame Frequency at different VDD ($T_A = 25^\circ C$).

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	I ² C-bus Clock frequency, SCL	0	-	400	kHz
T_{CLKL}	I ² C-bus Clock Low period, SCL	1.3	-	-	s
T_{CLKH}	I ² C-bus Clock high period, SCL	0.6	-	-	s
T_{DSW}	I ² C-bus Data Setup time, SDA	100	-	-	s
T_{DHW}	I ² C-bus Data Hold time, SDA	0.3	-	0.9	s
T_R	Rise time between SDA & SCL	$20+0.1C_{BUS}$	-	300	ns
T_F	Fall time between SDA & SCL	$20+0.1C_{BUS}$	-	300	ns
C_{BUS}	Capacitive loadings at each I ² C-bus channel	-	-	400	pF
T_{DH_START}	I ² C-bus Hold time, START condition	0.6	-	-	s
T_{DS_STOP}	I ² C-bus Setup time, STOP condition	0.6	-	-	s

Table 10 - I²C-bus timing Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS} , V_{DD} = 1.8 to 3.3V, T_A = -20 to +70°C)

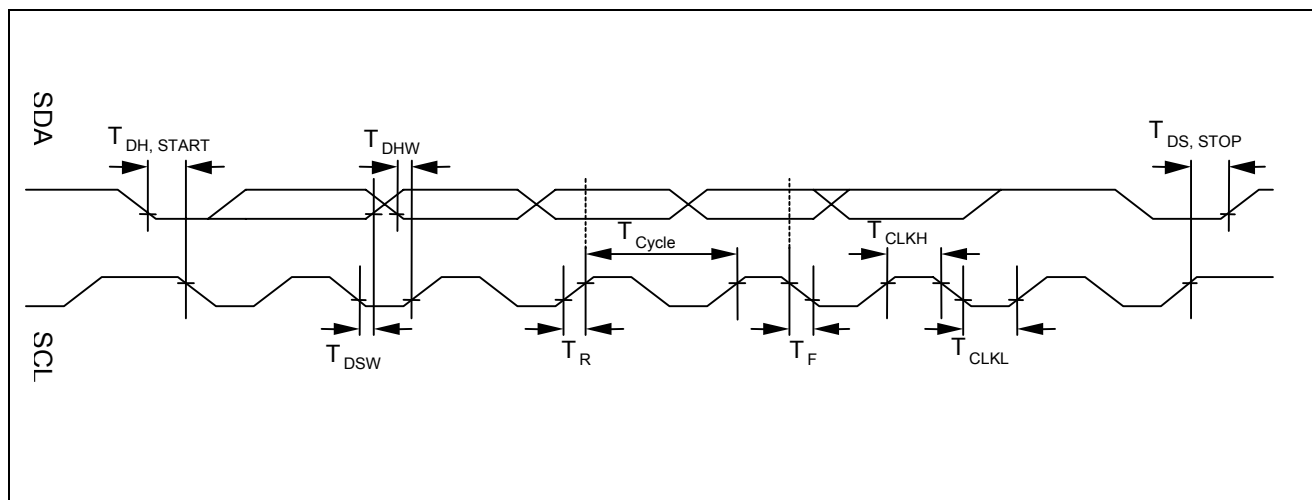


Figure 17 - I²C data bus Interface driving waveform

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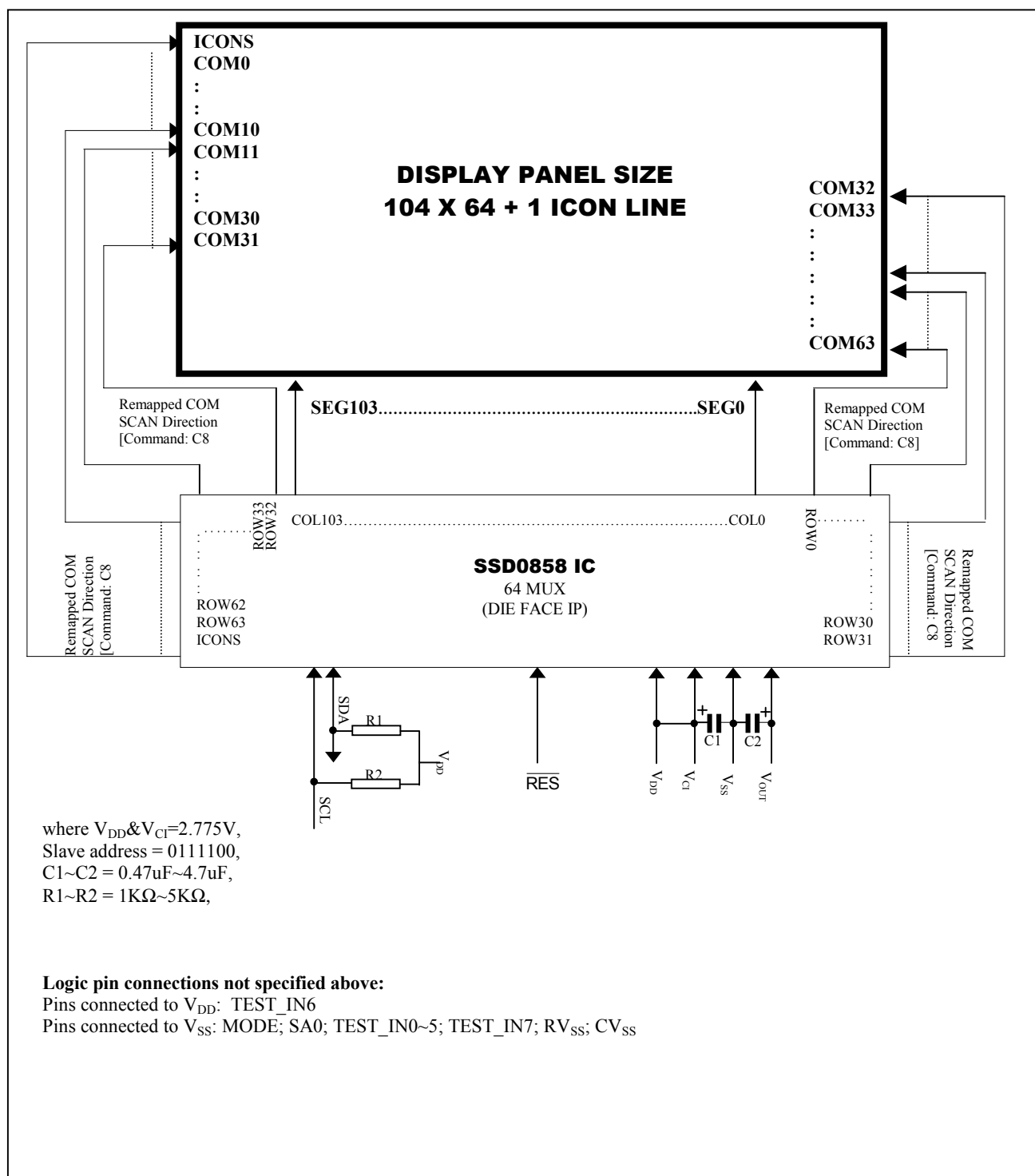


Figure 18 - Typical Application (I²C Interface)

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