

SSSB153

STM16 - STM1 DeMultiplexer

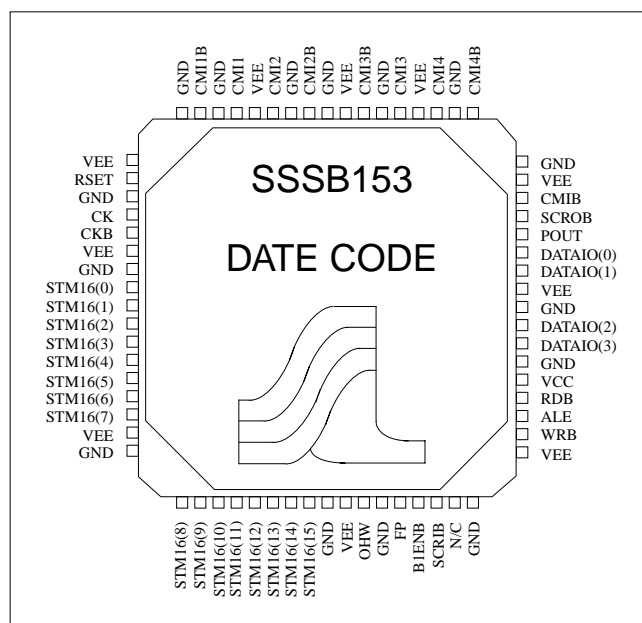
SDH Product Range

STM16 - STM1 DEMULTIPLEXER

The SSSB153 receives STM16 frames in 2 byte parallel form, and sends out selected STM1 frames in bit serial form. Each SSSB153 selects up to four STM1 frames out of the incoming STM16 frame. Up to four SSSB153 devices, together with an SSSB149, are used to form a complete 2.5 GHz STM16 to STM1 demultiplexer for SDH communication applications.

FEATURES

- 16 bit parallel STM16 input
- ECL 100k compatible STM16 interface
- Interfaces with SSSB149
- Four 75 Ω differential STM1 outputs
- 155.52MBit/s NRZ or 311.04 MBaud CMI serial data output format
- Built in scrambling and parity circuits
- TTL I/O for control interface
- High performance Silicon Bipolar process
- Twin power supply (-5V & +5V)
- Low dissipation (2.5W)
- 68 pin J-leaded ceramic package with heat sink
- Meets ITU-T Recommendations



FUNCTIONAL OVERVIEW

The SSSB153 accepts data as STM16 frames in 16 bit parallel form at a clock speed of 155MHz, and has 4 differential 75 Ω output channels. The output channels carry STM1 frames in bit serial form in either 155MBit/s NRZ or 311 MBaud CMI format. Each output channel can be any one of the 16 STM1 frames contained in the STM16 input frame.

The device includes circuits to monitor frame detect failure and control the SSSB149 synchronisation logic, circuits to perform parity checking and descrambling of the STM16 input frames, and circuits for parity generation, scrambling and CMI code conversion of the STM1 serial output frames

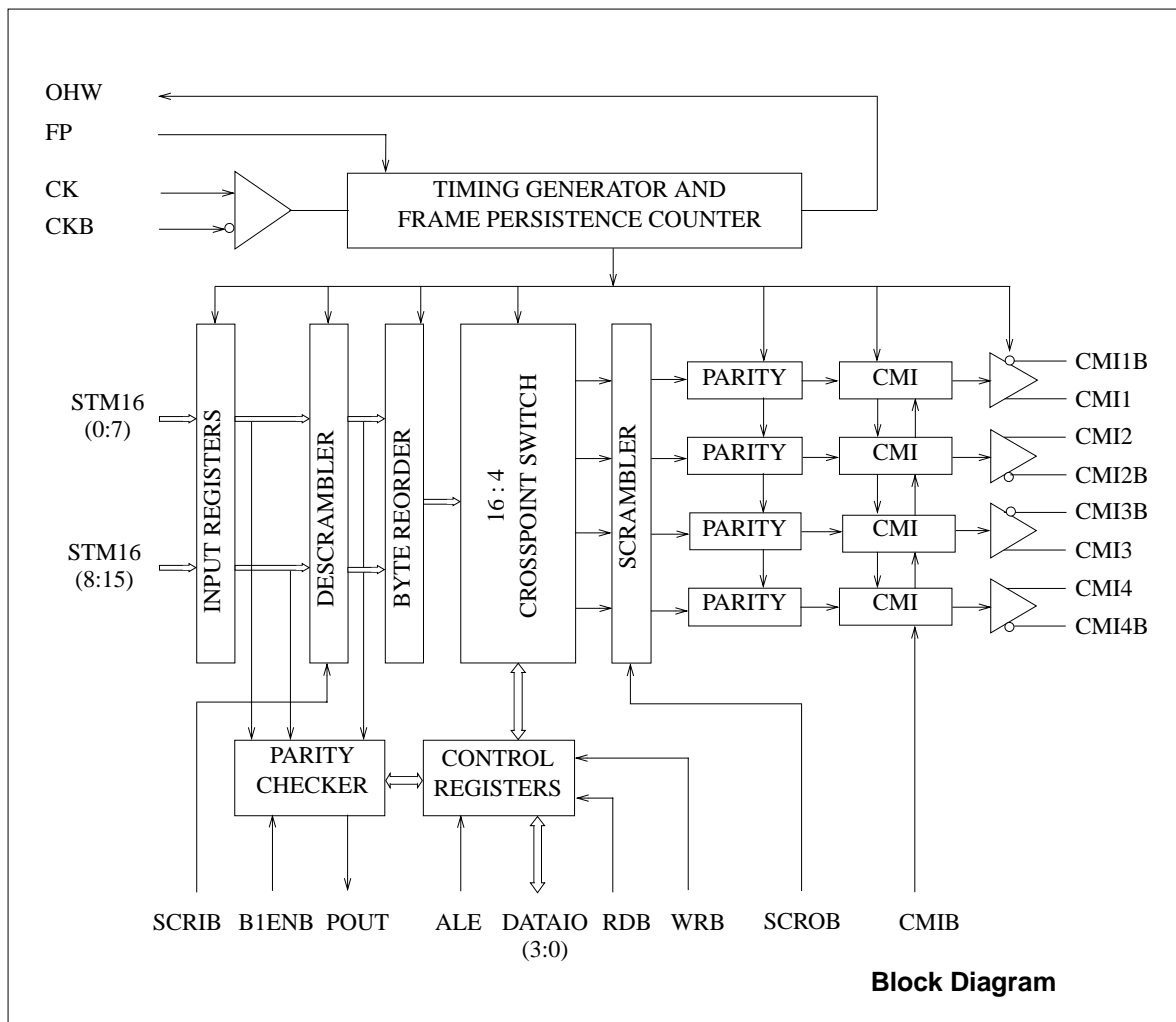
The SSSB153 has a TTL compatible control interface which is used for STM1 frame selection to the 4 output channels, and for access to the parity checking circuit.

FUNCTIONAL DESCRIPTION

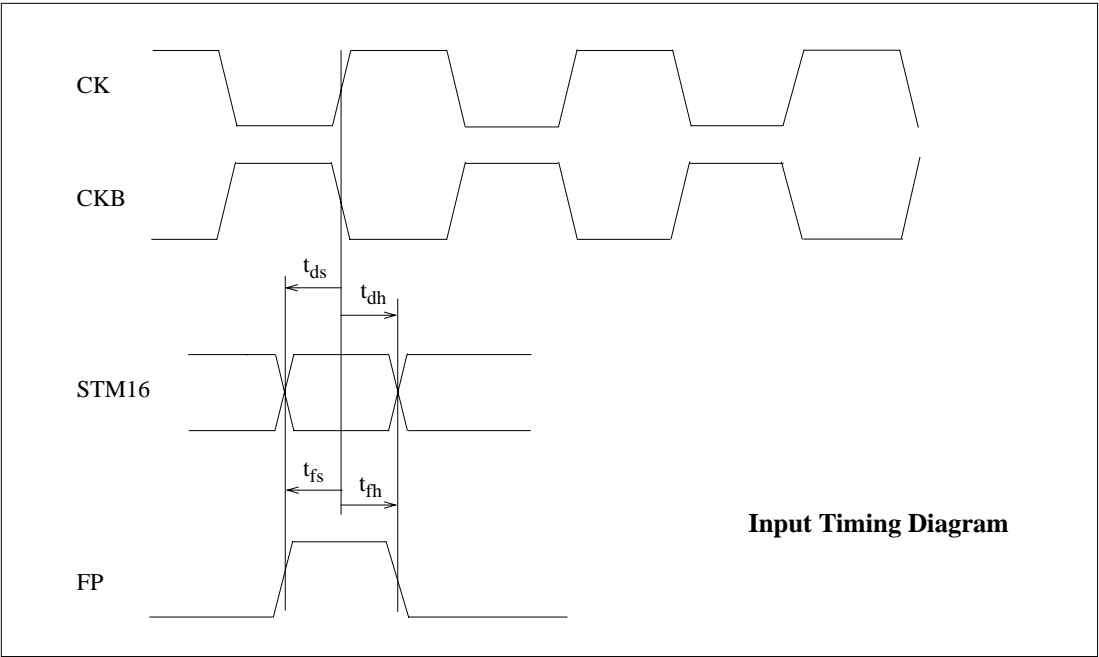
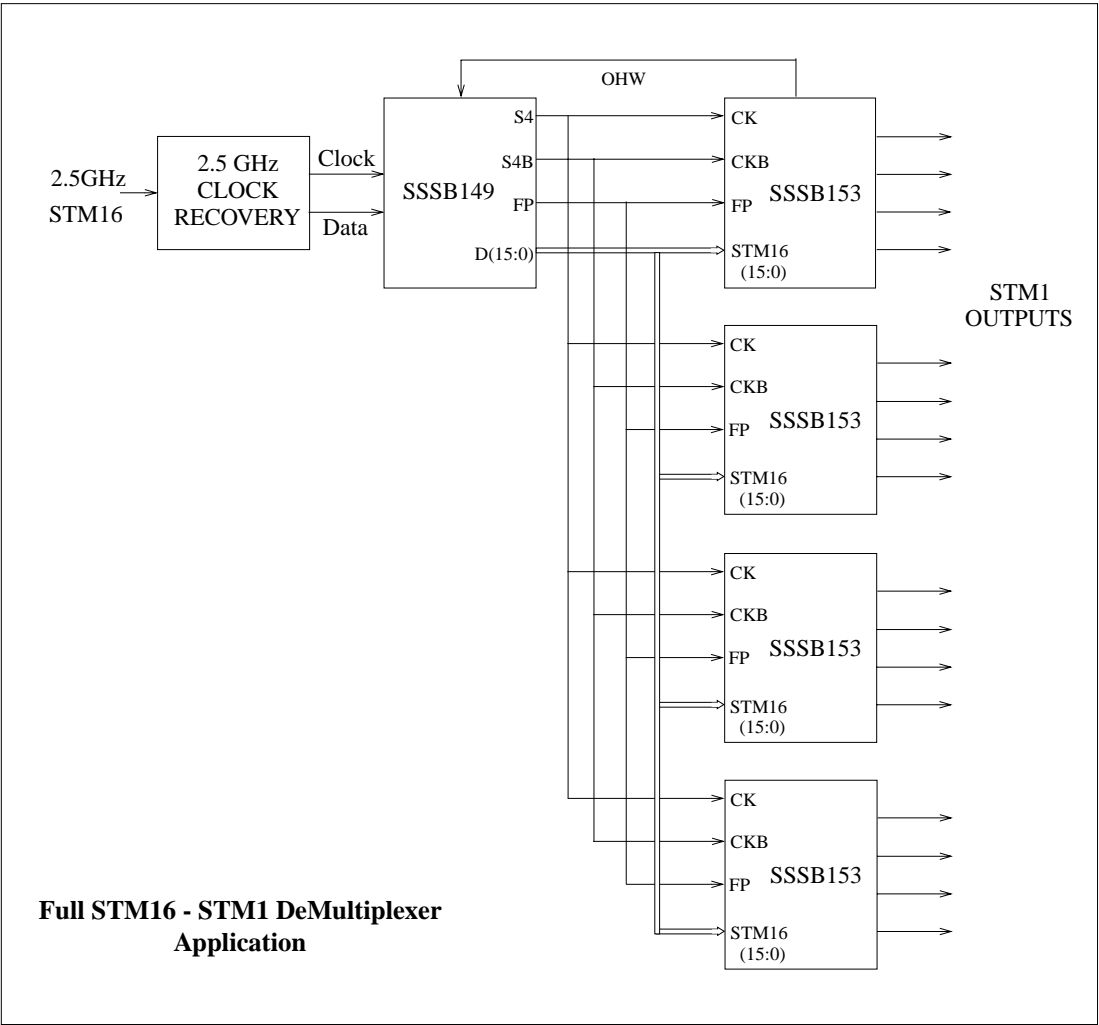
STM16 Interface

The SSSB153 accepts data as STM16 frames in 16 bit parallel form at a clock speed of 155MHz. The STM16 interface into the SSSB153 is designed to work with the Swindon Silicon Systems SSSB149 16 : 1 bit demultiplexer device. Data is clocked into the SSSB153 Input Register from the 155MHz differential clock inputs CK and CKB. Data is clocked in on the rising edge of CK, the falling edge of CKB.

The S4 and S4B outputs from the SSSB149 are suitable for driving the CK and CKB inputs of the SSSB153 respectively. Note that each SSSB149 can drive up to 4 SSSB153 devices.

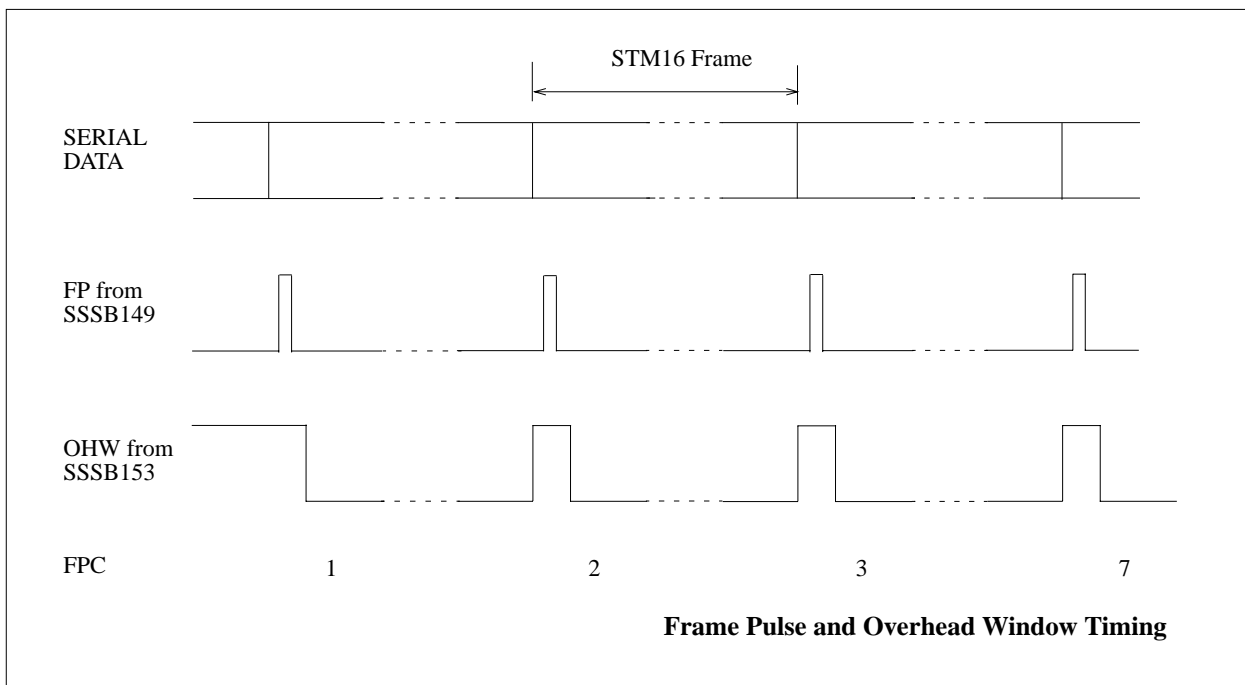


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Frame synchronisation

Frame synchronisation, i.e. the alignment of the parallel STM16 frame to the high speed serial input data stream, is achieved by the SSSB149. In ITU-T applications, the SSSB149 will synchronise onto the A1A2 word in the serial input data stream whenever the OHW signal is high. As the SSSB149 achieves synchronisation, it generates a frame pulse (FP) which is sent to each SSSB153. Upon receipt of the frame pulse, the SSSB153 drives the OHW signal low for almost one complete STM16 frame. This puts the SSSB149 into locked mode for most of the STM16 frame and prevents the SSSB149 from attempting to synchronise onto A1A2 words elsewhere in the STM16 frame. Note that in applications with multiple SSSB153 devices driven by a single SSSB149 device, only one SSSB153 OHW output is used to drive the SSSB149 OHW input.



The SSSB153 timing circuit includes a Frame Persistence Counter. The purpose of this counter is to determine whether the devices are correctly synchronised to the serial data stream at the SSSB149 input. The Frame Persistence Counter is a 3 bit counter, i.e. it stores count values of 0 to 7.

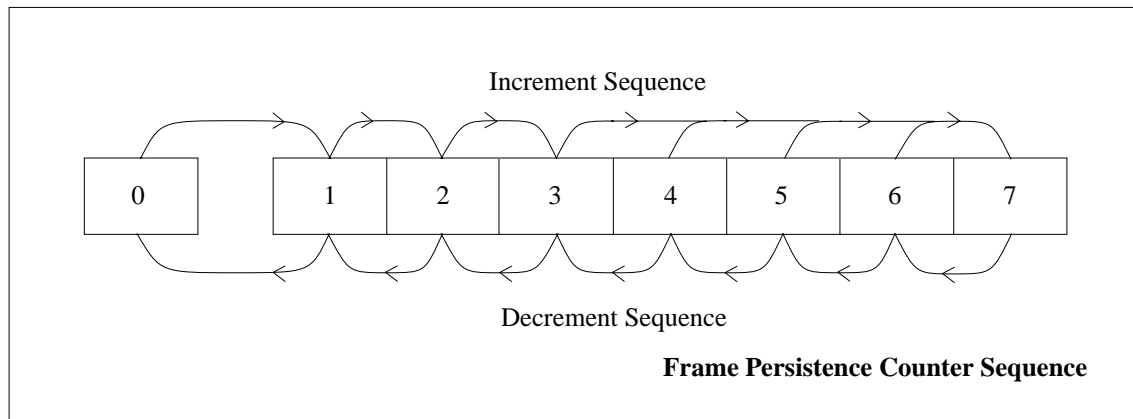
When the Frame Persistence Counter is at 0, the SSSB149 and SSSB153 devices are assumed to be not synchronised to the serial data stream. In this condition, the OverHead Window (OHW) signal is held continuously high. With OHW high, the SSSB149 will search its input serial data stream, and generate a frame pulse (FP) whenever a synchronisation pattern occurs in the data stream. When the SSSB153 receives a frame pulse, the Frame Persistence counter will increment to '1', the OHW output will be reset low, and the internal timing generator will be reset.

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When the Frame Persistence Counter value is between 1 and 7, the internal timing generator will generate a narrow high going pulse on the OHW output once every STM16 frame. (An STM16 frame length is 16x2430 bytes, or 19,440 cycles of the 155MHz clock, or 125µs.) If the devices are correctly synchronised, OHW will pulse high for eight cycles of the 155MHz clock, starting three cycles before the expected position of the A1A2 word in the serial data stream. This timing of the OHW pulse will allow the SSSB149 to recognise and lock on to the sync word. If the sync word is recognised during an OHW pulse, the SSSB149 sends further Frame Pulses back to the SSSB153.

Each frame pulse received by the SSSB153 during the OHW pulse will increment the Frame Persistence Counter in the sequence 0 - 1 - 2 - 3, then one more FP causes the counter to jump to 7. If a frame pulse is not received during the OHW pulse, the SSSB153 continues as if it were still synchronised, i.e. the OHW output is still pulsed high once per STM16 frame, but the Frame Persistence Counter decrements in the sequence 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0 (no jumps). When the counter reaches the value 0, a frame sync loss is recognised, and the OHW output is held continuously high, allowing the SSSB149 to resume the search for the sync word in the serial data stream.



If the Frame Persistence Counter value is between 1 and 7 but the devices are not correctly synchronised, either because the serial data stream or its timing was changed or corrupted, or because the SSSB149 generated a spurious frame pulse, then the OHW pulse will not be at the start of the incoming serial STM16 frame. The A1A2 sync word will occur only occasionally during these incorrectly timed OHW pulses, so few frame pulses will be generated and the Frame Persistence Counter will quickly decrement to zero, thus allowing the SSSB149 to resume the search until it captures the sync word at the start of the STM16 frame. In practice, the search will quickly move through the payload section of the STM16 frame, and home in on the correct position at the start of the STM16 frame.

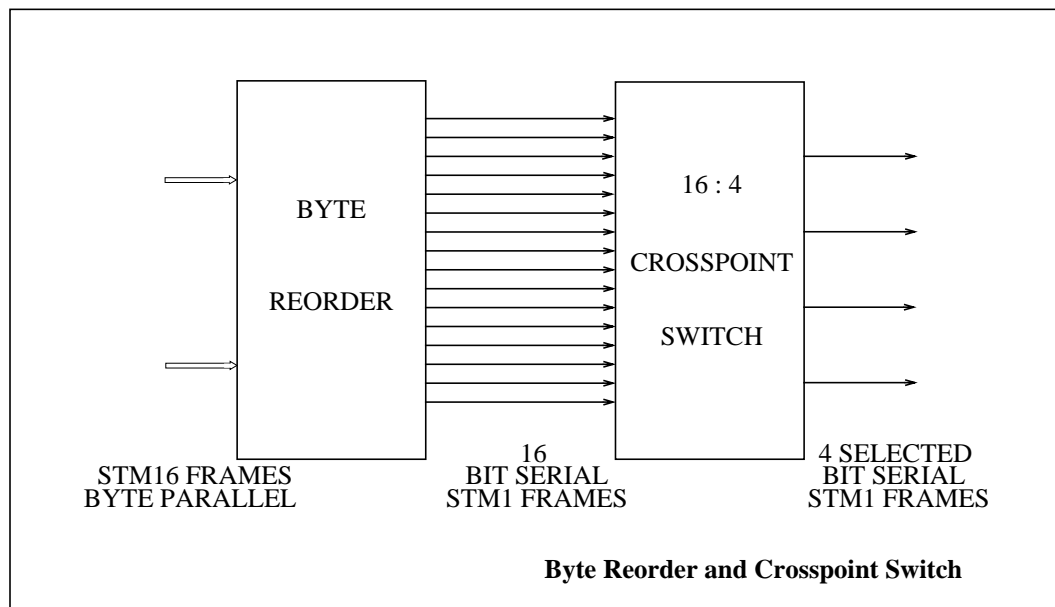
Descrambling and Parity Checking

The SSSB153 includes a descrambler circuit which operates on the STM16 parallel input frames. This circuit conforms to ITU-T Rec. G709, and operates on the whole STM16 frame except for the first 16 x 9 bytes of each frame. Descrambling is enabled when SCRIB is low.

The device includes error detection circuits which operate on the STM16 parallel input frames. These circuits conform to ITU-T Rec. G708 for Bit Interleaved Parity 8 (BIP-8) using even parity. Parity is calculated on the whole STM16 frame prior to descrambling, and is compared with the B1 byte in the Section OverHead (SOH) of the STM1 no1 of the following frame after descrambling. On detection of a single or multi bit parity error, the Parity Output (POUT) goes high, and the number of errors detected (0 to 8) is recorded in a parity error counter. This counter can be read and cleared through the 4 bit control interface as described later in this document. Reading the counter through the control interface resets POUT low. The parity error counter, and the POUT signal, are only valid from the SOH in the frame where the error was detected until either they are reset by a read operation on the parity error counter, or the SOH of the next frame. The parity check is enabled when the B1ENB input is held low. If B1ENB is held high, then POUT is forced low and the counter is inhibited.

Byte Reorder and Crosspoint Switch

The primary function of the SSSB153 is to receive STM16 frames in byte parallel form, and send out selected STM1 frames in bit serial form. This function is provided by the Byte Reorder and Crosspoint Switch circuits.



The Byte Reorder circuit converts the data from byte parallel form to bit serial form, i.e. the 16 outputs of the Byte Reorder circuit are the 16 STM1 frames in bit serial form.

The Crosspoint Switch circuit allows the 4 STM1 output channels to be selected from the 16 STM1 frames at the output of the Byte Reorder circuit. Each of the Crosspoint Switch data paths to the output channels can be any one of the 16 STM1 frames. The Crosspoint Switch is non-blocking, i.e. any of the 16 STM1 frames can be connected to single or multiple output channels. The selection of STM1 frames for each output channel is set by control registers which have read and write access through the control interface as described later in this document.

Serial Scrambling, Parity Generation, and CMI Code Conversion

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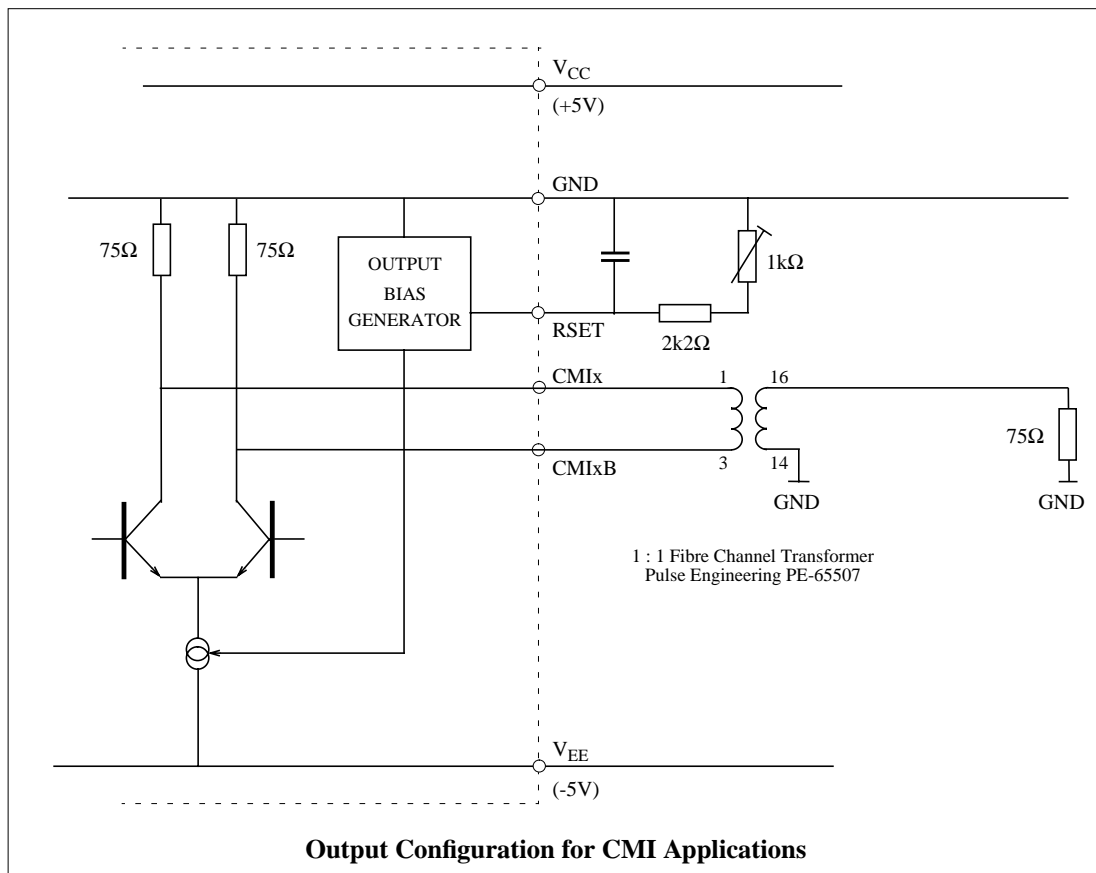
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The SSSB153 has 4 output channels. Each of the output channels can be any one of the 16 STM1 frames contained in the STM16 input frame. The 4 selected STM1 frames can be scrambled in accordance with ITU-T Rec. G.709. The scrambling for all 4 output channels is enabled if the SCROB input is held low.

The device will generate B1 parity for the 4 selected STM1 frames. This will be BIP-8 even parity, and will be calculated independently for each STM1 frame on the whole frame after scrambling. The result of the calculation is inserted in the SOH (row2, column1) of the following frame prior to scrambling.

The SSSB153 includes CMI (Coded Mark Invert) converters on each of the output channels. All converters are enabled if the CMIB input is held low. If CMIB is high, the serial outputs are 155MBit/s NRZ. If CMIB is low, the serial outputs are 311MBaud CMI. The CMI code is a 311MBaud rate code that has no DC content and can be used on AC coupled transmission systems. It conforms to the ITU-T Rec. G703 for transmission of 155MBit/s data. In order to meet the stringent clock mark-space ratio specified for CMI, it is recommended that the device clock inputs are driven differentially if CMI operation is required.

The SSSB153 CMI outputs are differential outputs with a 75Ω (+/- 30%) source impedance. Output low levels are defined by a $2.7k\Omega$ resistor (and a parallel $10nF$ decoupling capacitor) connected between the pin RSET and ground. This sets the level of all the data outputs. For CMI application, all CMI outputs, including unused outputs, must be externally terminated with the transformer coupled arrangement shown below, or with 75Ω to GND as defined in the Electrical Characteristics Table (this is to minimise crosstalk between output channels). For CMI applications, the RSET resistor can be a fixed plus variable resistor as shown below.



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Control Interface

The SSSB153 includes a 4 bit TTL compatible I/O bus. This is used for read and write access to the 4 registers which control the STM1 frame selection for the 4 output channels, and for read access to the parity error counter.

For a read instruction, the address of the register to be read is latched into the SSSB153 on the falling edge of ALE, the contents of the register can be read on the DATAIO bus when RDB is low. Reading the parity error counter resets the counter to zero and resets POUT. Reading the contents of the 4 output channel control registers has no other effect on the device operation.

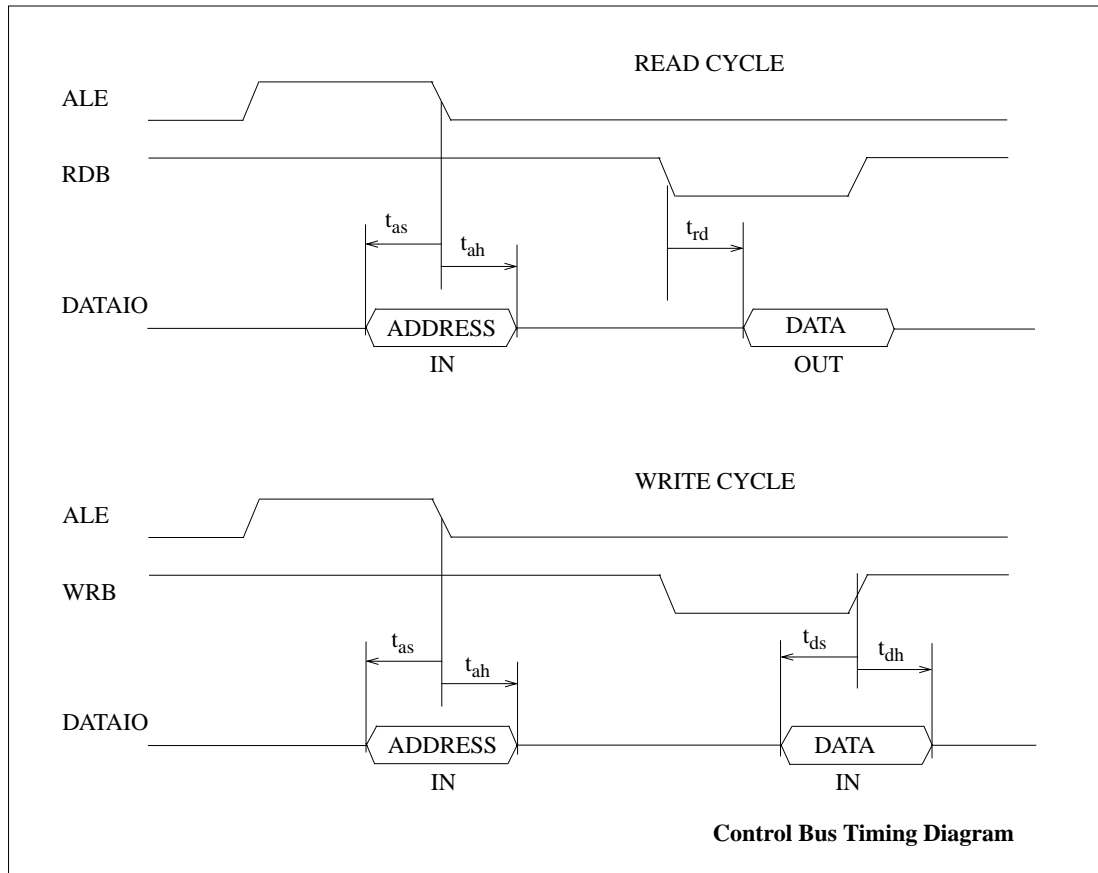
A write instruction is a two byte instruction. The address of the register to be written (i.e the selected output channel control register) is latched into the SSSB153 on the falling edge of ALE. The data for the register (i.e. the STM1 frame for that output channel) is written into the register when WRB is low.

DATAIO (3:0)		ADDRESS
Binary	Hex	
00xx	0-3	Invalid Address *1
0100	4	Control register for CMI1 Output
0101	5	Control register for CMI2 Output
0110	6	Control register for CMI3 Output
0111	7	Control register for CMI4 Output
10xx	8-B	Parity Error Counter
11xx	C-F	Invalid Address *1

*1 Undefined output on Read instruction, no operation on Write instruction

DATAIO (3:0)		DATA
Binary	Hex	(STM1 frame for selected output)
0000	0	STM No1
0001	1	STM No2
0010	2	STM No3
0011	3	STM No4
0100	4	STM No5
0101	5	STM No6
0110	6	STM No7
0111	7	STM No8
1000	8	STM No9
1001	9	STM No10
1010	A	STM No11
1011	B	STM No12
1100	C	STM No13
1101	D	STM No14
1110	E	STM No15
1111	F	STM No16

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Useful life may be impaired if the device is operated outside these limits

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	Gnd = 0V	-0.5		+6.0	V
Supply Voltage	V_{EE}	Gnd = 0V	-6.0		+0.5	V
Input Voltage (TTL)	V_{IT}		-0.5		V_{CC}	V
Input Voltage (ECL)	V_{IE}		V_{EE}		0.5	V
Output Current (TTL)	I_{OUT}				40	mA
Output Current (ECL)	I_{OUT}				40	mA
Junction Temperature	T_j				+150	°C
Storage Temperature	T_{stg}		-55		+150	°C

All pins are protected against ESD. However, the normal ESD precautions for high speed devices must be observed at all times

ELECTRICAL CHARACTERISTICS (Cont...)

OPERATING CONDITIONS

These operating conditions apply to all subsequent characteristics, unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Supply Voltage	V_{CC}		4.5		5.5	V
Operating Supply Voltage	V_{EE}		-5.5		-4.5	V
Ambient Temperature	T_a	No forced air cooling	0		70	° C

GENERAL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Dissipation	P_D	all outputs loaded		2500		mW
Supply Current	I_{EE}	$V_{EE} = -5.00V$		500		mA
Supply Current	I_{CC}	$V_{CC} = +5.00V$		20		mA

ECL OUTPUTS

OHV

(ECL100k outputs)

These characteristics apply when the relevant output is terminated by a 100Ω 1% resistor to -2V (V_{TT})

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Level	V_{OH}		-1.025		-0.88	V
Output Low Level	V_{OL}		-1.81		-1.62	V
Rise Time	t_r	20% - 80%		0.6	1.5	ns
Fall Time	t_f	20% - 80%		0.6	1.5	ns

ECL INPUTS

STM16(15:0) and FP

(ECL100k inputs with 50kΩ pulldown resistors)

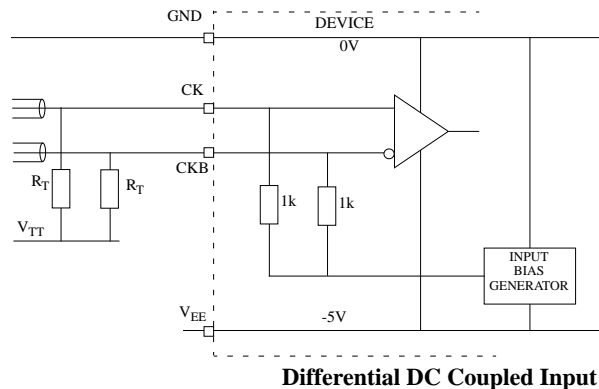
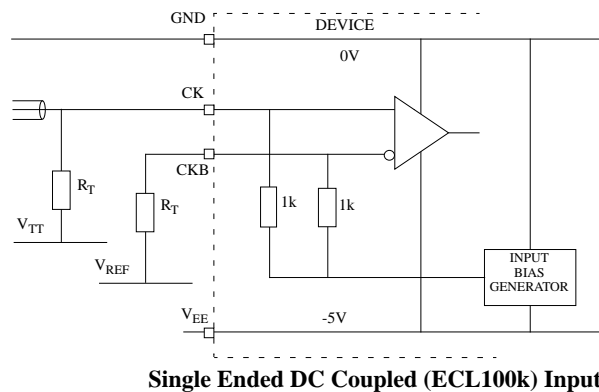
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Level	V_{IH}		-1.165		-0.88	V
Input Low Level	V_{IL}		-1.81		-1.475	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(Max)}$			150	μA
Input Low Current	I_{IL}	$V_{IN} = -2V$	25			μA
Data Setup Time	t_{ds}		2.5			ns
Data Hold Time	t_{dh}		1.0			ns
FP Setup Time	t_{fs}		2.5			ns
FP Hold Time	t_{fh}		1.0			ns

CLOCK INPUTS

CK, CKB, (Differential ECL compatible inputs)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Maximum Clock Rate	F_{MAX}	*1	160			MHz
Input Slew Rate	V_{slew}		0.25			V/ns
Clock Period	t_{per}		6.25			ns
Clock Rate		CMI mode	-20ppm	155.52	+20ppm	MHz
Clock M:S Ratio		CMI mode	49		51	%
Single Ended DC Coupled Inputs						
Input High Level	V_{IH}	$V_{REF} = -1.32V$	-1.165		-0.88	V
Input Low Level	V_{IL}	$V_{REF} = -1.32V$	-1.81		-1.475	V
Differential DC Coupled Inputs						
Input High Level	V_{IH}				-0.88	V
Input Low Level	V_{IL}		-1.81			V
Input Differential	V_{DIFF}		400		900	mV

*1 This device will operate down to zero frequency provided that the minimum input slew rate specification is met.



ELECTRICAL CHARACTERISTICS (Cont...)

CMI OUTPUTS

CMI(1:4)(B)

(Open Collector 75Ω outputs, externally loaded with 75Ω 1% to GND on all outputs)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Level	V _{OH}		-0.05			
Output Low Level	V _{OL}	RSET = 2.7kΩ	-1.15	-1.0	-0.9	V
P-P Output Swing	V _{PK}	*1	0.9	1.0	1.1	V
P-P Variation	V _{PKa}	*2			0.1	V
CMI output rise time	t _{rc}	10% - 90%			2	ns
CMI output fall time	t _{rc}	90% - 10%			2	ns
CMI edge skew	t _{e1}	*3			0.1	ns
CMI edge skew	t _{e2}	*4			0.35	ns

*1 V_{PK} is the guaranteed voltage swing on any one CMI output

*2 V_{PKa} is the variation in peak to peak swing between any two CMI outputs

*3 t_{e1} is the transition timing tolerance in CMI mode at the 50% point across all negative output edges

*4 t_{e2} is the transition timing tolerance in CMI mode at the 50% point across all positive output edges with respect to the negative edges

TTL INPUTS

ALE, RDB, WRB, DATAIO (3:0), SCRIB, SCROB, B1ENB and CMIB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Level	V _{IH}		2.0			V
Input Low Level	V _{IL}				0.8	V
Input High Current	I _{IH}				1.0	μA
Input Low Current	I _{IL}				1.0	μA
Address Setup Time	t _{as}		20			ns
Address Hold Time	t _{ah}		20			ns
Data Setup Time	t _{ds}		20			ns
Data Hold Time	t _{dh}		20			ns

TTL OUTPUTS

DATAIO (3:0) and POUT

(load = 15pF)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Level	V _{OH}	I _{OH} = -0.4 mA	2.4			V
Output Low Level	V _{OL}	I _{OL} = 4 mA			0.4	V
Rise Time	t _r	20% - 80%		6		ns
Fall Time	t _f	20% - 80%		6		ns
Output Delay	t _{rd}				15	ns

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PIN ASSIGNMENT TABLE

Pin No.	Name	Levels	Type	Description
1	STM16(1)	ECL100k	Input	Data Input
2	STM16(0)	ECL100k	Input	Data Input
3	GND			Ground
4	V _{EE}			Negative supply (-5V)
5	CKB	ECL100k	Input	Inverse 155MHz Clock Input
6	CK	ECL100k	Input	155MHz Clock Input
7	GND			Ground
8	RSET	Resistor	Input	Output level setting resistor
9	V _{EE}			Negative supply (-5V)
10	GND			Ground
11	CMI1B	75Ω	Output	STM1 Output
12	GND			Ground
13	CMI1	75Ω	Output	STM1 Output
14	V _{EE}			Negative supply (-5V)
15	CMI2	75Ω	Output	STM1 Output
16	GND			Ground
17	CMI2B	75Ω	Output	STM1 Output
18	GND			Ground
19	V _{EE}			Negative Supply (-5V)
20	CMI3B	75Ω	Output	STM1 Output
21	GND			Ground
22	CMI3	75Ω	Output	STM1 Output
23	V _{EE}			Negative supply (-5V)
24	CMI4	75Ω	Output	STM1 Output
25	GND			Ground
26	CMI4B	75Ω	Output	STM1 Output
27	GND			Ground
28	V _{EE}			Negative supply (-5V)
29	CMIB	TTL	Input	CMI Enable Input
30	SCROB	TTL	Input	Scrambling Enable Input
31	POUT	TTL	Output	Parity Detect Output
32	DATAIO(0)	TTL	I/O	Control Port Data Bus
33	DATAIO(1)	TTL	I/O	Control Port Data Bus
34	V _{EE}			Negative supply (-5V)
35	GND			Ground
36	DATAIO(2)	TTL	I/O	Control Port Data Bus
37	DATAIO(3)	TTL	I/O	Control Port Data Bus
38	GND			Ground
39	V _{CC}			Positive supply (+5V)
40	RDB	TTL	Input	Read Bus Input
41	ALE	TTL	Input	Address Latch Input
42	WRB	TTL	Input	Write Bus Input
43	V _{EE}			Negative supply (-5V)
44	GND			Ground
45	N/C			No Connection
46	SCRIB	TTL	Input	Descrambling Enable Input
47	B1ENB	TTL	Input	B1 Parity Check Enable Input
48	FP	ECL100k	Input	Frame Pulse Input
49	GND			Ground

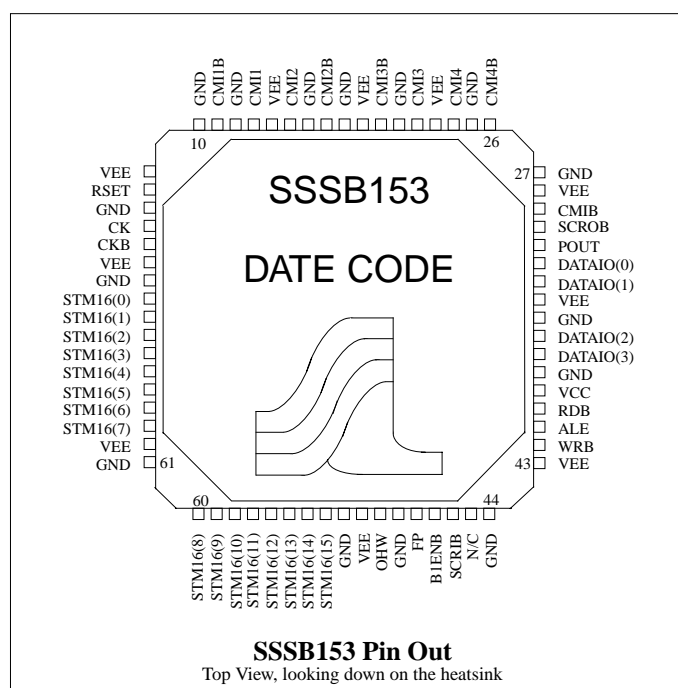
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PIN ASSIGNMENT TABLE (cont)

Pin No.	Name	Levels	Type	Description
50	OHW	ECL100k	Output	Overhead Window Output
51	V _{EE}			Negative Supply (-5V)
52	GND			Ground
53	STM16(15)	ECL100k	Input	Data Input
54	STM16(14)	ECL100k	Input	Data Input
55	STM16(13)	ECL100k	Input	Data Input
56	STM16(12)	ECL100k	Input	Data Input
57	STM16(11)	ECL100k	Input	Data Input
58	STM16(10)	ECL100k	Input	Data Input
59	STM16(9)	ECL100k	Input	Data Input
60	STM16(8)	ECL100k	Input	Data Input
61	GND			Ground
62	V _{EE}			Negative Supply (-5V)
63	STM16(7)	ECL100k	Input	Data Input
64	STM16(6)	ECL100k	Input	Data Input
65	STM16(5)	ECL100k	Input	Data Input
66	STM16(4)	ECL100k	Input	Data Input
67	STM16(3)	ECL100k	Input	Data Input
68	STM16(2)	ECL100k	Input	Data Input

To ensure correct operation :

- V_{EE} pins (4,9,14,19,23,28,34,43,51 and 62) and V_{CC} pin (39) must be decoupled to ground through high frequency ceramic capacitors close to the device pins
- All CMI outputs, including unused outputs, must be terminated with 75Ω to GND (this is to minimise crosstalk between output channels)
- All GND pins must be connected to a ground plane
- Some GND pins are not connected together on the device
- For correct operation, a 2.7kΩ resistor and parallel 10nf capacitor must be connected between the RSET pin and ground

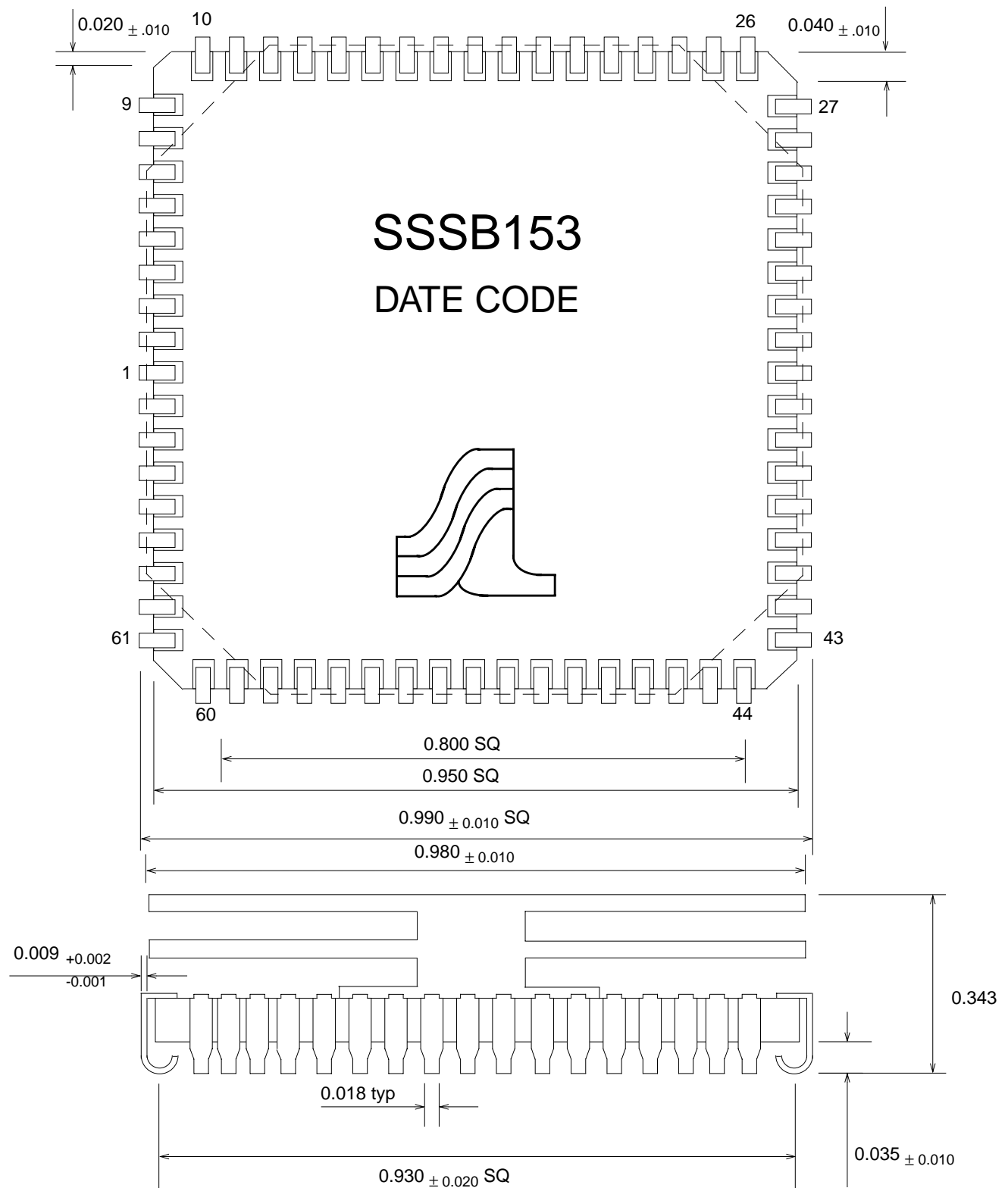


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PACKAGE DIMENSIONS

68 pin .050 inch pitch
J leaded ceramic chip carrier
Cavity up



- Leads are Kovar or Alloy 42
- All exposed metal is Gold plated, 60 micro inch minimum over Nickel plated, 100 micro inch minimum
- Lid is isolated from all leads

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