

# 1 Mbit / 2 Mbit / 4 Mbit (x8) Multi-Purpose Flash

SST39SF010A / SST39SF020A / SST39SF040



*Preliminary Specification*

## FEATURES:

- **Organized as 128K x8 / 256K x8 / 512K x8**
- **Single 5.0V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical)
  - Standby Current: 30  $\mu$ A (typical)
- **Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 45 and 70 ns
- **Latched Address and Data**
- **Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14  $\mu$ s (typical)
  - Chip Rewrite Time:
    - 2 seconds (typical) for SST39SF010A
    - 4 seconds (typical) for SST39SF020A
    - 8 seconds (typical) for SST39SF040
- **Automatic Write Timing**
  - Internal  $V_{PP}$  Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-pin PLCC
  - 32-pin TSOP (8mm x 14mm)
  - 32-pin PDIP

## PRODUCT DESCRIPTION

The SST39SF010A/020A/040 are CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A/020A/040 devices write (Program or Erase) with a 5.0V power supply. The SST39SF010A/020A/040 devices conform to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39SF010A/020A/040 devices provide a maximum Byte-Program time of 20  $\mu$ sec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF010A/020A/040 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during erase and program than alternative flash technologies. The total energy consumed is a

function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39SF010A/020A/040 are offered in 32-pin PLCC and 32-pin TSOP packages. A 600 mil, 32-pin PDIP is also available. See Figures 1, 2, and 3 for pinouts.

## Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE#



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

## Read

The Read operation of the SST39SF010A/020A/040 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram (Figure 4) for further details.

## Byte-Program Operation

The SST39SF010A/020A/040 are programmed on a byte-by-byte basis. Before programming, one must ensure that the sector, in which the byte which is being programmed exists, is fully erased. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20  $\mu$ s. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 15 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

## Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data#

Polling or Toggle Bit methods. See Figure 9 for timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

## Chip-Erase Operation

The SST39SF010A/020A/040 provide Chip-Erase operation, which allows the user to erase the entire memory array to the "1s" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 10 for timing diagram, and Figure 18 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

## Write Operation Status Detection

The SST39SF010A/020A/040 provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ<sub>7</sub>) and Toggle Bit (DQ<sub>6</sub>). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ<sub>7</sub> or DQ<sub>6</sub>. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

## Data# Polling (DQ<sub>7</sub>)

When the SST39SF010A/020A/040 are in the internal Program operation, any attempt to read DQ<sub>7</sub> will produce the complement of the true data. Once the Program operation is completed, DQ<sub>7</sub> will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ<sub>7</sub> will produce a '0'. Once the internal Erase operation is completed, DQ<sub>7</sub> will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sec-



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

## Preliminary Specification

tor- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 16 for a flowchart.

## Toggle Bit (DQ<sub>6</sub>)

During the internal Program or Erase operation, any consecutive attempts to read DQ<sub>6</sub> will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 16 for a flowchart.

## Data Protection

The SST39SF010A/020A/040 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

## Hardware Data Protection

**Noise/Glitch Protection:** A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

**V<sub>DD</sub> Power Up/Down Detection:** The Write operation is inhibited when V<sub>DD</sub> is less than 2.5V.

**Write Inhibit Mode:** Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

## Software Data Protection (SDP)

The SST39SF010A/020A/040 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST39SF010A/020A/040 devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T<sub>RC</sub>.

## Product Identification

The product identification mode identifies the device as the SST39SF040, SST39SF010A, or SST39SF020A and manufacturer as SST. This mode may be accessed by software operations. Users may wish to use the software product identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 17 for the ID entry command sequence flowchart.

**TABLE 1: PRODUCT IDENTIFICATION**

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39SF010A	0001H	B5H
SST39SF020A	0001H	B6H
SST39SF040	0001H	B7H

T1.2 398

## Product Identification Mode Exit/Reset

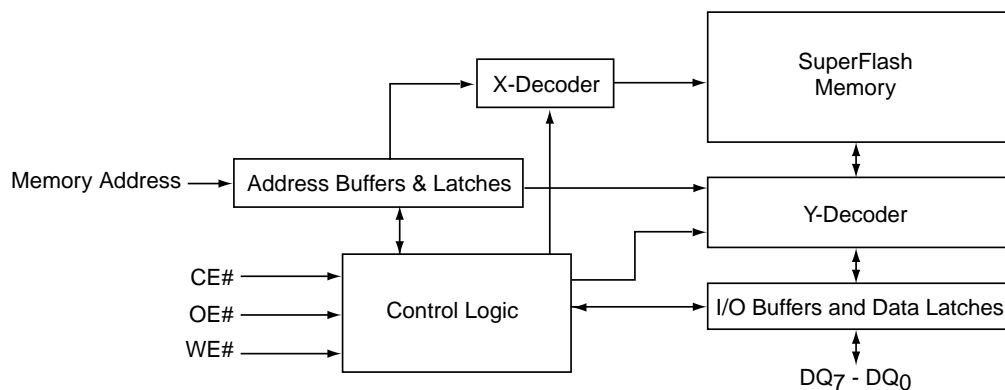
In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 17 for a flowchart.



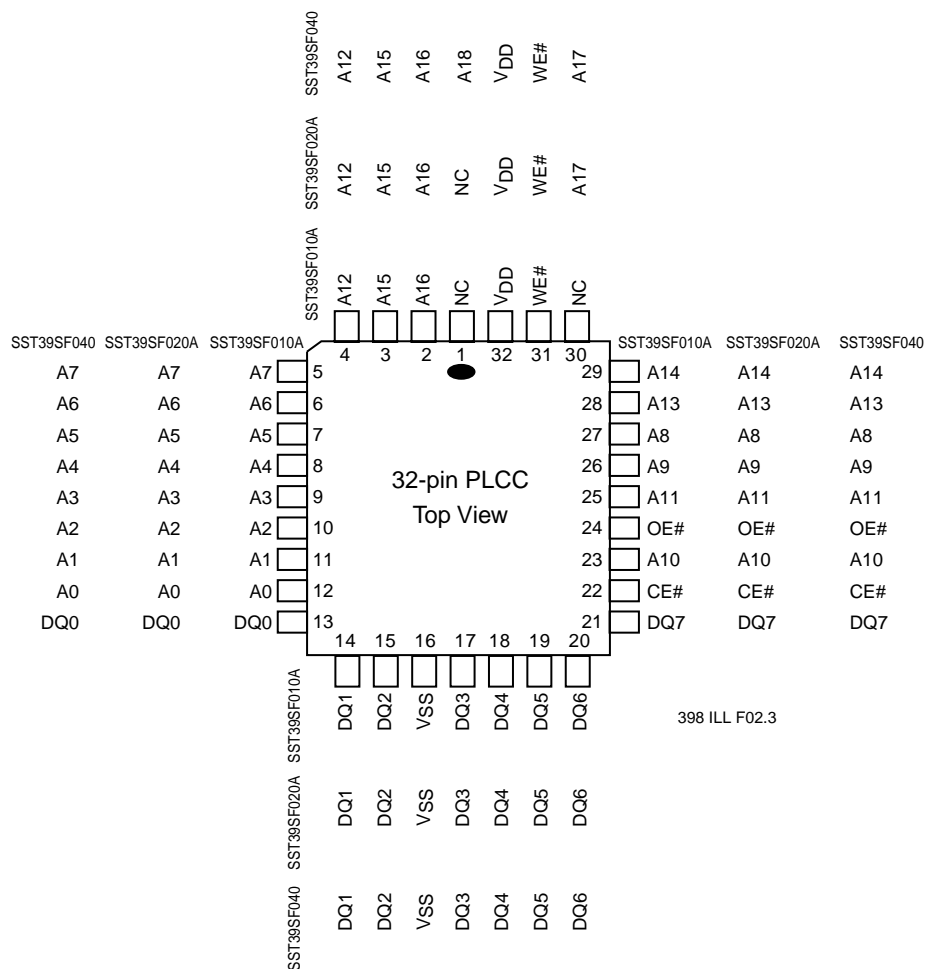
# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

## FUNCTIONAL BLOCK DIAGRAM



398 ILL B1.2



398 ILL F02.3

FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN PLCC



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

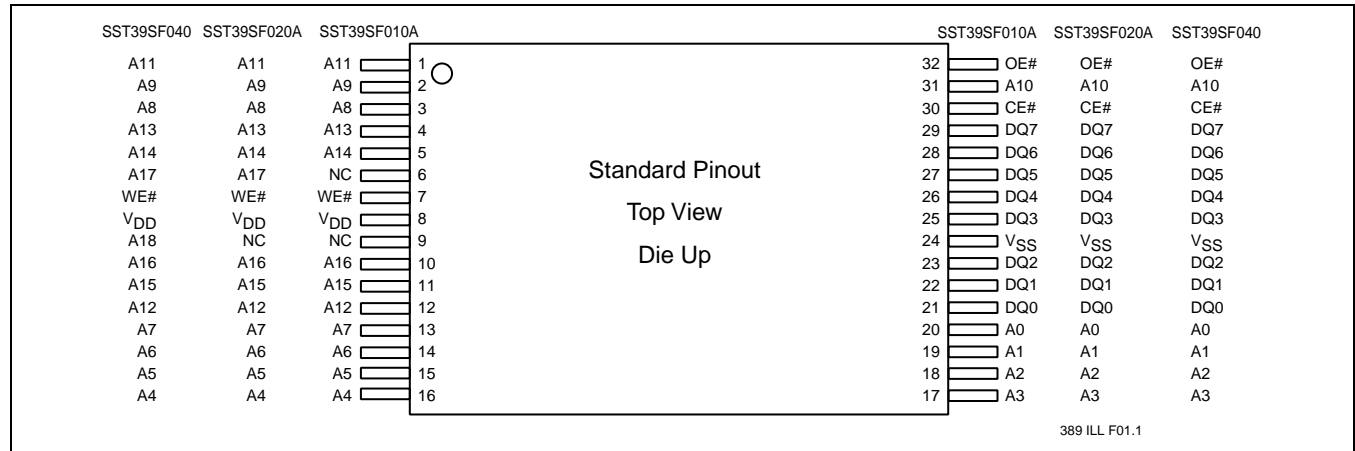


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN TSOP (8MM X 14MM)

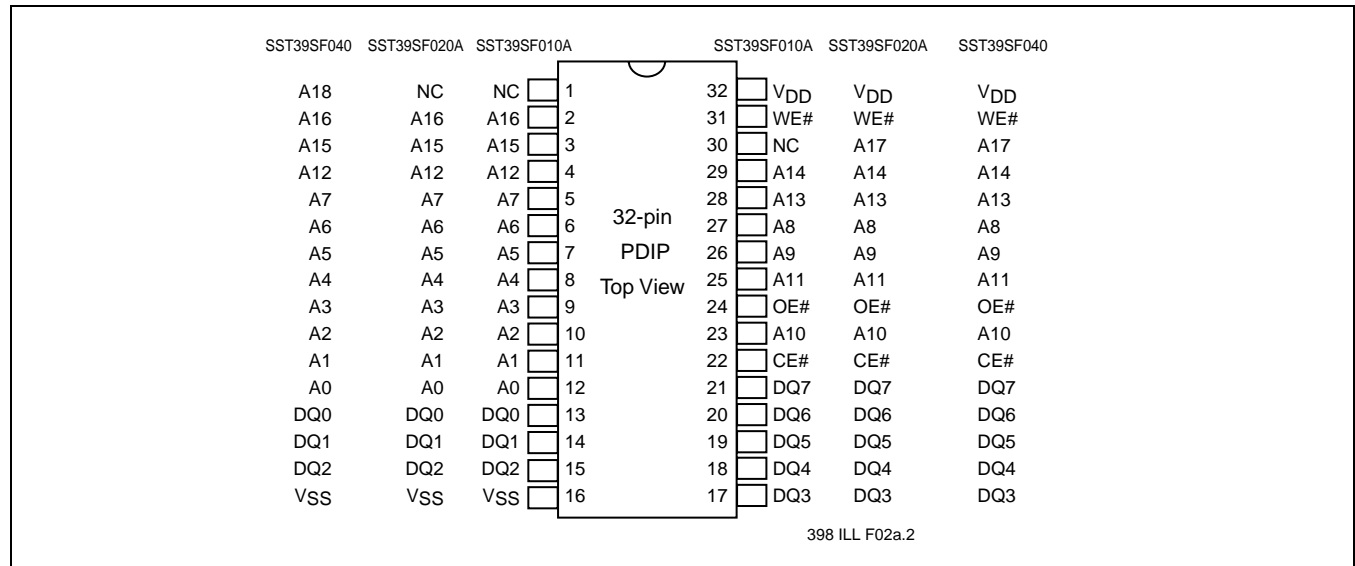


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

**TABLE 2: PIN DESCRIPTION**

Symbol	Pin Name	Functions
$A_{MS}^1-A_0$	Address Inputs	To provide memory addresses. During Sector-Erase $A_{MS}-A_{12}$ address lines will select the sector.
$DQ_7-DQ_0$	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when $OE\#$ or $CE\#$ is high.
$CE\#$	Chip Enable	To activate the device when $CE\#$ is low.
$OE\#$	Output Enable	To gate the data output buffers.
$WE\#$	Write Enable	To control the Write operations.
$V_{DD}$	Power Supply	To provide 5.0V supply ( $\pm 10\%$ )
$V_{SS}$	Ground	
NC	No Connection	Unconnected pins.

T2.1 398

1.  $A_{MS}$  = Most significant address  
 $A_{MS}$  =  $A_{16}$  for SST39SF010A,  $A_{17}$  for SST39SF020A, and  $A_{18}$  for SST39SF040

**TABLE 3: OPERATION MODES SELECTION**

Mode	$CE\#$	$OE\#$	$WE\#$	DQ	Address
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$	$A_{IN}$
Program	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN}$	$A_{IN}$
Erase	$V_{IL}$	$V_{IH}$	$V_{IL}$	$X^1$	Sector address, XXH for Chip-Erase
Standby	$V_{IH}$	X	X	High Z	X
Write Inhibit	X	$V_{IL}$	X	High Z/ $D_{OUT}$	X
	X	X	$V_{IH}$	High Z/ $D_{OUT}$	X
Product Identification					
Software Mode	$V_{IL}$	$V_{IL}$	$V_{IH}$		See Table 4

T3.3 398

1. X can be  $V_{IL}$  or  $V_{IH}$ , but no other value.



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash

## SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

**TABLE 4: SOFTWARE COMMAND SEQUENCE**

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA <sup>2</sup>	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA <sub>X</sub> <sup>3</sup>	30H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry <sup>4,5</sup>	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit <sup>6</sup>	XXH	F0H										
Software ID Exit <sup>6</sup>	5555H	AAH	2AAAH	55H	5555H	F0H						

T4.2 398

1. Address format A<sub>14</sub>-A<sub>0</sub> (Hex), Addresses A<sub>15</sub> - A<sub>MS</sub> can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value, for the Command sequence.
2. BA = Program Byte address
3. SA<sub>X</sub> for Sector-Erase; uses A<sub>MS</sub>-A<sub>12</sub> address lines  
A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>16</sub> for SST39SF010A, A<sub>17</sub> for SST39SF020A, and A<sub>18</sub> for SST39SF040
4. The device does not remain in Software Product ID Mode if powered down.
5. With A<sub>MS</sub>-A<sub>1</sub> = 0; SST Manufacturer's ID = BFH, is read with A<sub>0</sub> = 0,  
SST39SF010A Device ID = B5H, is read with A<sub>0</sub> = 1  
SST39SF020A Device ID = B6H, is read with A<sub>0</sub> = 1  
SST39SF040 Device ID = B7H, is read with A<sub>0</sub> = 1
6. Both Software ID Exit operations are equivalent

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to V <sub>DD</sub> + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-1.0V to V <sub>DD</sub> + 1.0V
Voltage on A <sub>9</sub> Pin to Ground Potential	-0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Through Hold Lead Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current <sup>1</sup>	100 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

### OPERATING RANGE

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0°C to +70°C	5.0V±10%
Industrial	-40°C to +85°C	5.0V±10%

### AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C <sub>L</sub> = 30 pF for 45 ns
Output Load	C <sub>L</sub> = 100 pF for 70 ns
See Figures 13 and 14	



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

**TABLE 5: DC OPERATING CHARACTERISTICS  $V_{DD} = 5.0V \pm 10\%$**

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
$I_{DD}$	Power Supply Current				Address input= $V_{IL}/V_{IH}$ , at $f=1/T_{RC}$ Min $V_{DD}=V_{DD}$ Max
	Read		25	mA	$CE\#=OE\#=V_{IL}$ , $WE\#=V_{IH}$ , all I/Os open
	Write		25	mA	$CE\#=WE\#=V_{IL}$ , $OE\#=V_{IH}$
$I_{SB1}$	Standby $V_{DD}$ Current (TTL input)		3	mA	$CE\#=V_{IH}$ , $V_{DD}=V_{DD}$ Max
$I_{SB2}$	Standby $V_{DD}$ Current (CMOS input)		100	$\mu A$	$CE\#=V_{IHC}$ , $V_{DD}=V_{DD}$ Max
$I_{LI}$	Input Leakage Current		1	$\mu A$	$V_{IN}=GND$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT}=GND$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max
$V_{IL}$	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
$V_{IH}$	Input High Voltage	2.0		V	$V_{DD}=V_{DD}$ Max
$V_{IHC}$	Input High Voltage (CMOS)	$V_{DD}-0.3$		V	$V_{DD}=V_{DD}$ Max
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL}=2.1$ mA, $V_{DD}=V_{DD}$ Min
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH}=-400$ $\mu A$ , $V_{DD}=V_{DD}$ Min

T5.4 398

**TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS**

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	Power-up to Read Operation	100	$\mu s$
$T_{PU-WRITE}^1$	Power-up to Program/Erase Operation	100	$\mu s$

T6.1 398

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 7: CAPACITANCE ( $T_a = 25^\circ C$ ,  $f=1$  Mhz, other pins open)**

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
$C_{IN}^1$	Input Capacitance	$V_{IN} = 0V$	6 pF

T7.0 398

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Minimum Specification	Units	Test Method
$N_{END}^1$	Endurance	10,000	Cycles	JEDEC Standard A117
$T_{DR}^1$	Data Retention	100	Years	JEDEC Standard A103
$I_{LTH}^1$	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

T8.1 398

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.





# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

## AC CHARACTERISTICS

**TABLE 9: READ CYCLE TIMING PARAMETERS  $V_{DD} = 5.0V \pm 10\%$**

Symbol	Parameter	SST39SF010A/020A/040-45		SST39SF010A/020A/040-70		Units
		Min	Max	Min	Max	
$T_{RC}$	Read Cycle Time	45		70		ns
$T_{CE}$	Chip Enable Access Time		45		70	ns
$T_{AA}$	Address Access Time		45		70	ns
$T_{OE}$	Output Enable Access Time		25		35	ns
$T_{CLZ}^1$	CE# Low to Active Output	0		0		ns
$T_{OLZ}^1$	OE# Low to Active Output	0		0		ns
$T_{CHZ}^1$	CE# High to High-Z Output		15		25	ns
$T_{OHZ}^1$	OE# High to High-Z Output		15		25	ns
$T_{OH}^1$	Output Hold from Address Change	0		0		ns

T9.3 398

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS**

Symbol	Parameter	Min	Max	Units
$T_{BP}$	Byte-Program Time		20	$\mu s$
$T_{AS}$	Address Setup Time	0		ns
$T_{AH}$	Address Hold Time	30		ns
$T_{CS}$	WE# and CE# Setup Time	0		ns
$T_{CH}$	WE# and CE# Hold Time	0		ns
$T_{OES}$	OE# High Setup Time	0		ns
$T_{OEH}$	OE# High Hold Time	10		ns
$T_{CP}$	CE# Pulse Width	40		ns
$T_{WP}$	WE# Pulse Width	40		ns
$T_{WPH}^1$	WE# Pulse Width High	30		ns
$T_{CPH}^1$	CE# Pulse Width High	30		ns
$T_{DS}$	Data Setup Time	40		ns
$T_{DH}^1$	Data Hold Time	0		ns
$T_{IDA}^1$	Software ID Access and Exit Time		150	ns
$T_{SE}$	Sector-Erase		25	ms
$T_{SCE}$	Chip-Erase		100	ms

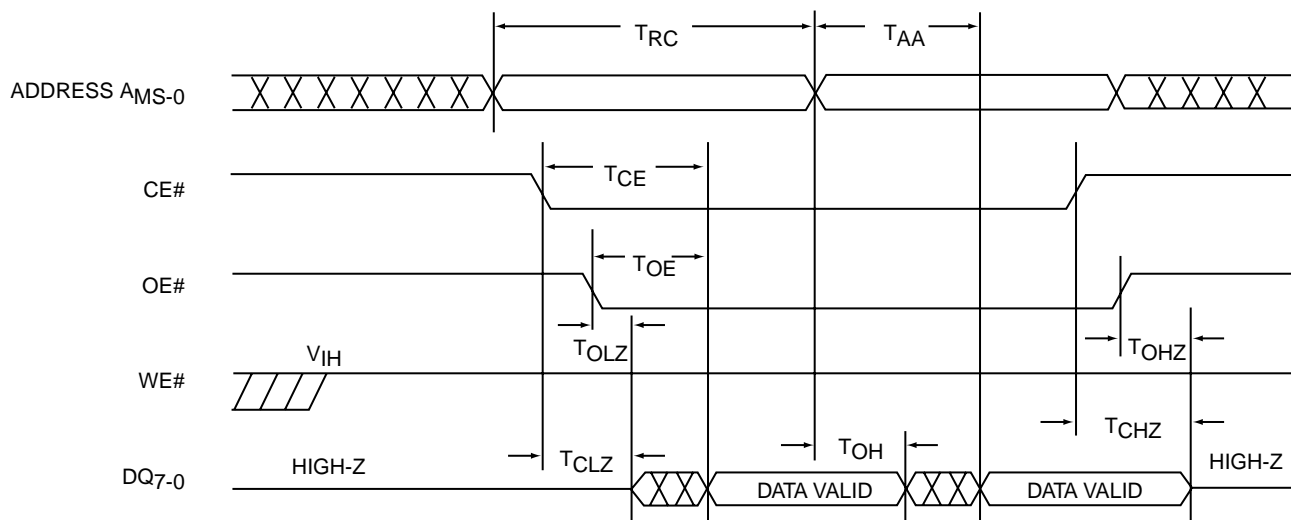
T10.1 398

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

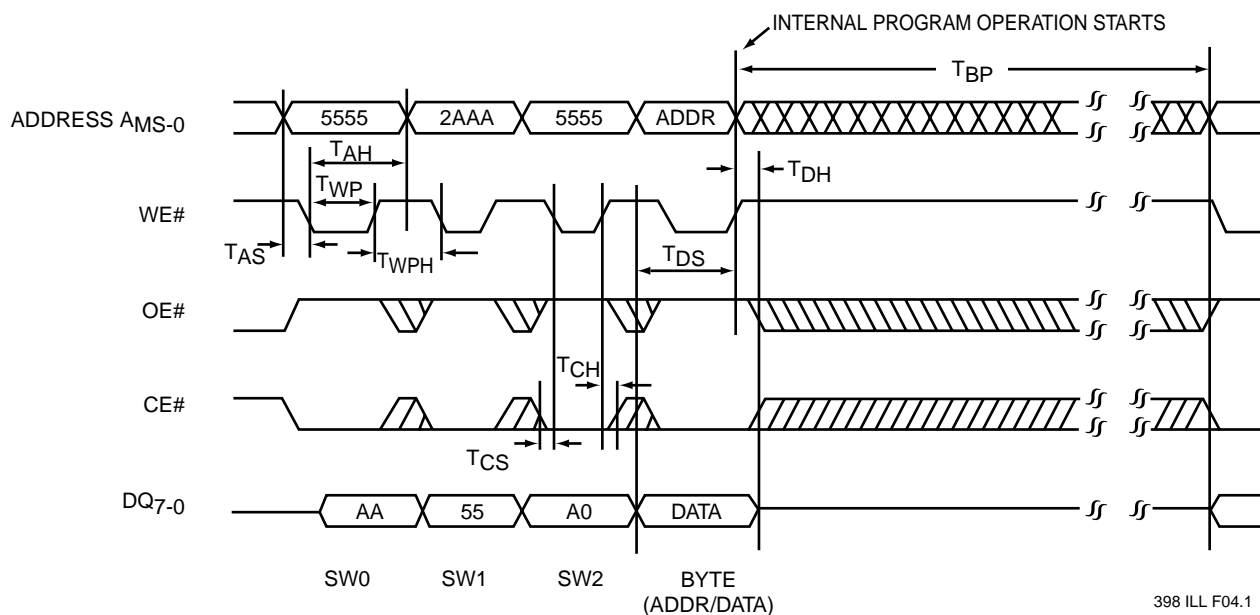
Preliminary Specification



Note: A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>16</sub> for SST39SF010A, A<sub>17</sub> for SST39SF020A, and A<sub>18</sub> for SST39SF040

398 ILL F03.1

**FIGURE 4: READ CYCLE TIMING DIAGRAM**



Note: A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>16</sub> for SST39SF010A, A<sub>17</sub> for SST39SF020A, and A<sub>18</sub> for SST39SF040

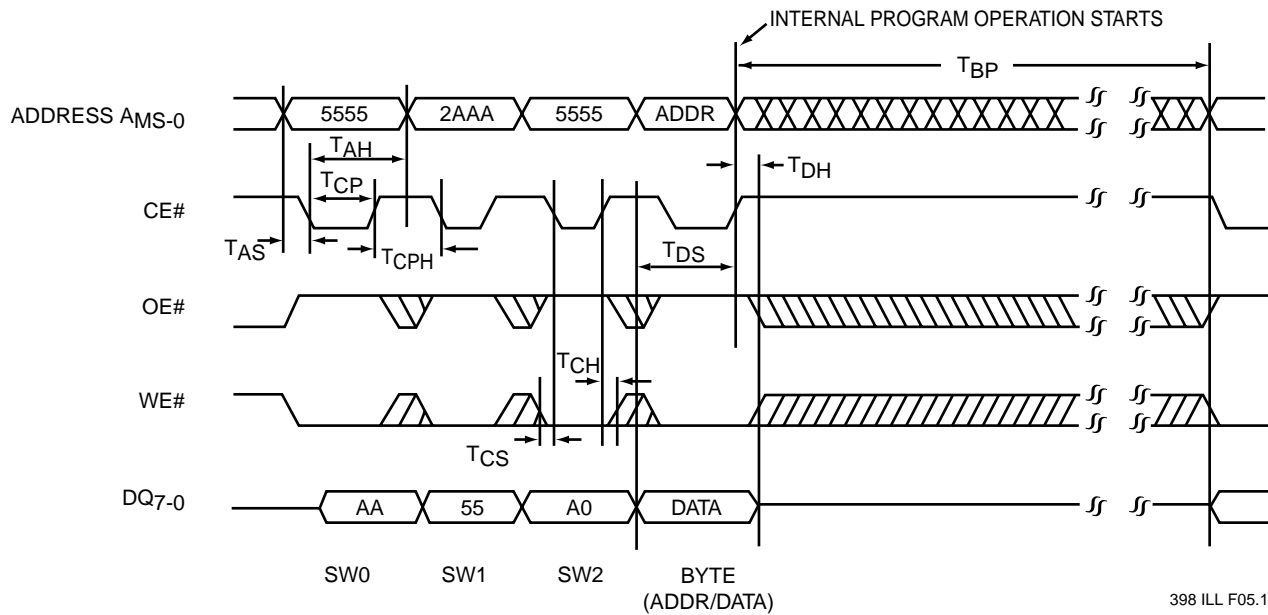
398 ILL F04.1

**FIGURE 5: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM**



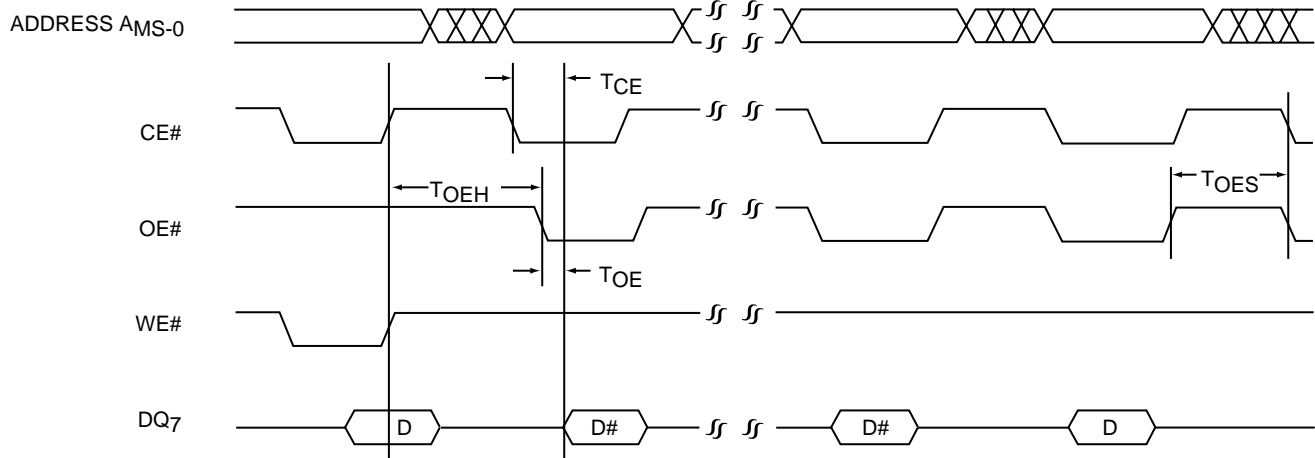
# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification



Note:  $A_{MS}$  = Most significant address  
 $A_{MS}$  =  $A_{16}$  for SST39SF010A,  $A_{17}$  for SST39SF020A, and  $A_{18}$  for SST39SF040

**FIGURE 6: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM**



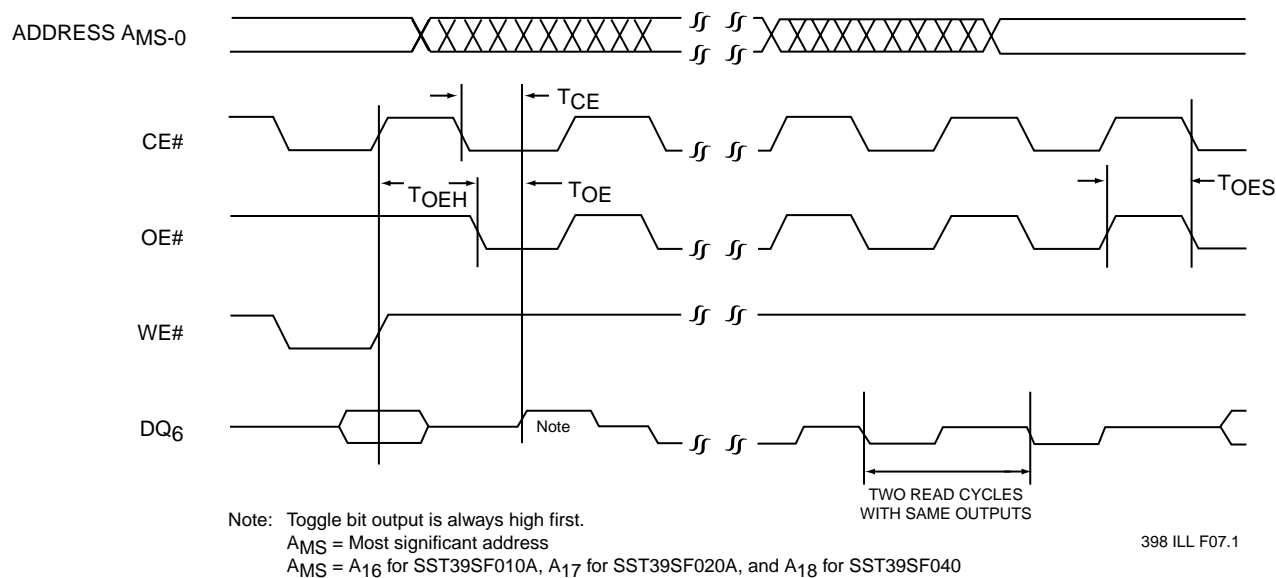
Note:  $A_{MS}$  = Most significant address  
 $A_{MS}$  =  $A_{16}$  for SST39SF010A,  $A_{17}$  for SST39SF020A, and  $A_{18}$  for SST39SF040

**FIGURE 7: DATA# POLLING TIMING DIAGRAM**

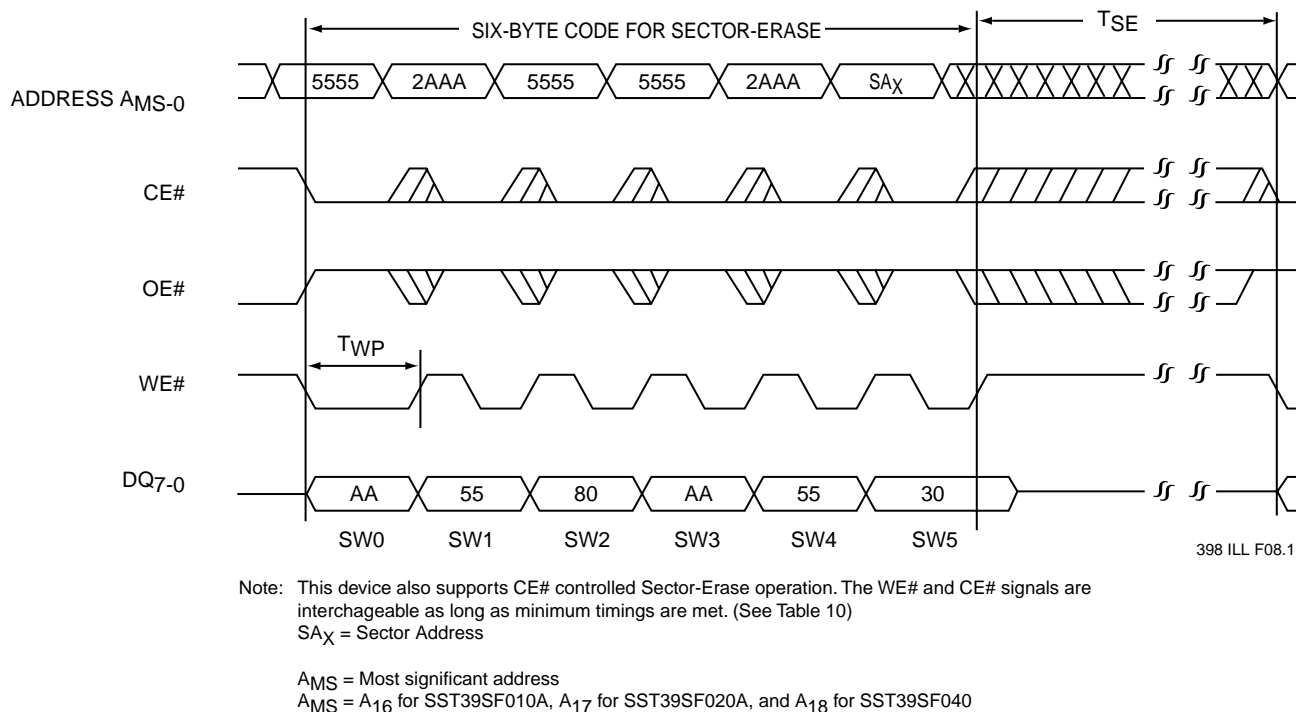


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Preliminary Specification



**FIGURE 8: TOGGLE BIT TIMING DIAGRAM**

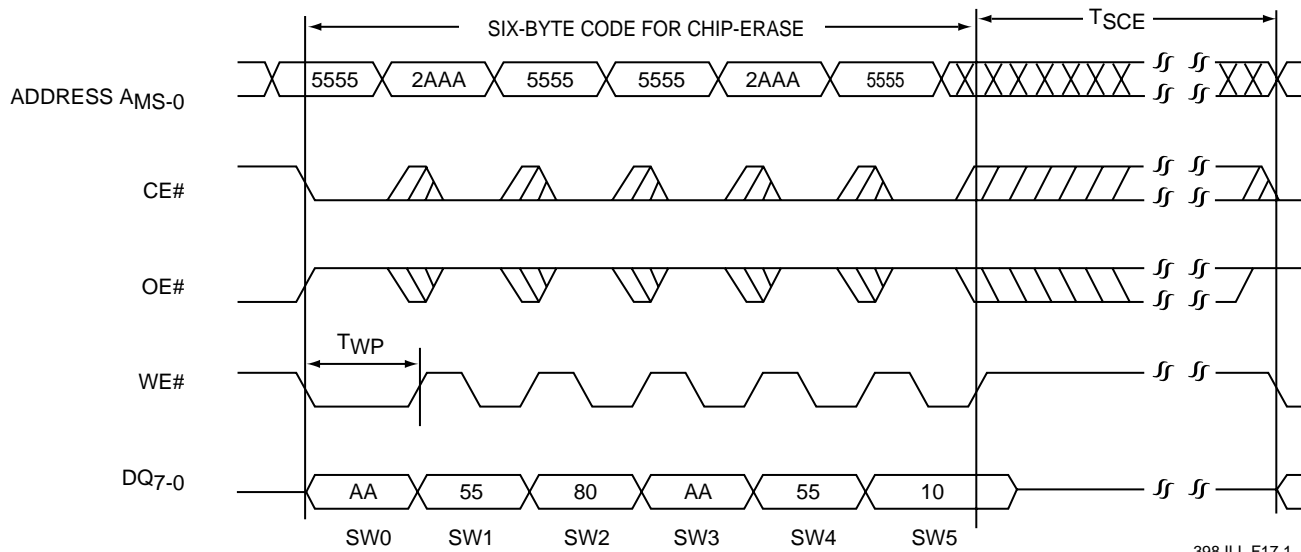


**FIGURE 9: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM**



# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

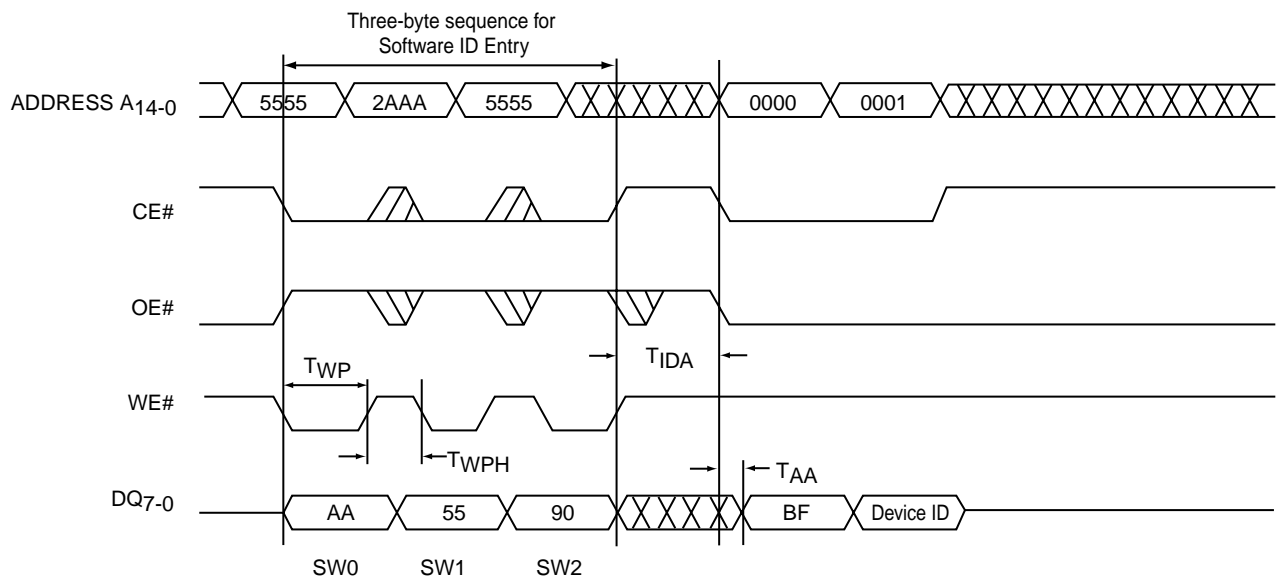


Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)  
SA<sub>X</sub> = Sector Address

AMS = Most significant address

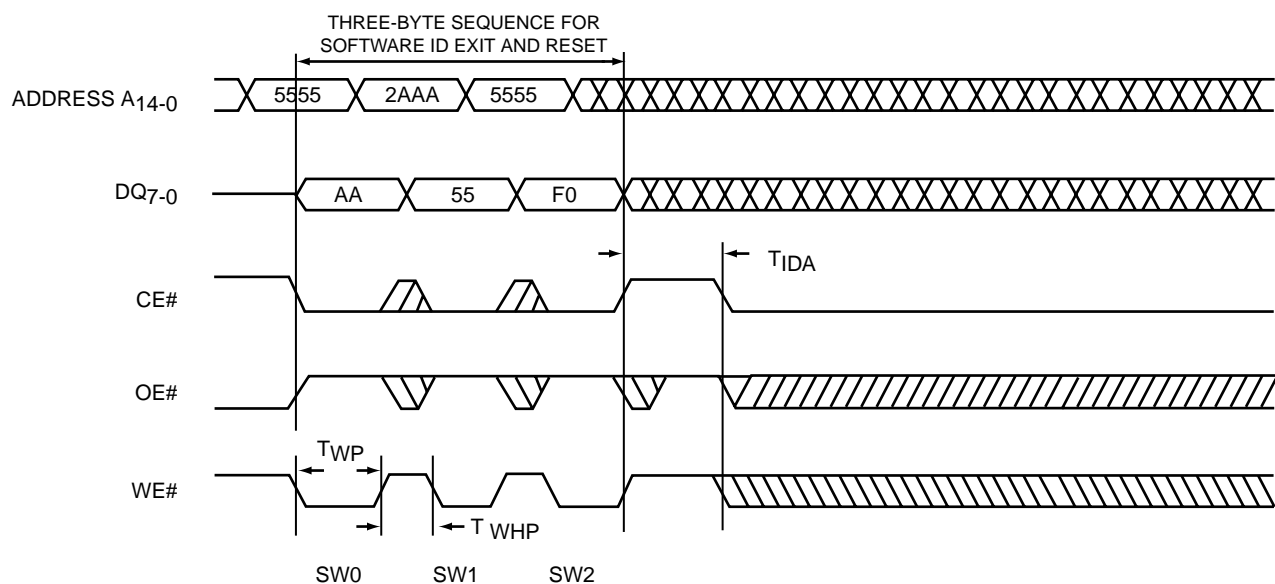
AMS = A<sub>16</sub> for SST39SF010A, A<sub>17</sub> for SST39SF020A, and A<sub>18</sub> for SST39SF040

**FIGURE 10: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM**



Device ID = B5H for SST39SF010A, B6H for SST39SF020A, and B7H for SST39SF040

**FIGURE 11: SOFTWARE ID ENTRY AND READ**



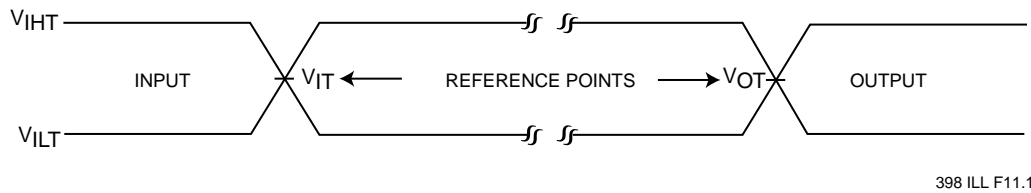
398 ILL F10.0

FIGURE 12: SOFTWARE ID EXIT AND RESET



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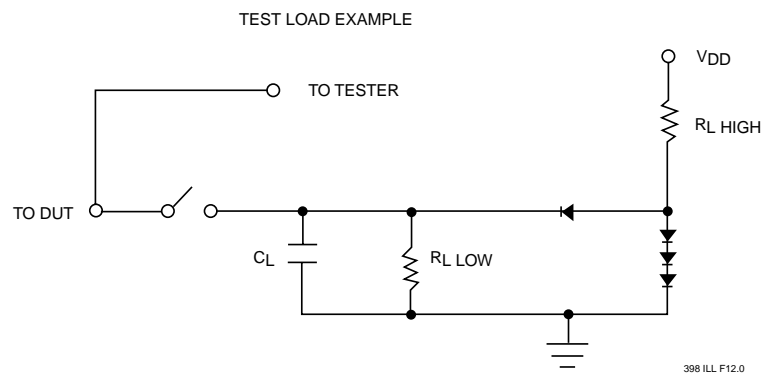
Preliminary Specification



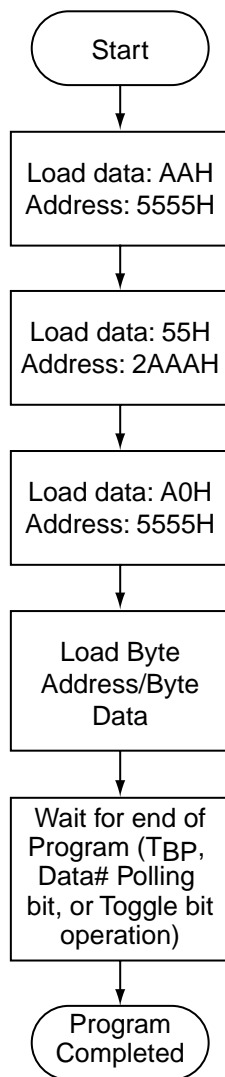
AC test inputs are driven at  $V_{IHT}$  (3.0V) for a logic "1" and  $V_{ILT}$  (0V) for a logic "0". Measurement reference points for inputs and outputs are  $V_{IT}$  (1.5V) and  $V_{OT}$  (1.5V). Input rise and fall times (10%  $\leftrightarrow$  90%) are  $<5$  ns.

**Note:**  $V_{IT}$  -  $V_{INPUT}$  Test  
 $V_{OT}$  -  $V_{OUTPUT}$  Test  
 $V_{IHT}$  -  $V_{INPUT}$  HIGH Test  
 $V_{ILT}$  -  $V_{INPUT}$  LOW Test

**FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS**



**FIGURE 14: A TEST LOAD EXAMPLE**



398 ILL F13.1

FIGURE 15: BYTE-PROGRAM ALGORITHM





# 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

Preliminary Specification

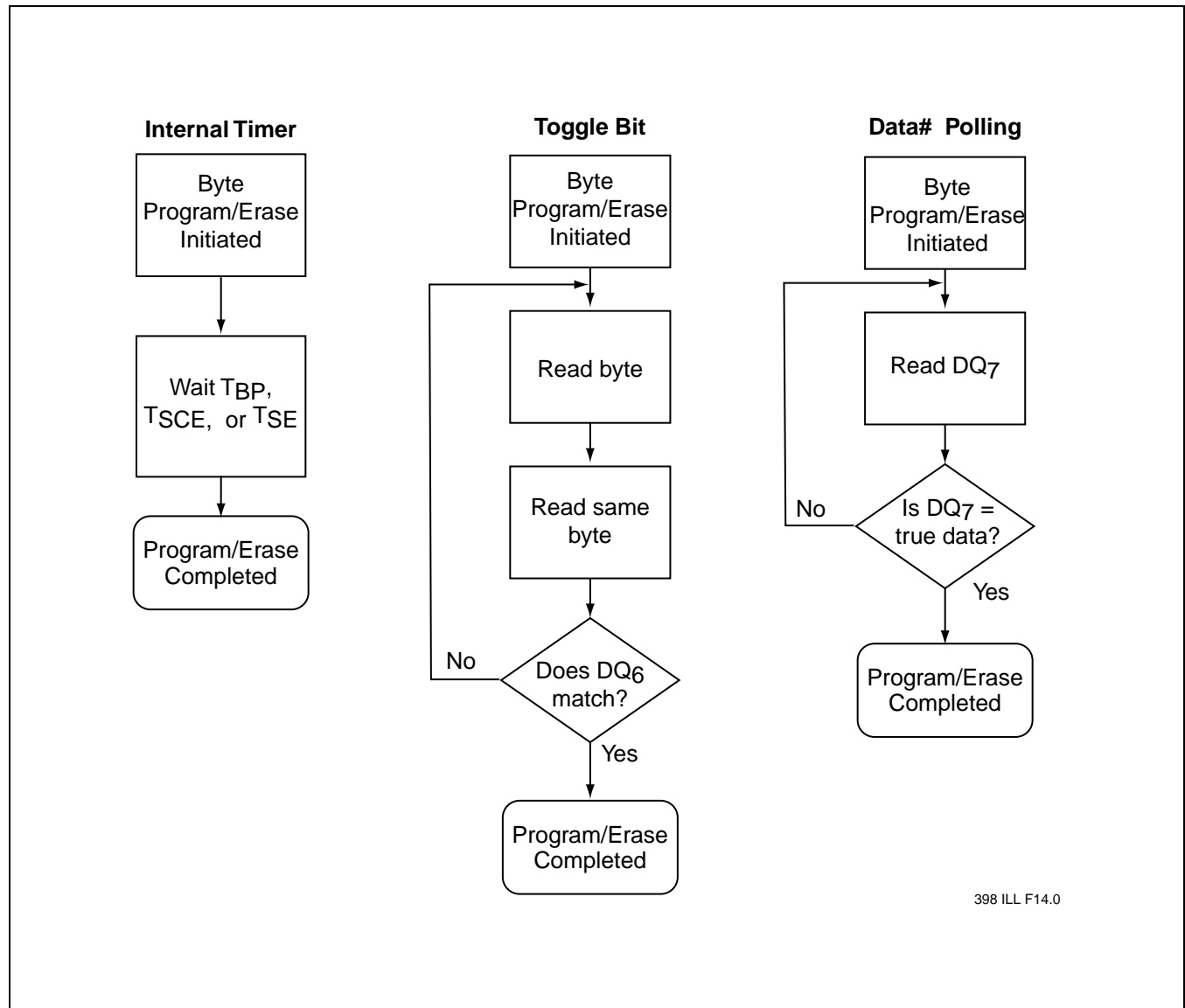
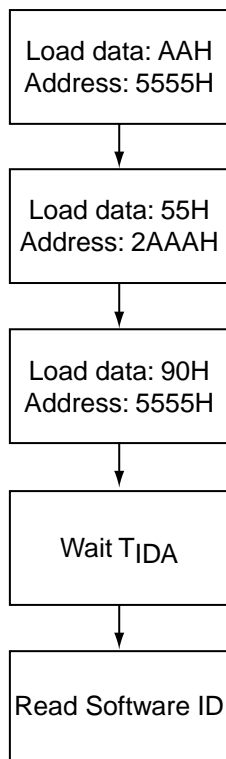


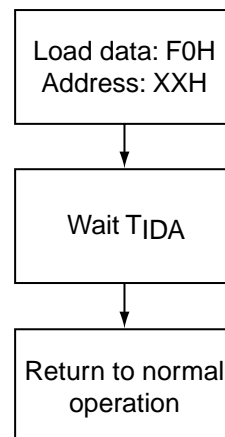
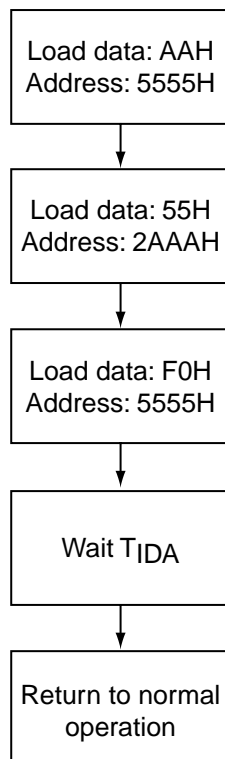
FIGURE 16: WAIT OPTIONS



**Software Product ID Entry  
Command Sequence**



**Software Product ID Exit &  
Reset Command Sequence**



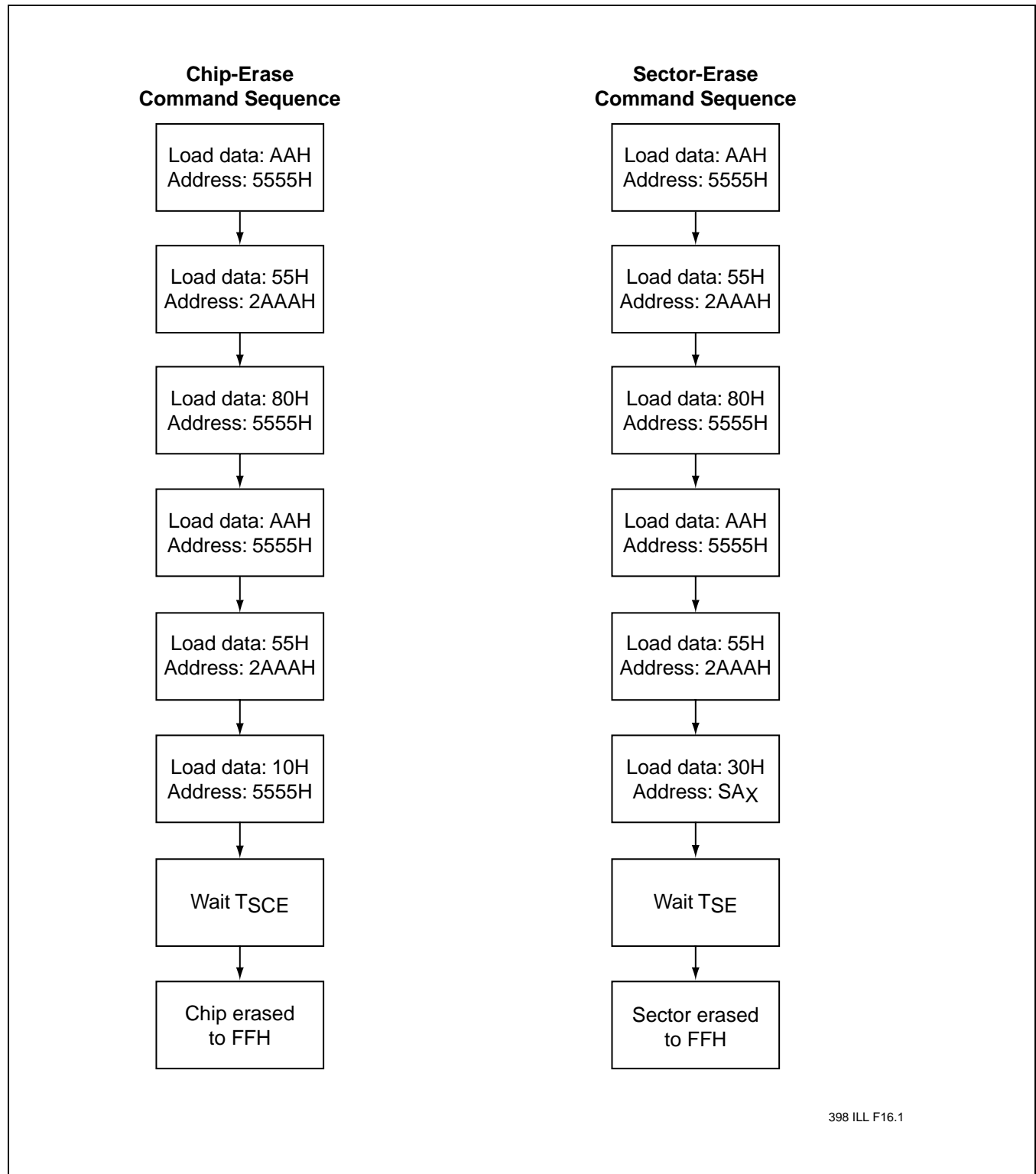
398 ILL F15.1

**FIGURE 17: SOFTWARE PRODUCT COMMAND FLOWCHARTS**



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Preliminary Specification

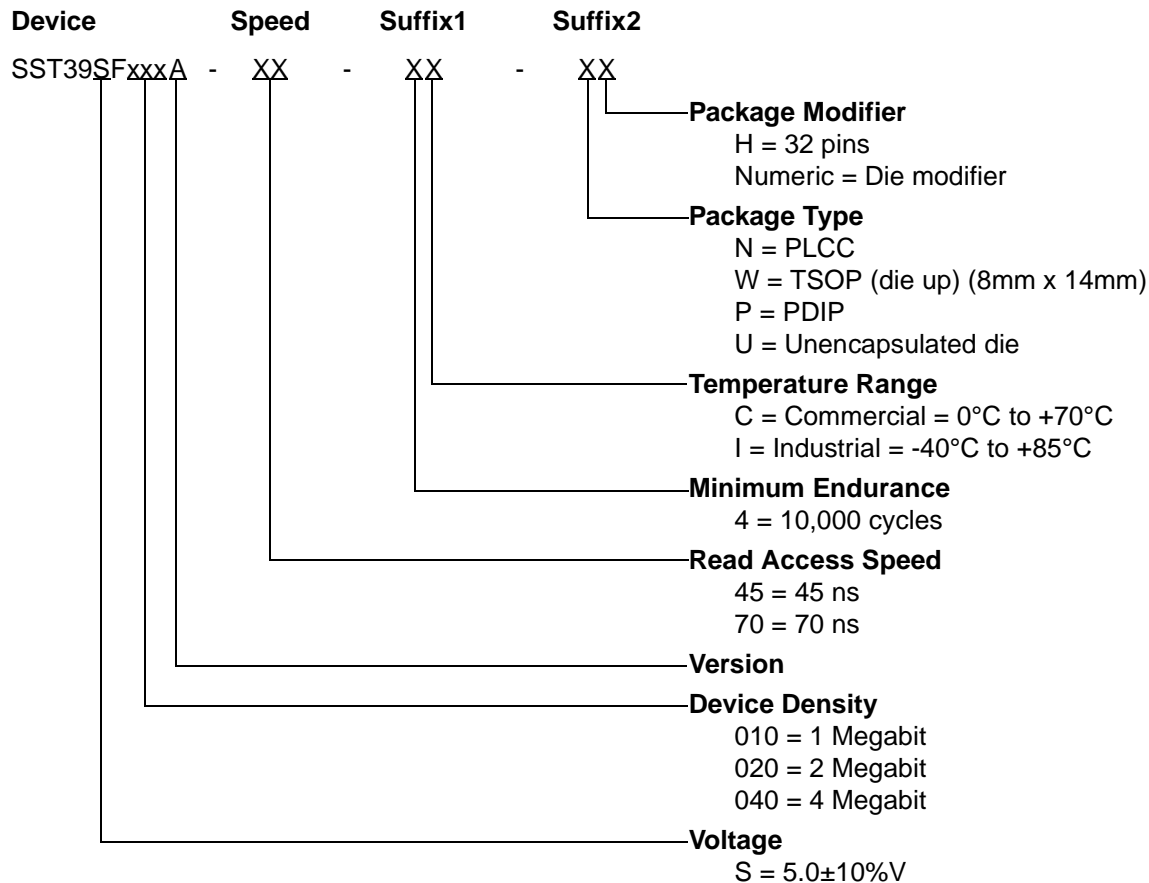


**FIGURE 18: ERASE COMMAND SEQUENCE**



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Preliminary Specification



## SST39SF040 Valid combinations

SST39SF040-45-4C-NH	SST39SF040-45-4C-WH	
SST39SF040-70-4C-NH	SST39SF040-70-4C-WH	SST39SF040-70-4C-PH
SST39SF040-45-4I-NH	SST39SF040-45-4I-WH	
SST39SF040-70-4I-NH	SST39SF040-70-4I-WH	

## SST39SF010A Valid combinations

SST39SF010A-45-4C-NH	SST39SF010A-45-4C-WH	
SST39SF010A-70-4C-NH	SST39SF010A-70-4C-WH	SST39SF010A-70-4C-PH
SST39SF010A-70-4C-U1		
SST39SF010A-45-4I-NH	SST39SF010A-45-4I-WH	
SST39SF010A-70-4I-NH	SST39SF010A-70-4I-WH	

## SST39SF020A Valid combinations

SST39SF020A-45-4C-NH	SST39SF020A-45-4C-WH	
SST39SF020A-70-4C-NH	SST39SF020A-70-4C-WH	SST39SF020A-70-4C-PH
SST39SF020A-70-4C-U1		
SST39SF020A-45-4I-NH	SST39SF020A-45-4I-WH	
SST39SF020A-70-4I-NH	SST39SF020A-70-4I-WH	

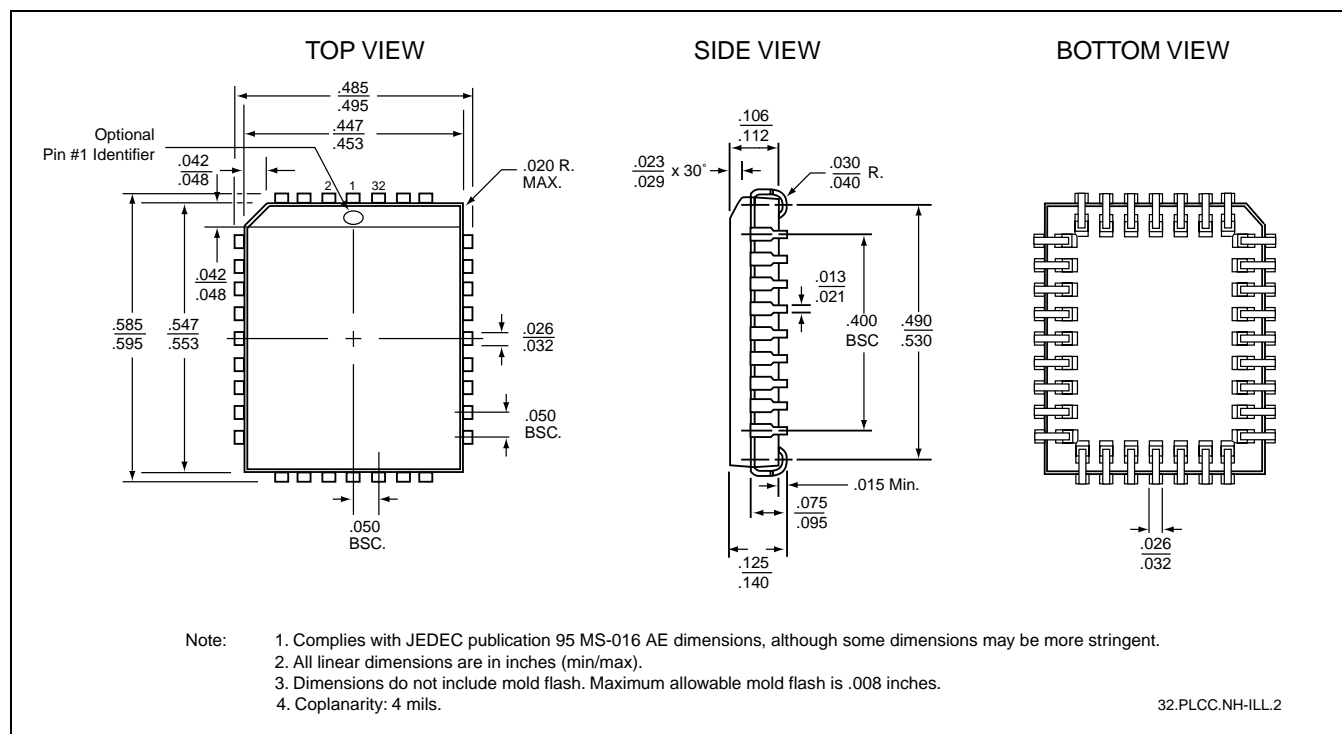
**Example:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



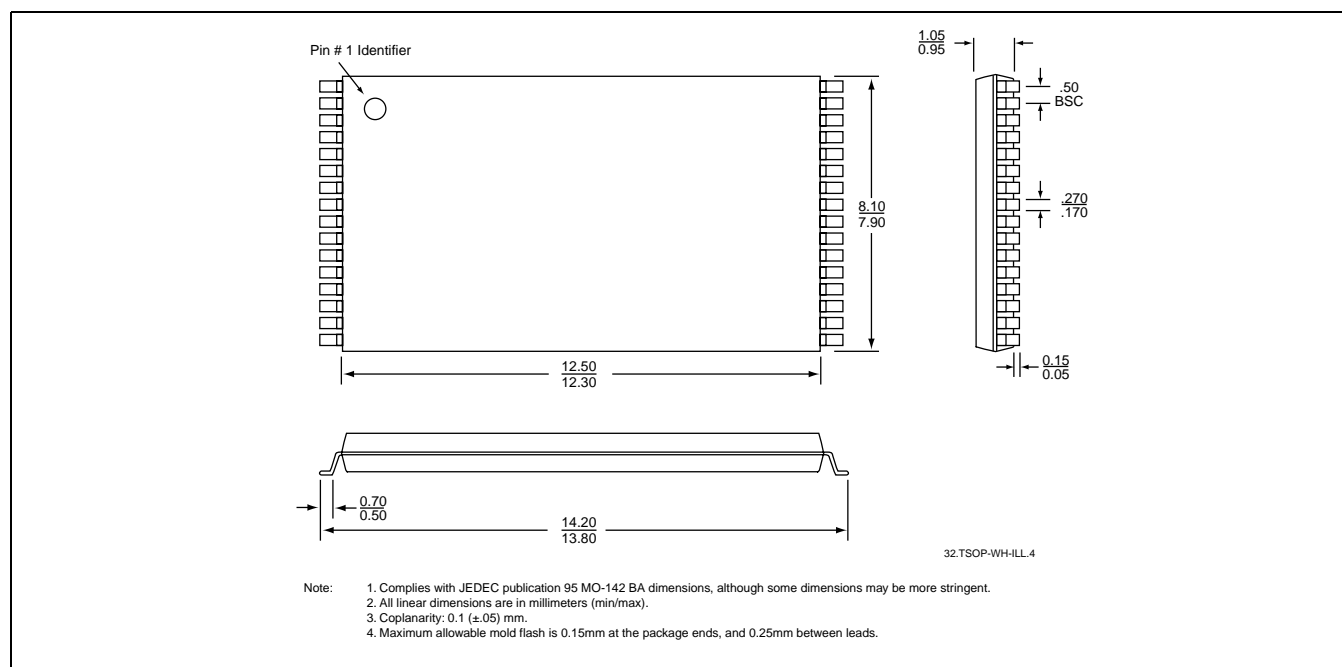
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Preliminary Specification

## PACKAGING DIAGRAMS



### 32-PIN PLASTIC LEAD CHIP CARRIER (PLCC) SST PACKAGE CODE: NH

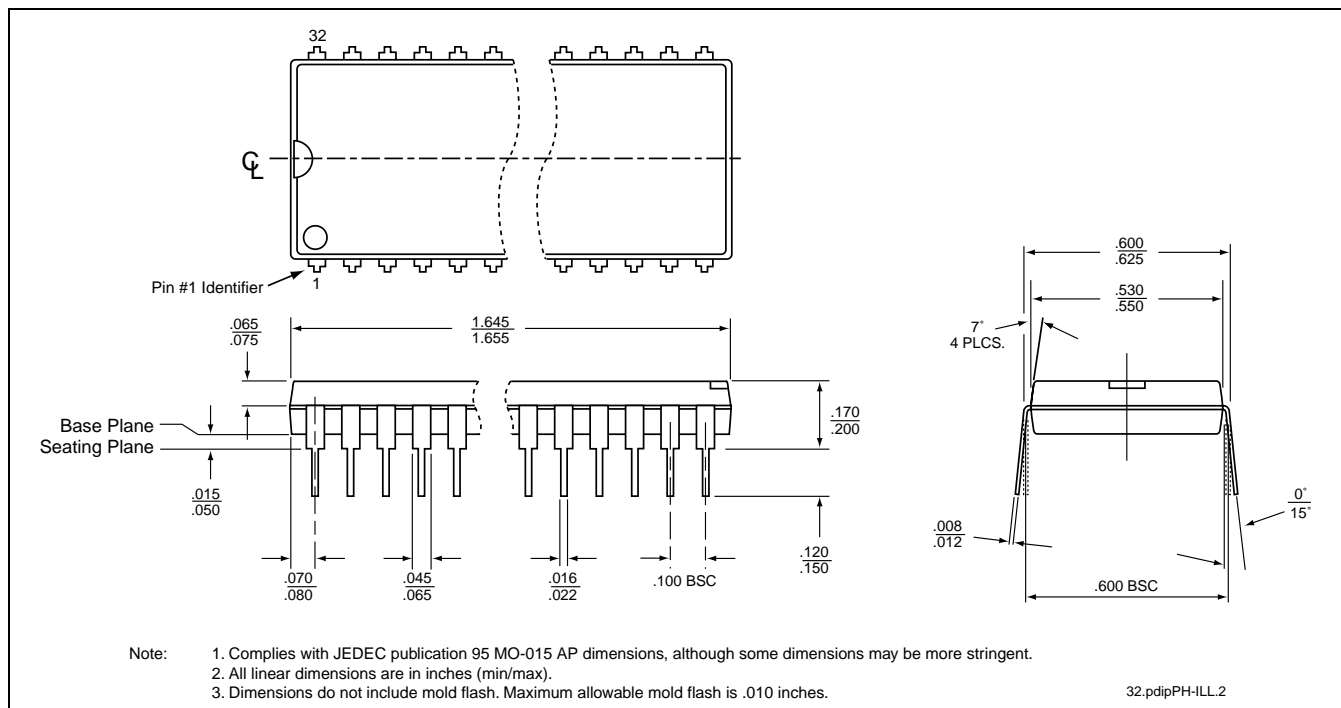


### 32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM SST PACKAGE CODE: WH



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Preliminary Specification



## 32-PIN PLASTIC DUAL-IN-LINE PACKAGE (PDIP)

SST PACKAGE CODE: PH