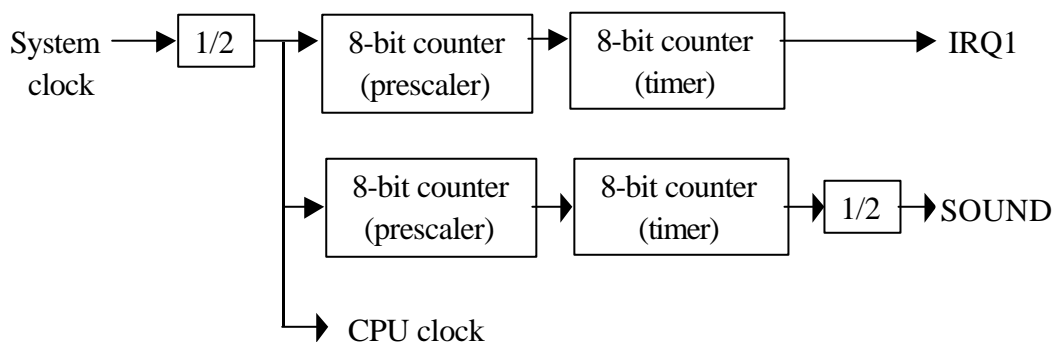




Specification

1. CHIP FEATURES :

- * Operating voltage : 2.5V-6.5V
- * Operating current : under 3mA at 3V.
- * Dual frequency
 - 32.768 KHz for LCD & 0.5 second timer interrupt.
 - RC or resonator oscillator for system clock.
 - CPU clock is half of system clock.
- * Built-in 2K bytes RAM, including LCD display RAM.
- * Built-in 64K bytes ROM with 16K bytes per bank.
- * Two chip enable signals. One can be expanded to 512K bytes with 16K per bank, and the other one can be expanded to 2M bytes with 16K per bank.
- * One 0.5 second pre-divider timer interrupt with start/stop control.
- * 2 output ports for key matrices
 - 14 pins for port 1, also used as address pins.
 - 4 input pins with wake-up interrupt for port 2.
 - Built-in pull-up resistors for port 2.
- * 8-bit timer with 8-bit prescale counter, both are auto-reloadable.



- * 8-bit sound generator with 8-bit prescaler, both are auto-reloadable.
- * Two LCD modes
 - LCD mode 1 : 80 segments, 16 commons, 1/5 bias, 1/16 duty and 64 Hz frame frequency.
 - LCD mode 2 : 65 segments, 32 commons, 1/5 bias, 1/32 duty and 64 Hz frame frequency.
- * Selectable 64 Hz Interrupt by NMI.
- * Timers and port 2 enable IRQ Interrupt.



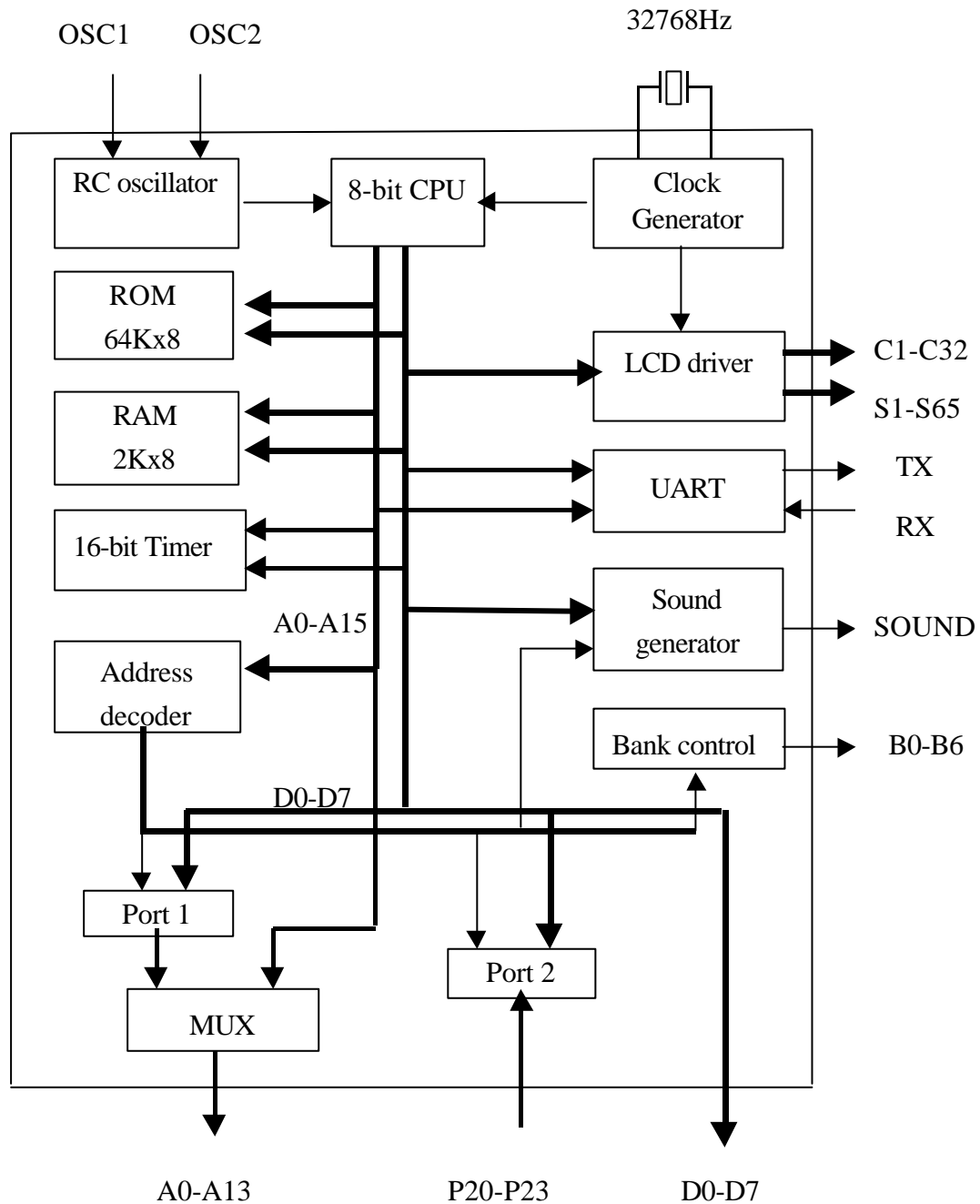
- * Timer range is programmable.
- * One output for the speaker.
 - 2 KHz or 4 KHz signal with two different envelopes are selectable for sound output.
- * One UART serial port with even parity check bit added after MSB for error detecting.
- * The internal ROM can be disabled and the corresponding memory area are mapped to the highest banks of external ROM.
- * Sleep mode : LCD off , crystal & system oscillator stop, Vdd=3V, Idd < 1 μ A.
Stand-by mode : LCD on and system oscillator stop, Vdd=3V, Idd < 80 μ A. LCD off
and system oscillator stop, Vdd=3V, Idd < 8 μ A.

2. APPLICATION:

- Data Bank
- Translator
- Organizer
- Hand-held game



3. BLOCK DIAGRAM:





4. PIN DESCRIPTION : (Total 149 pads)

Pin name	I/O	Description
COM1-COM32	O	Output pins for driving the commons of LCD panel
SEG1-SEG65	O	Output pins for driving the segments of LCD panel
SEG66-SEG80	O	Output pins for driving the segments of LCD panel. These pins are shared with COM18-COM32.
SOUND	O	Output pin for speaker
A0-A13	O	Address bus outputs shared with port 1 output
L0-L3	IU	4 input pins for key matrix with wake-up interrupt
D0-D7	I/O	Data pins
OSC1	I	RC/Crystal Oscillator input pin for system clock
OSC2	O	RC/Crystal Oscillator output pin for system clock (Note: CPU clock = system clock/2)
OSC3	I/O	RC Oscillator bi-directional pin for system clock
/RES	IU	Chip reset
VDD	I	Power input
VSS	I	Signal ground
LOSC1	I	Crystal oscillator input pin
LOSC2	O	Crystal oscillator output pin
BANK0-BANK4	O	To select external memory banks. The data on \$1209 will be output in these pins except during /CE2 read/write cycle. At that time these pins will output the data on \$120A
BANK5-BANK6	O	General purpose output pins. Also can be used to select external memory banks.
/CE1	O	External chip enable 1. This pin will be forced to high during sleep mode.
/CE2	O	External chip enable 2. This pin will be forced to high during sleep mode.
/TEST	IU	Test pin. Keep floating or connect to VDD
RWB	O	Read/Write signal output
VLCD	I	Power supply for LCD driver
VR	I	Contrast control for LCD
CLKOUT	O	512 Hz output clock for voltage doubler. This clock will be stopped if 32.768K Hz crystal is stopped



Pin name	I/O	Description
/DIROM	IU	Internal ROM control pin. =0 Disable internal ROM =1 Enable internal ROM
TX	O	Transmit data pin
RX	IU	Receive data pin

Note : IU -- Input pin with pull-up resistor.

5. ADDRESS ARRANGEMENT :

1) RAM

0000-009F : for LCD output data storage while operating in LCD mode 1.
for data area while operating in LCD mode 2.

	SEG1-SEG8	SEG9-SEG16	• • •	SEG65-SEG72	SEG73-SEG80
COM1	0000	0010	• • •	0080	0090
COM2	0001	0011	• • •	0081	0091
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
COM16	000F	001F	• • •	008F	009F

* The LSB of low byte - SEG1
The MSB of high byte - SEG80
Middle bits are in order.

00A0-00FF : for zero page area
0100-01FF : for stack area
0200-031F : for data area while operating in LCD mode 1.
for LCD data area while operating in LCD mode 2.



	SEG1-SEG8	SEG9-SEG16	• • •	SEG57-SEG64	SEG65
COM1	0200	0220	• • •	02E0	0300
COM2	0201	0221	• • •	02E1	0301
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
COM32	021F	023F		02FF	031F

* The LSB of low byte - SEG1

The LSB of high byte - SEG65

Middle bits are in order.

0320-07FF : for data area

4000-7FFF : for external chip enable 1. While this area is accessed, /CE1 will be low and the data in \$1209 will be output on BANK0-BANK4. If bit 0 of \$121A is set to one, then this area can not be accessed.

2) ROM

8000-BFFF : for external chip 2 or internal ROM banks.

/DIROM	\$121A		Function description
	Bit 1	Bit 0	
X	0	0	This area is external memory. /CE2 will be low and the data in \$120A will output to BANK0-BANK6.
X	0	1	This condition is prohibited.
0	1	0	This area is external memory. /CE2 will be low and the value of \$1209 will be sent to BANK0-4.
0	1	1	This condition is prohibited.
1	1	X	This area is internal ROM. /CE2 will keep high. \$1209 defines the bank number of internal ROM. The internal ROM are located at bank 1CH-1FH. Bank 00H is used to define the volume of sound output.



C000-FFFF : for program memory

/DIROM	Bit 0 of \$121A	Function description
0	0	This area is external memory. /CE2 will be low and BANK4-BANK0=1FH.
0	1	This condition is prohibited.
1	X	The internal ROM bank 1FH is selected. /CE2 will be high.

FFFF,FFFE - IRQ vector

FFFD,FFFC - RES vector

FFFB,FFFA - NMI vector

3) Others

1200 To enter stand-by mode; write only.

- * In standby mode, the system oscillator will be stopped. But 32768Hz crystal will still work.
- * The CPU, UART and timer will be stopped.
- * LCD state is depended on bit 1 of \$120D.
- * NMI and IRQ3 are still functionally.
- * When in stand-by mode, NMI, IRQ2 or IRQ3 will wake up the CPU.

1201 To enter sleep mode; write only.

Bit 1 : = 0 Disable sleep mode
 = 1 Enable sleep mode

In sleep mode, whole chip will be stopped. That is, the system and 32768 Hz crystal oscillator will be stopped. The bit 1 of \$120D will be reset. Only reset and IRQ2 will wake up this chip.

1202 Sound output control

Bit 0 : For base frequency

	1/32 duty	1/16 duty
= 0	4 KHz	2 KHz
= 1	8 KHz	4 KHz

2-1 : = 0x Sound off

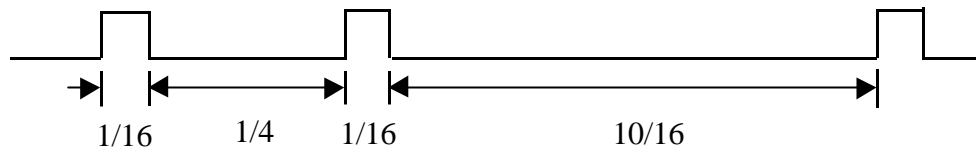
 = 10 For alarm envelope

 = 11 Sound always on



* The default value for each bit is zero.

Alarm envelope waveform: (unit = second)



1203 IRQ flag register; read & write.

- * Read : Bit 0 : if 1, timer interrupt, IRQ1.
Bit 1 : if 1, port 2 interrupt, IRQ2.
Bit 2 : if 1, 0.5 sec. timer interrupt, IRQ3.
Bit 3 : if 1, transmit data complete interrupt, IRQ4.
Bit 4 : if 1, receiver data ready interrupt, IRQ5.

- * Write : Bit 0 : if 0, clear the flag of IRQ1.
Bit 1 : if 0, clear the flag of IRQ2.
Bit 2 : if 0, clear the flag of IRQ3.
Bit 3 : if 0, clear the flag of IRQ4.
Bit 4 : if 0, clear the flag of IRQ5.

* When the system is in IRQ mode, the IRQ flag register must be cleared before having another interrupt request; otherwise, the system will always be in IRQ mode.

1204 Low byte data for port 1; write only.

The output data pins are shared with A0-A7.

1205 High byte data for port 1; write only.

Bit 5-0 : Output data. The output data pins are shared with A8-A13.

1206 Write: load prescaler value and timer value from buffer to counter

Read : read current counter value

* After \$1206 been written, timer will begin to count down. And IRQ1 happens when timer counts to zero.

elapsed time = $\$120B * (\$120C + 1) / (\text{system clock} / 2)$.

1207 Port 2 data; read only

Bit 3-0 : Input data . One wait state will be added while reading this port.



1208 Set port 2 bit interrupt function; write only.

- * An '0' in this register will set the interrupt function of the corresponding pin of port 2 to be enabled.
- * The port 2 interrupt is enabled only during sleep or standby mode.
- * The default value for each bit is one.

1209 For selecting the memory bank of external chip 1 or internal ROM; write only

Bit 4-0 : set bank number of external chip 1.

120A For selecting the memory bank of external chip 2; write only

Bit 4-0 : set bank number of external chip 2.

6-5 : General purpose output data.

120B Write initial timer prescaler value to buffer; write only

120C Write initial timer value to buffer; write only

120D Control register; write only

- | | | | | | |
|-----|---|---|---|---|---|
| Bit | 0 | : | = | 0 | Disable 64 Hz NMI |
| | | | = | 1 | Enable 64 Hz NMI (NMI frequency = 64Hz) |
| | 1 | : | = | 0 | LCD off |
| | | | = | 1 | LCD on |
| | 2 | : | = | 0 | Disable timer |
| | | | = | 1 | Enable timer |
| | 3 | : | = | 0 | Disable IRQ1 |
| | | | = | 1 | Enable IRQ1 |
| | 4 | : | = | 0 | Operating in LCD mode 1 |
| | | | = | 1 | Operating in LCD mode 2 |

The default value is zero.

120E 0.5 sec timer interrupt; write only

- | | | | | |
|-------|---|---|---|------------------------------------|
| Bit 0 | : | = | 0 | Stop 0.5 second timer and reset it |
| | | = | 1 | Start 0.5 second timer |

When 0.5 second is elapsed, IRQ3 will occur.

120F Select oscillator warm-up time.



Bit 0 : = 0 warm-up time is 4 system clocks, for RC oscillator
= 1 warm-up time is 31.25ms, for crystal oscillator

1214 Load baud rate counter value to buffer; write only.

Baud rate = (system clock)/16/([1214]+1)

Example: For system clock = 2MHz

Baud rate	Counter Value (Dec)	Actual Baud rate	Error (%)
1200	103	1201.92	0.16
2400	51	2403.85	0.16
3600	34	3571.43	-0.79
4800	25	4807.69	0.16
7200	16	7352.94	2.12
9600	12	9615.38	0.16

1215 Load baud rate counter value from buffer to counter to generate desired baud rate; write only.

1216 Read : read the received data from buffer

Write: load data to buffer for transmission

1217 UART status register; read only.

Bit 0 : = 0 Received data no error
= 1 Received data parity error
1 : = 0 Transmit buffer not ready
= 1 Transmit buffer empty

1218 Write initial prescaler value to sound generator; write only

1219 Write initial value to sound generator; write only

* Output frequency = system clock/[(1219)+1]/[(1218)+1]/4

121A Control register. Write only.

Bit 0 : = 0 Enable external memory expansion. \$8000-\$BFFF are external memory. A0-A13 are shared with port 1. D0-D7 are data bus.
= 1 Disable external memory expansion. \$8000-\$BFFF are internal



ROM. A0-A13 are output port 1 and D0-D7 are data bus.

1 := 0 \$8000-\$BFFF are external memory bank.

= 1 \$8000-\$BFFF are internal ROM bank.

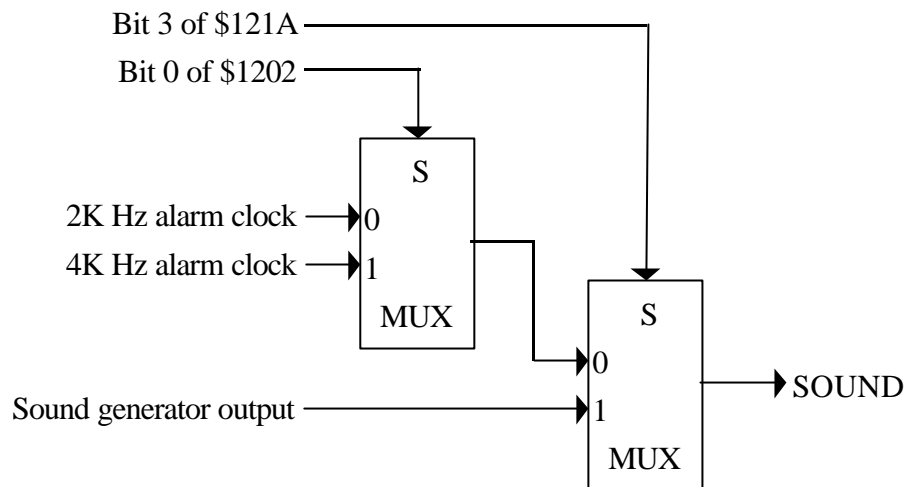
3 := 0 Select alarm clock output.

= 1 Select sound generator output.

4 := 0 Disable sound generator.

= 1 Enable sound generator.

The default value is zero.



4) The reset status of CPU

If the /RES is keep low more than two system clocks, then the CPU will be reset. After reset, the interrupt mask flag is set, the decimal mode is cleared and the program counter will be loaded with the reset vector from address \$FFFC and \$FFFD. So, **after initial procedure the firmware should do a 'CLI' instruction.** Otherwise, the CPU will not acknowledge any interrupt.

5) Interrupts

* There are six interrupt sources :

NMI - 64 Hz interrupt

IRQ1 - Timer interrupt

IRQ2 - Sleep and Stand-by interrupts by port 2

IRQ3 - 0.5 second timer interrupt

IRQ4 - Transmit buffer ready interrupt

IRQ5 - Receiver data ready interrupt

* Only IRQ2 will wake up CPU from sleep mode.

* Only IRQ2, IRQ3 and NMI can wake up CPU from stand-by mode.

* An oscillator warm-up time (4 cycles or 31.25ms) will be added before CPU been waken up from standby or sleep mode.

* After CPU wake up from sleep mode, programmer should turn on LCD again.

* 0.5 sec. timer interrupt, with start/stop control, is operated by writing \$120E.

* When port 2 interrupt is enabled, a low signal from any pin will generate IRQ2.



- * Before starting timer, load new prescaler value (by writing \$120B) or new timer value (by writing \$120C) to buffer for having different IRQ time ranges. Otherwise, write \$1206 to have the same IRQ time range as the previous one's.
- * When the CPU acknowledge the interrupt, following things will be done:
 - a) The interrupt mask flag will be set by CPU
 - b) The return address and status register will be pushed to stack.
- * When the CPU return from interrupt routine by RTI instruction following things will be done:
 - a) The return address and status register will be pulled from stack.
 - b) The interrupt mask flag will be cleared.
- * **It is not necessary to add SEI and CLI instructions in interrupt routine.** If a CLI instruction is added in the interrupt routine, then another interrupt may be inserted during current interrupt routine and may cause stack overflow.

6) Serial port

- * Load baud rate counter value (by writing \$1214) to buffer then load it from buffer to counter(by writing \$1215) to generate desired baud rate.
- * Write \$1216 to transmit data, one byte at a time. When one data byte has been transmitted, hardware generates IRQ4 interrupt (transmit buffer ready).
- * When one data byte is received, hardware generates IRQ5 interrupt (receiver data ready). Read \$1216 to fetch data from buffer.
- * Read \$1217 bit 0 to check if data received is correct and read bit 1 to check when next data byte can be transmitted.
- * When system is in stand-by mode, serial port is disabled.

7) Internal ROM.

The internal 64K bytes ROM are split to 4 banks. The bank number is defined by \$1209 and the internal ROM are located at bank 1CH to 1FH. Only bank 1FH can be read from CPU address 0C000H-0F000H. All the other banks can be read from 8000H-0BFFFH by set \$1209 to the bank number and set bit 1 of \$121A to one.

8) Sound volume.

To change the volume, please follow the procedures listed below :

- a) Write zero to \$1209.
- b) Set bit 1 of \$121A to one.
- c) Set 0 to bit 0 of \$8001 to enable the melody output.



d) Write the volume value to \$8000 (bit 0 is do not care).

The default value of volume is \$FF.

9) Speech output.

To enable the speech function, please follow the procedures listed below :

a) Write zero to \$1209.

b) Set bit 1 of \$121A to one.

c) Set 1 to bit 0 of \$8001 to disable the melody output and have the DAC always on.

d) Change the volume data in \$8000 according to the speech data (bit 0 is do not care).

e) Repeat a), b) and d) to change the speech data.

f) After the speech data is finished, repeat procedure a) and b) and then write 0 to bit 0 of \$8001.

g) Due to the value of \$1209 will be changed during speech output, the speech output program should be located on the \$C000-\$FFFF area.

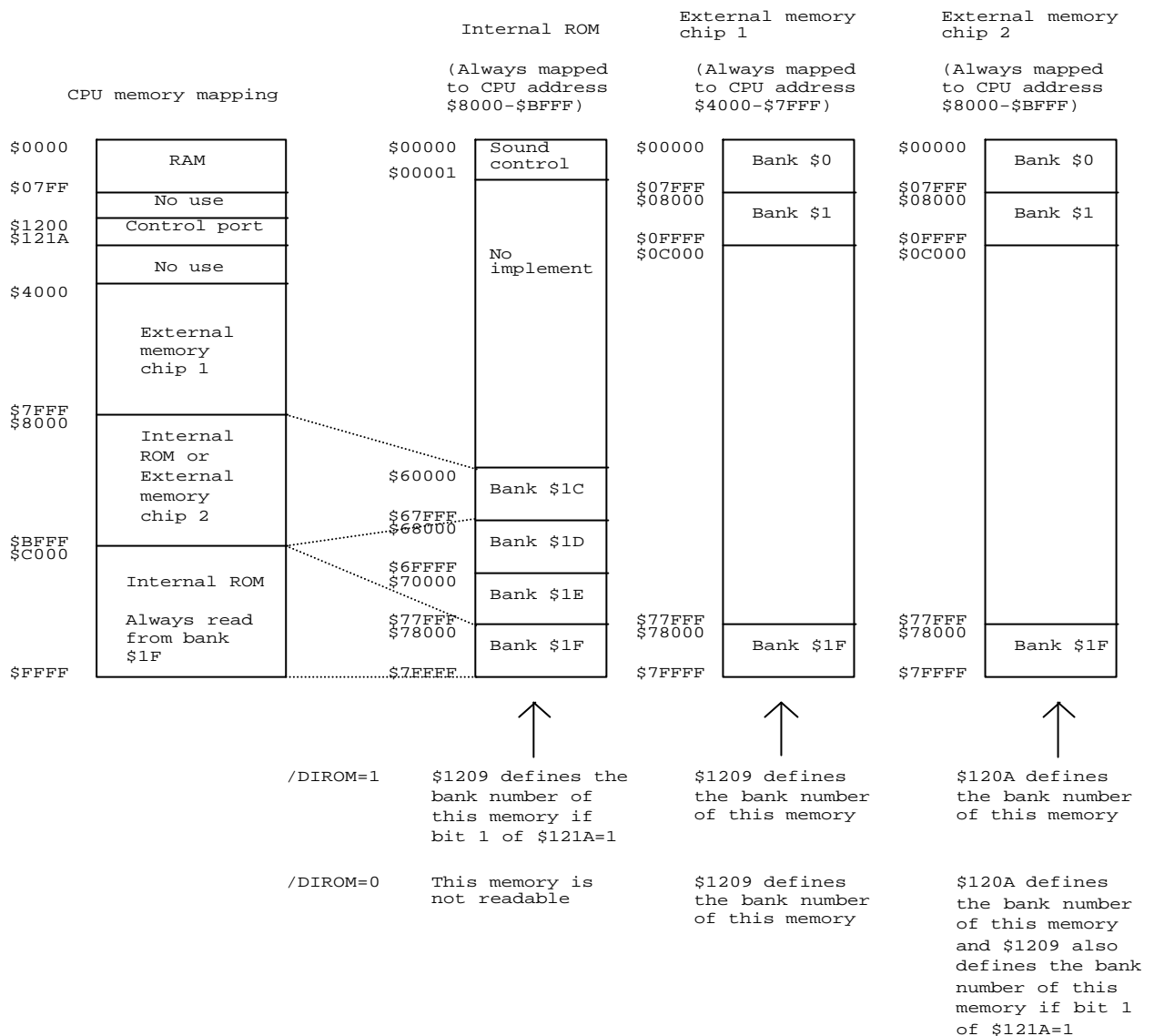
(Note : If there is no speech or melody output, then either the bit 0 of \$8001 or \$8000 should be kept at zero. Otherwise, a DC current may flow through the external speaker drive circuit.)

10) Summary for accessing each bank of memory:

/DIROM	Bit 1 of \$121A	Bit 0 of \$121A	Remarks
0	0	0	\$4000 - \$7FFF: CE1, bank = (\$1209) \$8000 - \$BFFF: CE2, bank = (\$120A) \$C000 - \$FFFF: CE2, bank = \$1F
0	0	1	Prohibited
0	1	0	\$4000 - \$7FFF: CE1, bank = (\$1209) \$8000 - \$BFFF: CE2, bank = (\$1209) \$C000 - \$FFFF: CE2, bank = \$1F
0	1	1	Prohibited
1	0	0	\$4000 - \$7FFF: CE1, bank = (\$1209) \$8000 - \$BFFF: CE2, bank = (\$120A) \$C000 - \$FFFF: internal, bank = \$1F
1	0	1	Prohibited
1	1	0	\$4000 - \$7FFF: CE1, bank = (\$1209) \$8000- \$BFFF: internal, bank = (\$1209)



/DIROM	Bit 1 of \$121A	Bit 0 of \$121A	Remarks
			\$C000 - \$FFFF: internal, bank = \$1F
1	1	1	\$4000 - \$7FFF: CE1 not accessible \$8000 - \$BFFF: internal, bank = (\$1209) \$C000 - \$FFFF: internal, bank = \$1F



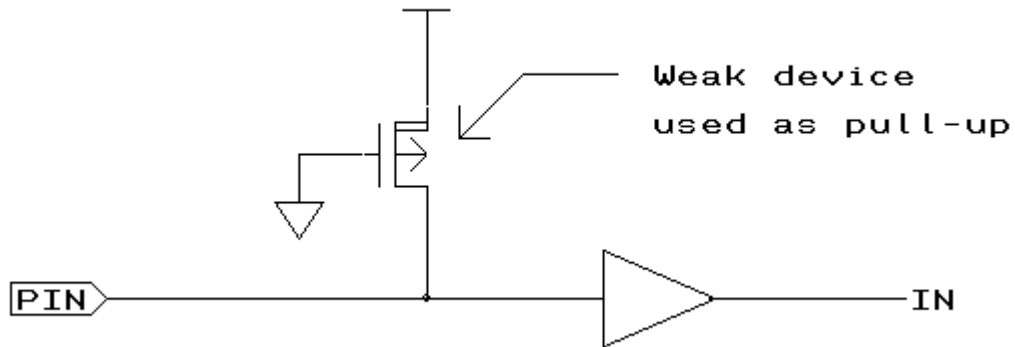


- 11) The sound volume or voice level can only be set at internal \$C000-\$FFFF bank or external \$C000-\$FFFF bank. (Unable to set at \$8000- \$BFFF bank , whether it is internal ROM program or external ROM program, also unable to set at \$4000-\$7FFF bank).

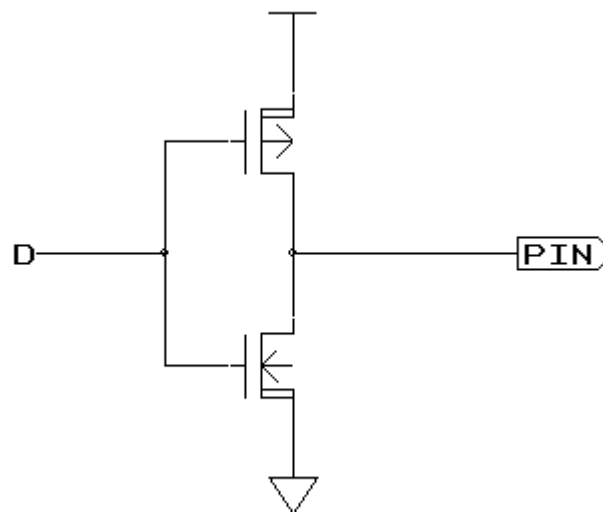


6. I/O STRUCTURE :

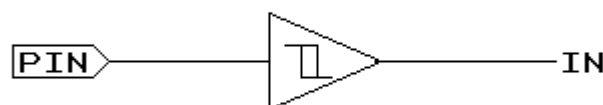
6.1 For L0-L3 :



6.2 For output pins :

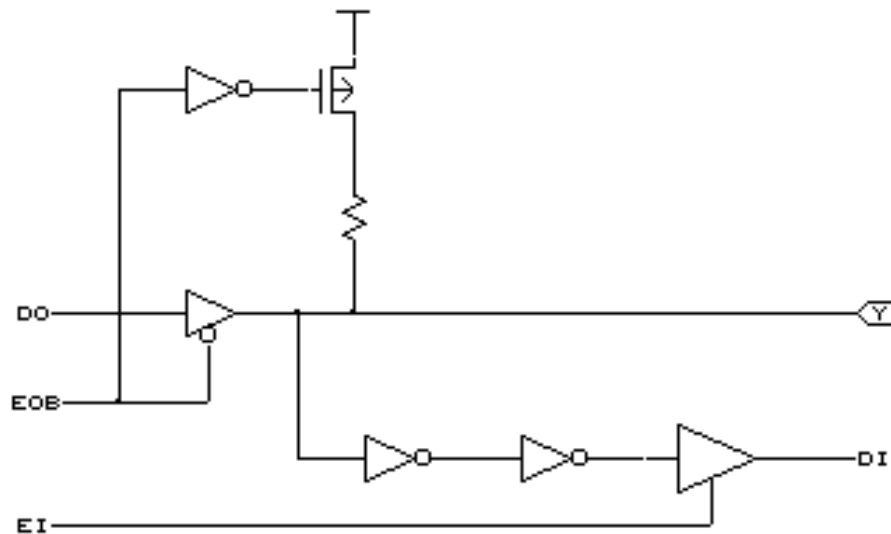


6.3 /RES pin :

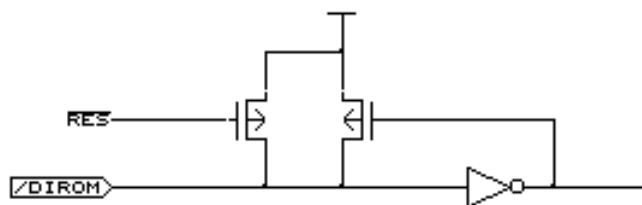




6.4 For I/O pins :

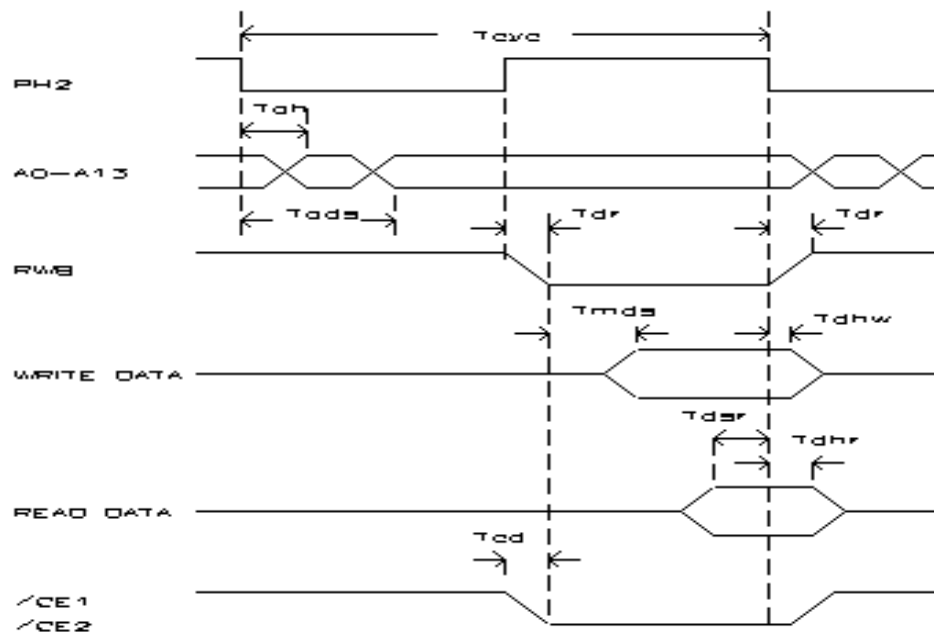


6.5 /DIROM pin :





7. TIMING DIAGRAM FOR EXTERNAL MEMORY ACCESS :



Description	Symbol	Min.	Typ.	Max.	Unit
Cycle Time	Tcyc		500		nS
Address hold time	Tah	10			nS
Address delay time	Tads			100	nS
Delay time	Tdr			10	nS
Write data delay time	Tmds			100	nS
Write data hold time	Tdhw	10			nS
Read data setup time	Tdsr	40			nS
Read data hold time	Tdhr	10			nS

8. ABSOLUTE MAXIMUM RATINGS :

Operating temperature 0 to 70
Storage temperature -65 to 150
Supply voltage 7 V
Input voltage -0.6 to Vdd+0.6 V



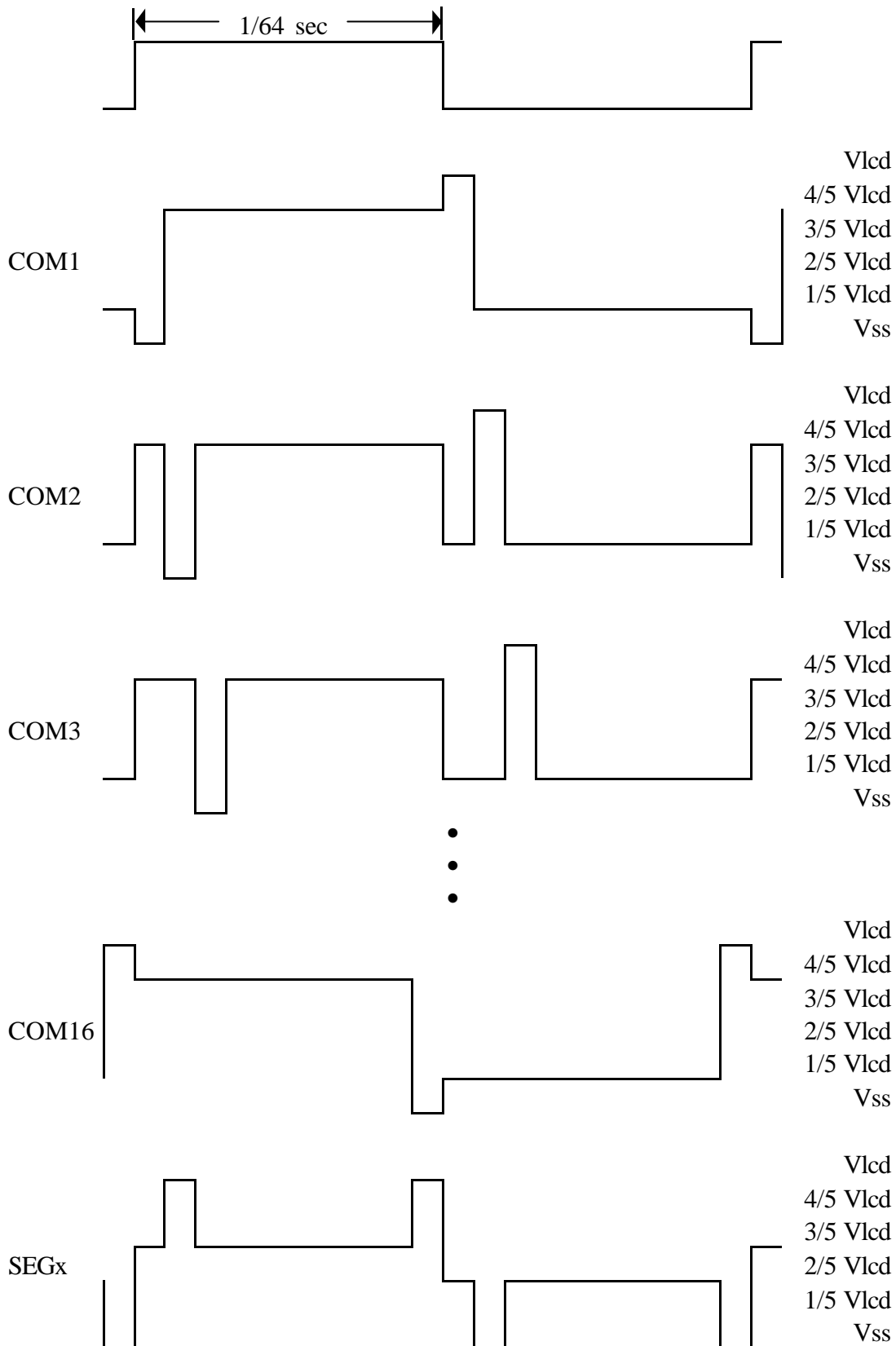
9. ELECTRICAL CHARACTERISTIC :

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	Vdd		2.5	3.0	6.5	V
Main system frequency	Øsys	Vdd=3V		1	5	Mhz
		Vdd=4.5V			7	Mhz
Crystal frequency	Øcry			32768		Hz
Operating current	Idd	Vdd=3V, Øsys=1Mhz		1.1		mA
Sleep current	Islp	Vdd=3.5V			1	µA
Standby current (LCD on)	Istdby	Vdd=2.5V, Vlcd=4V		81		µA
		Vdd=2.7V, Vlcd=4.5V		97		µA
		Vdd=3V, Vlcd=5.1V		124		µA
		Vdd=3.5V, Vlcd=6V		183		µA
		Vdd=4V, Vlcd=Vdd		83		µA
		Vdd=4.5V, Vlcd=Vdd		103		µA
		Vdd=5V, Vlcd=Vdd		124		µA
Standby current (LCD off)		Vdd=2.5V		3		µA
		Vdd=2.7V		3.5		µA
		Vdd=3V		4.1		µA
		Vdd=3.5V		5.3		µA
		Vdd=4V		6.5		µA
		Vdd=4.5V		8.3		µA
		Vdd=5V		11		µA
Input high voltage	Vih	Vdd=3.0V	1.5			V
Input low voltage	Vil	Vdd=3.0V	-0.6		0.6	V
Input high leakage current	Iih	Vih=Vdd			-1	µA
Input low leakage current	Iil	Vil=0			1	µA
Output high voltage (For SEGx and COMx)	Voh1	Ioh=-30µA	Vlcd -0.2		Vlcd	V
Output low voltage (for SEGx and COMx)	Vol1	Iol=40µA	0		0.2	V
Output high voltage (for other pins)	Voh2	Ioh=-4mA	Vdd- 0.8		Vdd	V
Output low voltage (for other pins)	Vol2	Iol=4mA	0		0.8	V



10. LCD WAVEFORM :

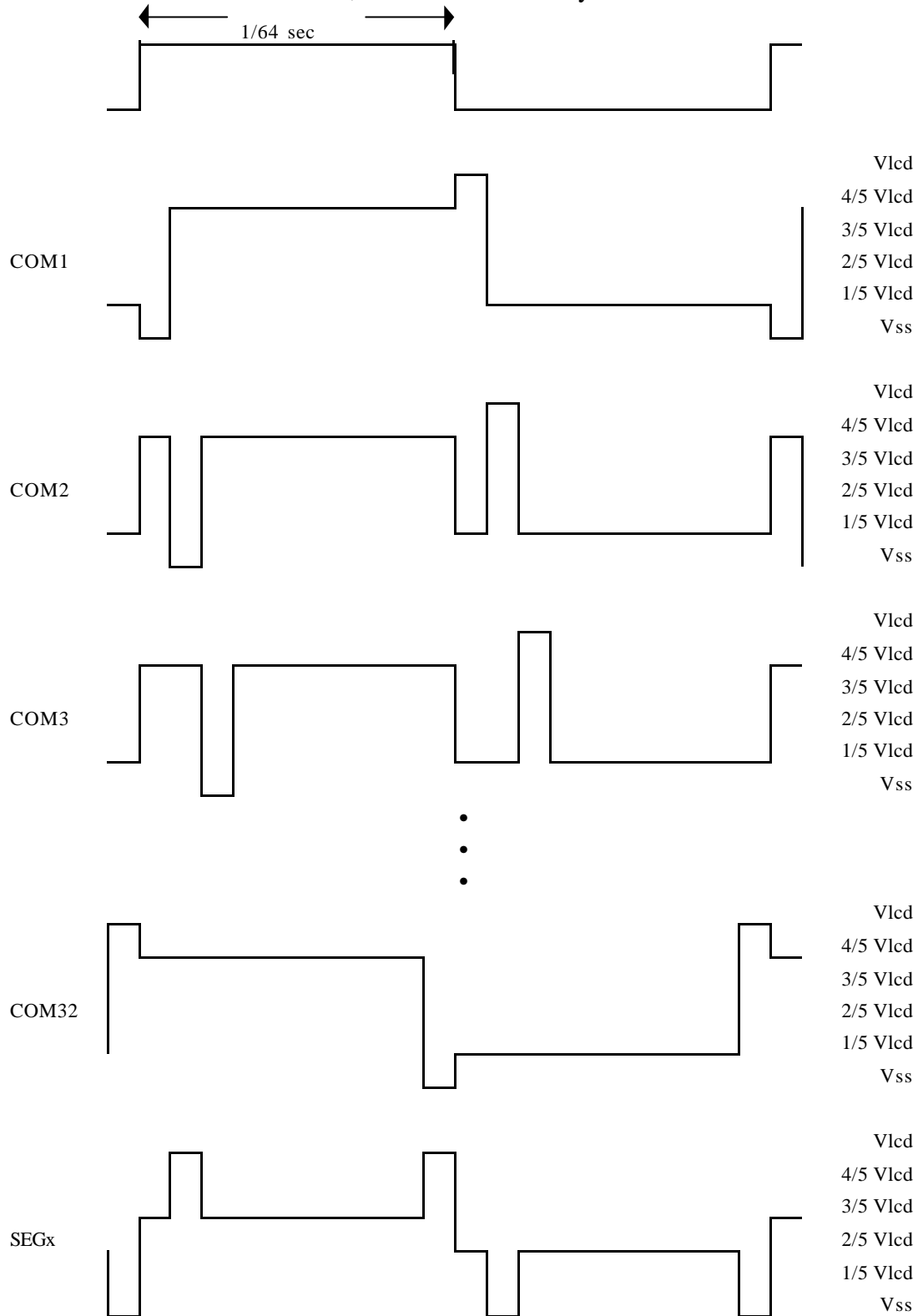
10.1 LCD mode 1 : 80 x 16, 1/5 bias and 1/16 duty





There are two LCD matrix DOTs active at (SEGx,COM2) and (SEGx,COM16)

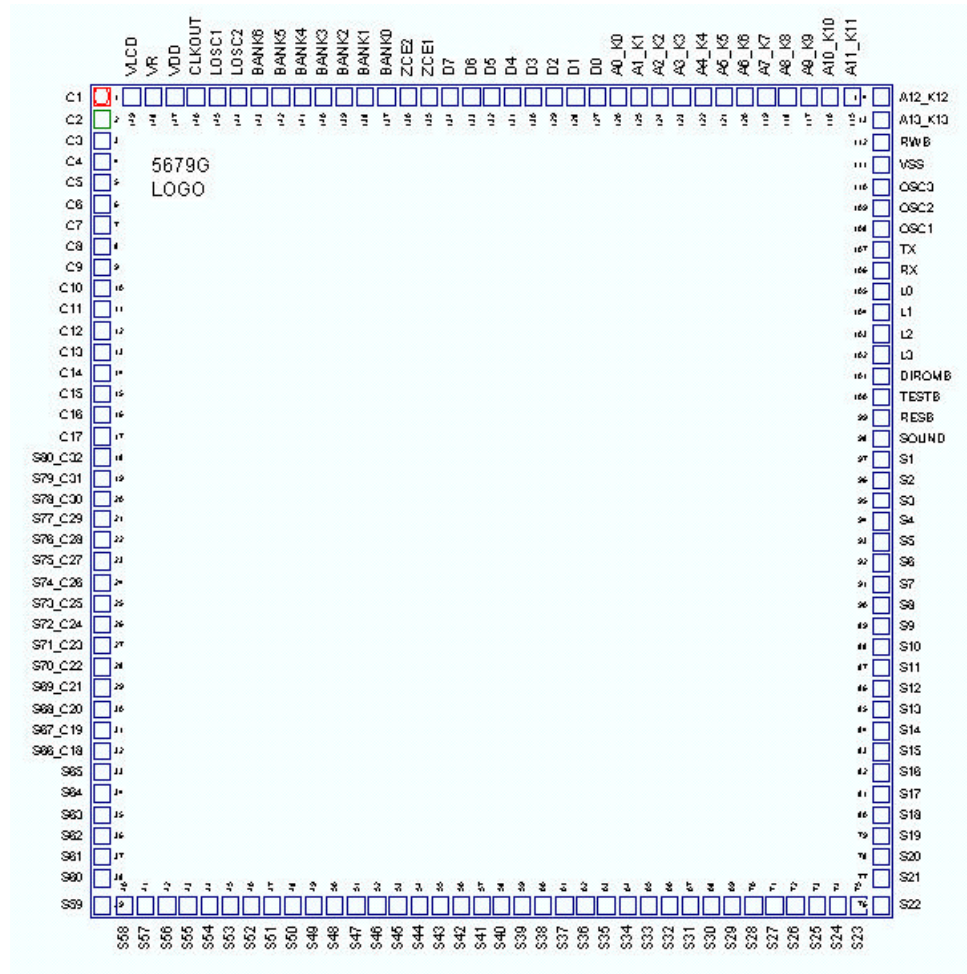
10.2 LCD mode 2 : 65 x 32, 1/5 bias and 1/32 duty



There are two LCD matrix DOTs active at (SEGx,COM2) and (SEGx,COM32)



11. PAD LOCATION :





Chip size : 4480 x 4650

Unit : μM

PAD-No	Name	X	Y	PAD-No	Name	X	Y
1	C1	65.00	4585.00	76	S22	4416.00	65.00
2	C2	65.00	4460.00	77	S21	4416.00	218.00
3	C3	65.00	4339.80	78	S20	4416.00	338.00
4	C4	65.00	4222.10	79	S19	4416.00	455.00
5	C5	65.00	4104.40	80	S18	4416.00	572.00
6	C6	65.00	3986.70	81	S17	4416.00	689.00
7	C7	65.00	3869.00	82	S16	4416.00	806.00
8	C8	65.00	3751.30	83	S15	4416.00	923.00
9	C9	65.00	3633.60	84	S14	4416.00	1040.00
10	C10	65.00	3515.90	85	S13	4416.00	1157.00
11	C11	65.00	3398.20	86	S12	4416.00	1274.00
12	C12	65.00	3280.50	87	S11	4416.00	1391.00
13	C13	65.00	3162.80	88	S10	4416.00	1508.00
14	C14	65.00	3045.10	89	S9	4416.00	1625.00
15	C15	65.00	2927.40	90	S8	4416.00	1742.00
16	C16	65.00	2809.70	91	S7	4416.00	1859.00
17	C17	65.00	2692.00	92	S6	4416.00	1976.00
18	S80_C32	65.00	2574.30	93	S5	4416.00	2093.00
19	S79_C31	65.00	2456.60	94	S4	4416.00	2210.00
20	S78_C30	65.00	2338.90	95	S3	4416.00	2327.00
21	S77_C29	65.00	2221.20	96	S2	4416.00	2444.00
22	S76_C28	65.00	2103.50	97	S1	4416.00	2561.00
23	S75_C27	65.00	1985.80	98	SOUND	4416.00	2678.00
24	S74_C26	65.00	1868.10	99	RESB	4416.00	2795.00
25	S73_C25	65.00	1750.40	100	TESTB	4416.00	2912.00
26	S72_C24	65.00	1632.70	101	DIROMB	4416.00	3029.00
27	S71_C23	65.00	1515.00	102	L3	4416.00	3146.00
28	S70_C22	65.00	1397.30	103	L2	4416.00	3263.00
29	S69_C21	65.00	1279.60	104	L1	4416.00	3380.00
30	S68_C20	65.00	1161.90	105	L0	4416.00	3497.00
31	S67_C19	65.00	1044.20	106	RX	4416.00	3614.00
32	S66_C18	65.00	926.50	107	TX	4416.00	3731.00
33	S65	65.00	808.80	108	OSC1	4416.00	3848.00



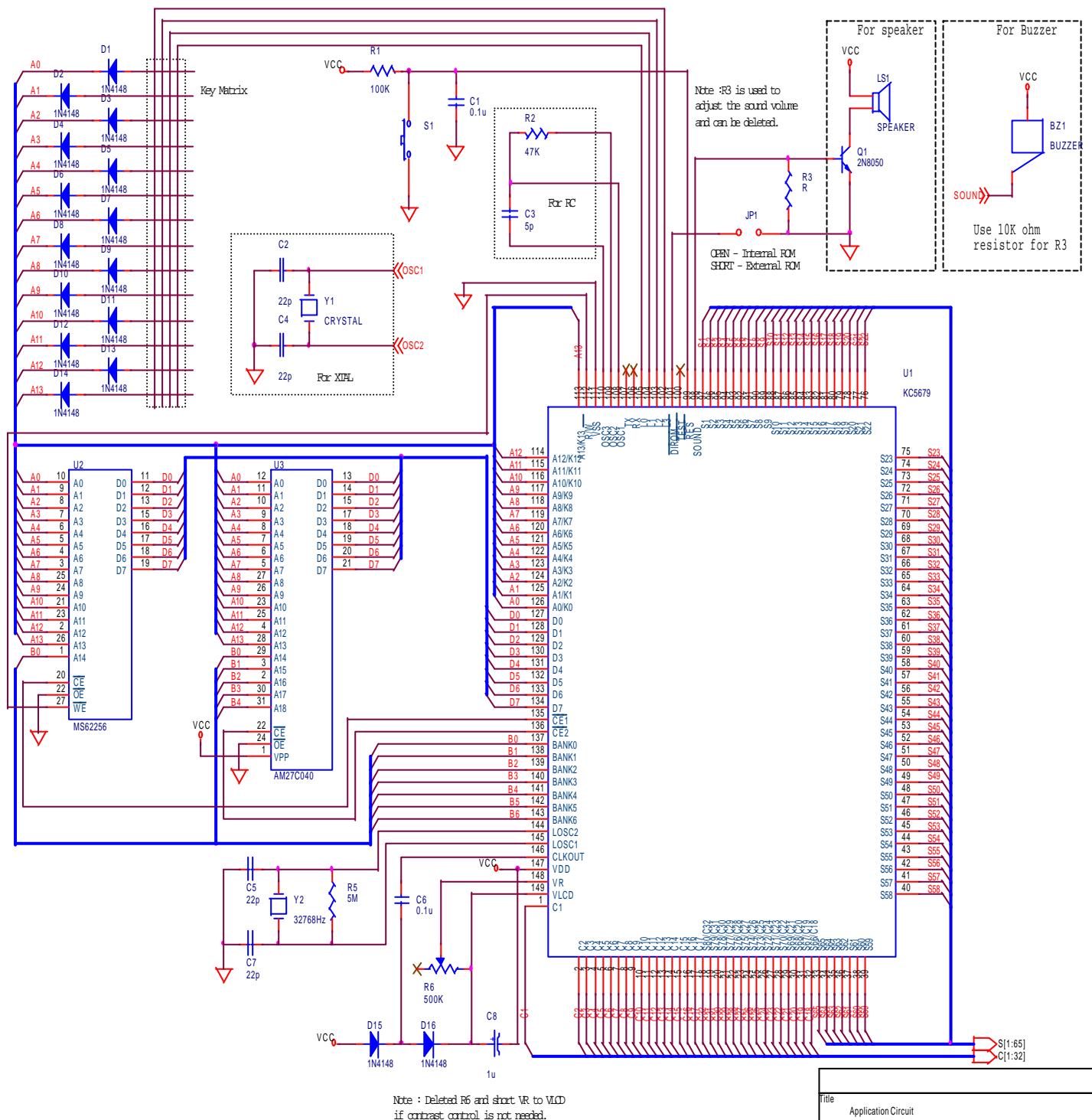
PAD-No	Name	X	Y	PAD-No	Name	X	Y
34	S64	65.00	691.10	109	OSC2	4416.00	3965.00
35	S63	65.00	573.40	110	OSC3	4416.00	4082.00
36	S62	65.00	455.70	111	VSS	4416.00	4205.60
37	S61	65.00	338.00	112	RWB	4416.00	4330.60
38	S60	65.00	218.00	113	A13_K13	4416.00	4455.60
39	S59	65.00	65.00	114	A12_K12	4416.00	4585.00
40	S58	190.00	65.00	115	A11_K11	4251.00	4585.00
41	S57	310.00	65.00	116	A10_K10	4129.00	4585.00
42	S56	427.00	65.00	117	A9_K9	4011.00	4585.00
43	S55	544.00	65.00	118	A8_K8	3893.00	4585.00
44	S54	661.00	65.00	119	A7_K7	3775.00	4585.00
45	S53	778.00	65.00	120	A6_K6	3657.00	4585.00
46	S52	895.00	65.00	121	A5_K5	3539.00	4585.00
47	S51	1012.00	65.00	122	A4_K4	3421.00	4585.00
48	S50	1129.00	65.00	123	A3_K3	3303.00	4585.00
49	S49	1246.00	65.00	124	A2_K2	3185.00	4585.00
50	S48	1363.00	65.00	125	A1_K1	3067.00	4585.00
51	S47	1480.00	65.00	126	A0_K0	2949.00	4585.00
52	S46	1597.00	65.00	127	D0	2831.00	4585.00
53	S45	1714.00	65.00	128	D1	2713.00	4585.00
54	S44	1831.00	65.00	129	D2	2595.00	4585.00
55	S43	1948.00	65.00	130	D3	2477.00	4585.00
56	S42	2065.00	65.00	131	D4	2359.00	4585.00
57	S41	2182.00	65.00	132	D5	2241.00	4585.00
58	S40	2299.00	65.00	133	D6	2123.00	4585.00
59	S39	2416.00	65.00	134	D7	2005.00	4585.00
60	S38	2533.00	65.00	135	ZCE1	1887.00	4585.00
61	S37	2650.00	65.00	136	ZCE2	1769.00	4585.00
62	S36	2767.00	65.00	137	BANK0	1651.00	4585.00
63	S35	2884.00	65.00	138	BANK1	1533.00	4585.00
64	S34	3001.00	65.00	139	BANK2	1415.00	4585.00
65	S33	3118.00	65.00	140	BANK3	1297.00	4585.00
66	S32	3235.00	65.00	141	BANK4	1179.00	4585.00
67	S31	3352.00	65.00	142	BANK5	1061.00	4585.00



PAD-No	Name	X	Y	PAD-No	Name	X	Y
68	S30	3469.00	65.00	143	BANK6	943.00	4585.00
69	S29	3586.00	65.00	144	LOSC2	825.00	4585.00
70	S28	3703.00	65.00	145	LOSC1	707.00	4585.00
71	S27	3820.00	65.00	146	CLKOUT	589.00	4585.00
72	S26	3937.00	65.00	147	VDD	471.00	4585.00
73	S25	4054.00	65.00	148	VR	353.00	4585.00
74	S24	4171.00	65.00	149	VLCD	230.00	4585.00
75	S23	4291.00	65.00				



12. APPLICATION CIRCUIT :





1. Customer's Name : _____
2. Project title : _____
3. Syntek part number : _____ (will be filled by Syntek)
4. Package ----- () Chip () QFP
5. Options :
- Oscillator type ----- () RC () XTAL
- Operating mode ----- () STK55C2081 () STK55C2080
6. Customer code :
- Code form ----- () EPROM () file _____
- Checksum ----- 0000-3FFF _____H
- 4000-7FFF _____H
- 8000-BFFF _____H
- C000-FFFF _____H
- 0000-FFFF _____H
7. Operating conditions :
- All the operating conditions listed below are for Syntek reference. Syntek will not guaranty on these values. Please refer to data book or contact Syntek for the guaranty values.
- Operating voltage : _____ - _____ V Voltage doubler : () Yes () No
- Operating current : _____ mA Operating frequency : _____ Hz
- Stand-by current : _____ μ A (LCD On) _____ μ A (LCD Off)
- Sleep current : _____ μ A (LCD Off)

Customer : _____ Salesman : _____ Date : __/__/__