

6 line low capacitance EMI filter and ESD protection
in Micro QFN package

- LCD and CAMERA for Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

The EMIF06-1005M12 is a 6 line highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the input pins.

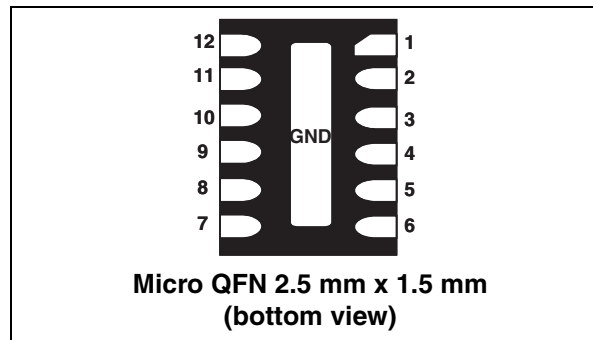
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering: -34 dB at frequencies from 900 MHz to 1.8 GHz
- Very low PCB space consuming: 2.5 mm x 1.5 mm
- Very thin package: 0.6 mm max
- High efficiency in ESD suppression on inputs pins (IEC 61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging.
- Lead free package

Complies with following standards:

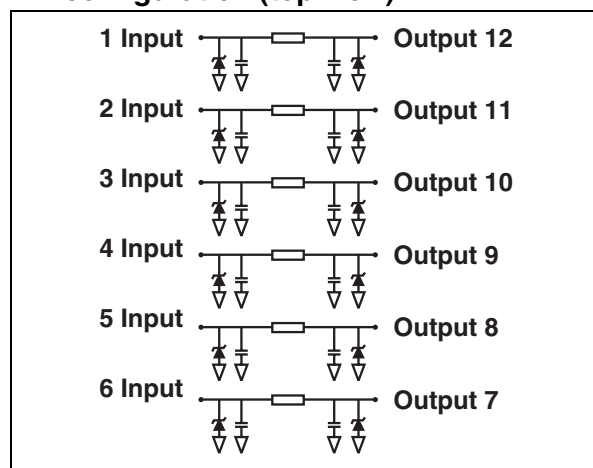
IEC 61000-4-2

level 4 input and output pins	15kV (air discharge) 8kV (contact discharge)
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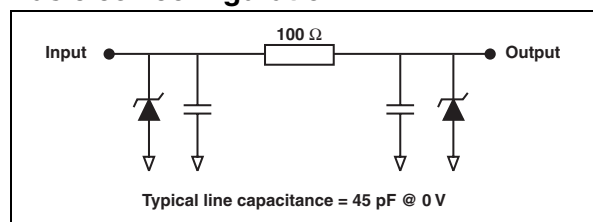
MIL STD 883E - Method 3015-6 Class 3 (all pins)



Pin configuration (top view)



Basic cell configuration

**Order code**

Part number	Marking
EMIF06-1005M12	F

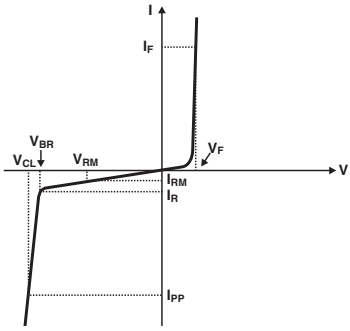
TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute ratings (limiting values at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2 air discharge on input pins	15	kV
	ESD discharge IEC 61000-4-2 contact discharge on input pins	8	
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

Table 2. Electrical characteristics ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter	
V_{BR}	Breakdown voltage	
I_{RM}	Leakage current @ V_{RM}	
V_{RM}	Stand-off voltage	
V_{CL}	Clamping voltage	
R_d	Dynamic resistance	
I_{PP}	Peak pulse current	
$R_{I/O}$	Series resistance between Input & Output	
C_{line}	Input capacitance per line	

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	8	10	V
V_F	$I = 10\text{ mA}$	0.5	1.0	1.5	
I_{RM}	$V_{RM} = 3\text{ V per line}$			200	nA
$R_{I/O}$	Tolerance $\pm 10\%$	90	100	110	Ω
C_{line}	$V_R = 0\text{ V}$	38	45	52	pF

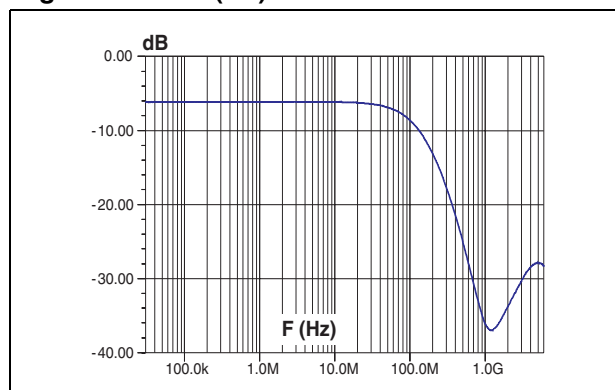
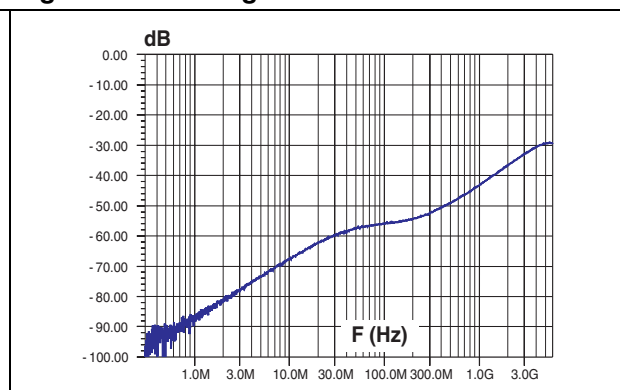
Figure 1. S21(dB) attenuation measurement

Figure 2. Analog cross talk measurements


Figure 3. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

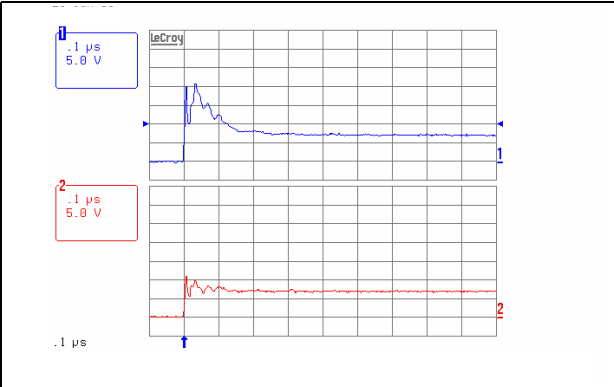


Figure 4. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

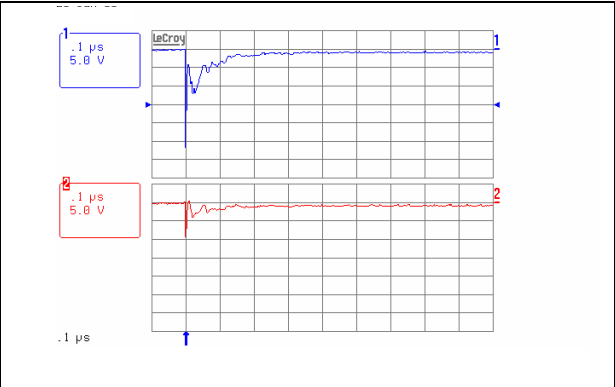
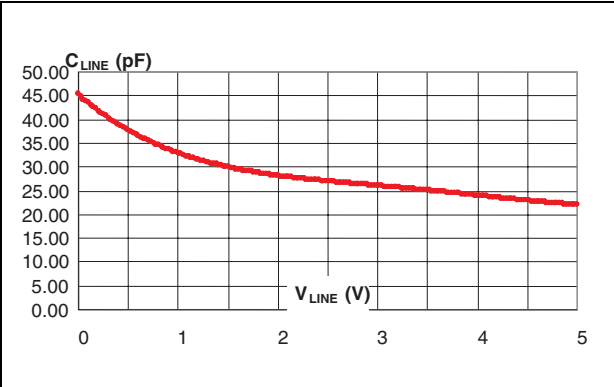
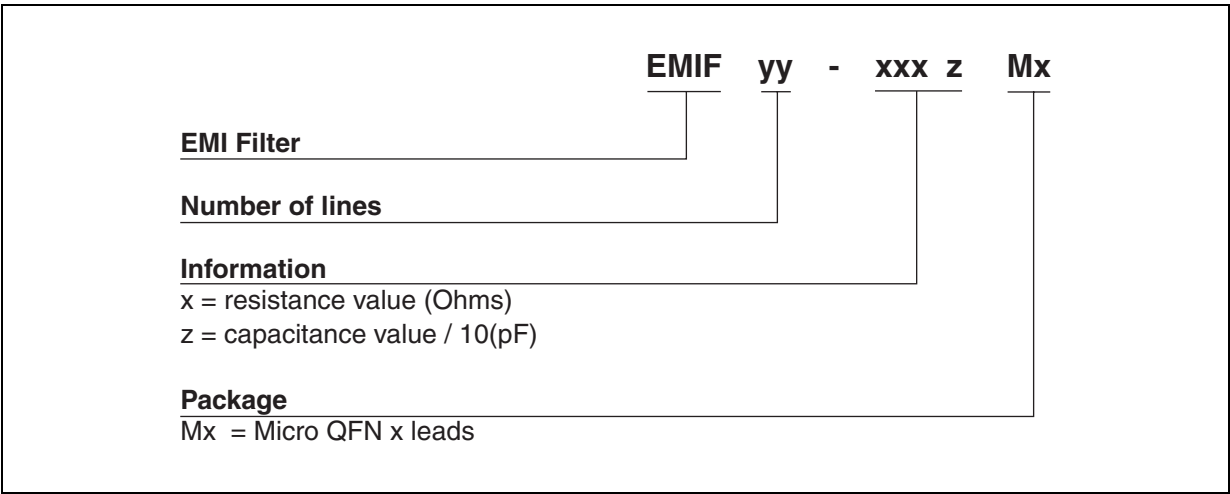


Figure 5. Line capacitance versus reverse voltage applied (typical value)



2 Ordering information scheme



3 Package information

Table 3. QFN 2.5 x 1.5 package dimensions

Ref	Dimensions					
	Millimeters			inches		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.50	0.55	0.60	0.20	0.22	0.24
A1	0.00	0.02	0.05	0.00	0.01	0.02
b	0.15	0.18	0.25	0.06	0.07	0.10
D		2.50			0.98	
D2	1.70	1.80	1.90	0.67	0.71	0.75
E		1.50			0.59	
E2	0.30	0.40	0.50	0.12	0.16	0.24
e		0.40			0.16	
k	0.20			0.08		
L	0.25	0.30	0.35	0.10	0.12	0.14

Figure 6. Footprint

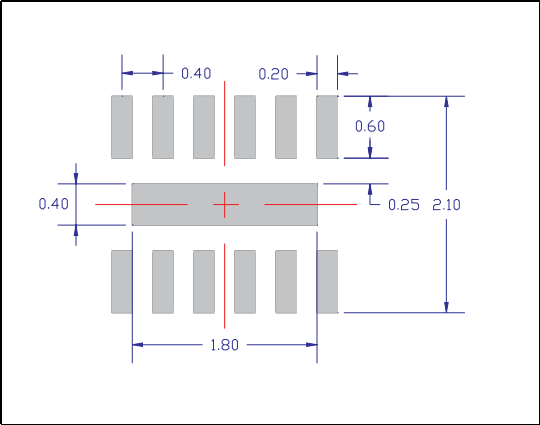


Figure 7. Marking

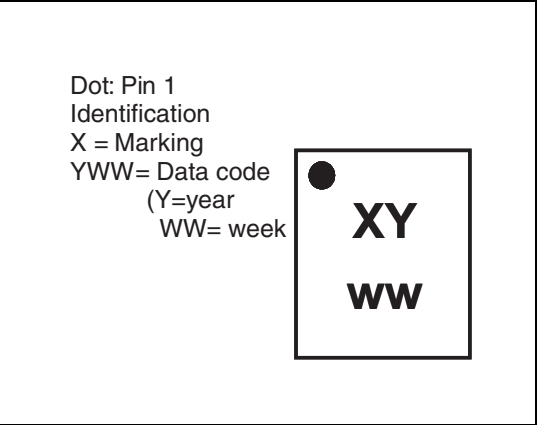
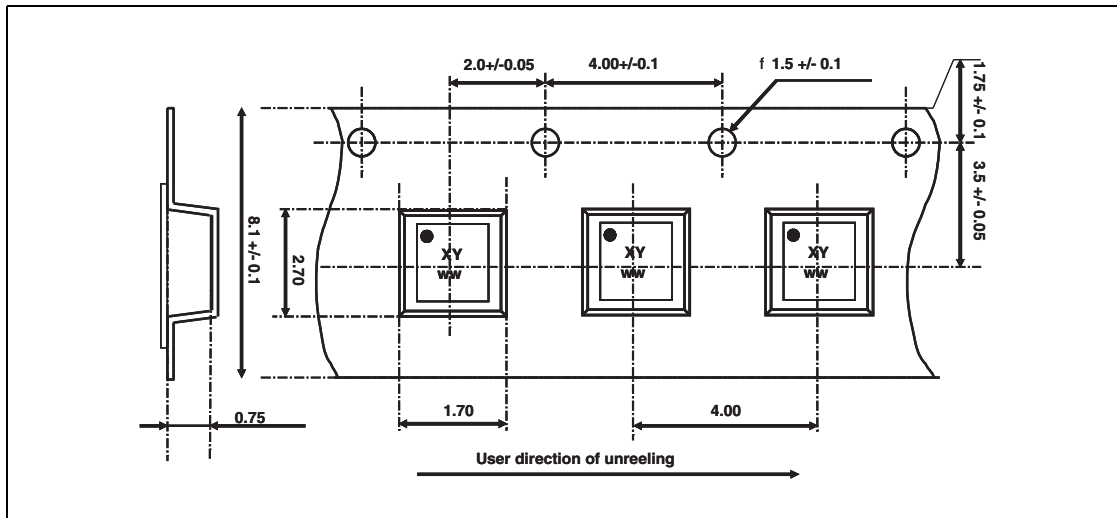


Figure 8. Tape and reel specification

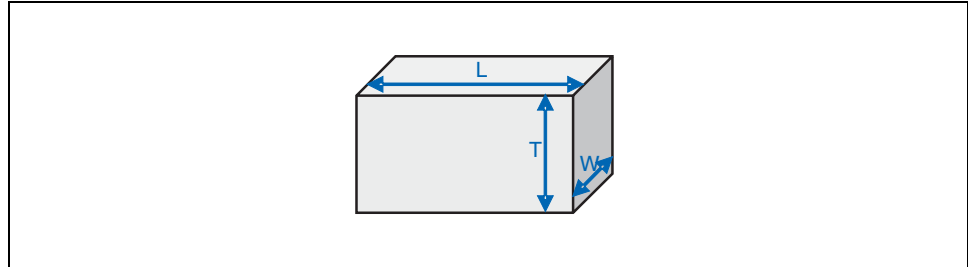


In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
 - a) Stencil Opening Dimensions: L (Length), W (Width), T (Thickness).



- b) General Design Rule
Stencil thickness (T) = 75 ~ 125 μm
Aspect Ratio = $\frac{W}{T} \geq 1.5$
Aspect Area = $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Reference design
 - a) Stencil opening thickness: 100 μm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
Example: Stencil opening L = 1224 μm , W = 300 μm ,
Footprint (see [Figure 6.](#)) L = 1800 μm , W = 400 μm .
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.
Example: Stencil opening L = 570 μm , W = 190 μm ,
Footprint (see [Figure 6.](#)) L = 600 μm , W = 200 μm .

4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 μm .

4.3 Placement

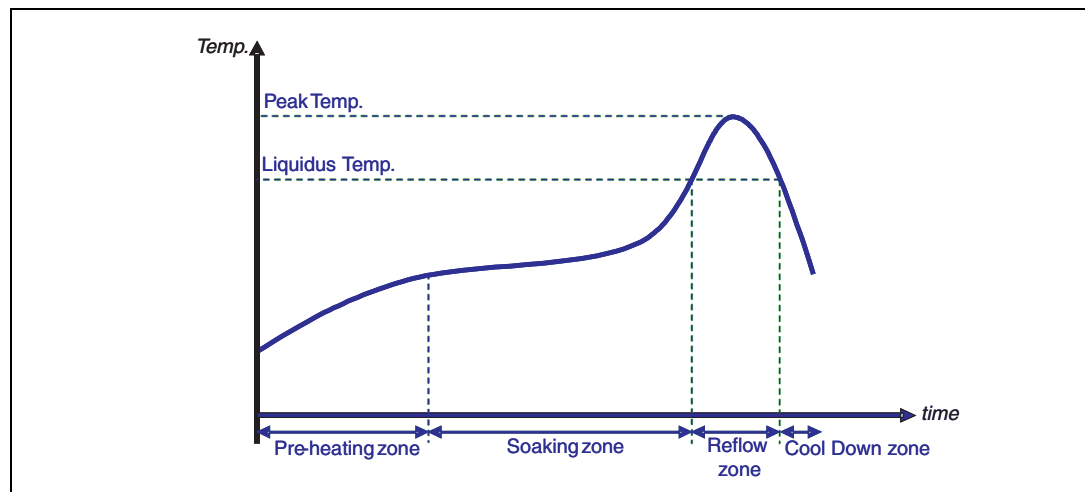
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.

4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile



Parameters	Tin-lead Alloy	Lead-Free Alloy
	[SnPb - SnPbAg]	[SnAgCu]
Pre-heating rate	$\leq 2.5^{\circ} \text{C/s}$	$\leq 2.5^{\circ} \text{C/s}$
Soaking temp.	120-180° C	140-180° C
Soaking time	80-120 s	80-180 s
Peak temperature	210-240° C	245-260° C
Reflow time above liquidus	40-80 s	40-140 s
Cool down rate	$< 6^{\circ} \text{C/s}$	$< 6^{\circ} \text{C/s}$

Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-1005M12	F	Micro QFN	6 mg	3000	Tape and reel (7")

6 Revision history

Date	Revision	Changes
3-Jul-2006	1	Initial release.

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